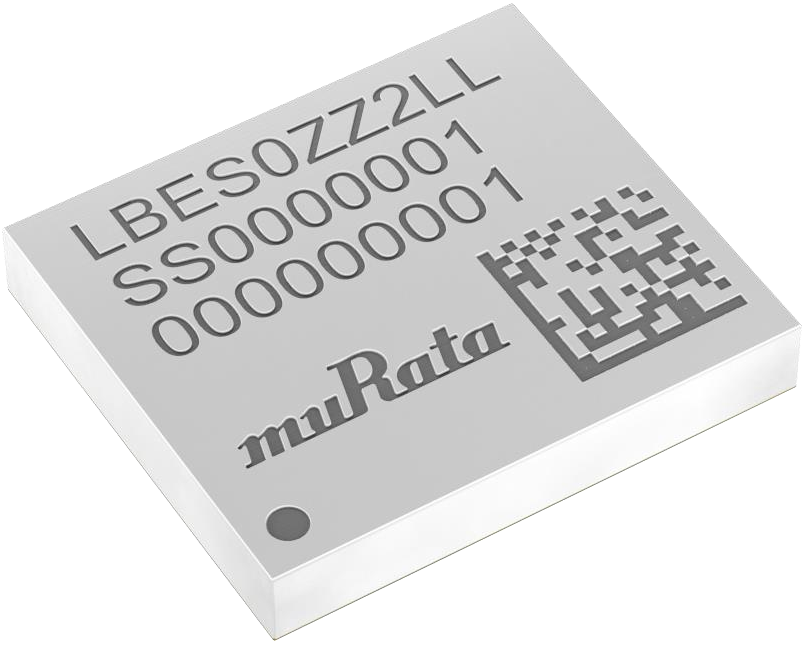
Datasheet

Wi-Fi™+ Bluetooth® + 802.15.4 Tri-Radio Module

NXP IW610G Chipset for 802.11a/b/g/n/ac/ax (HE20) + Bluetooth 5.4 + IEEE 802.15.4 Datasheet - Rev. 2

- Design Name: Type 2LL
- P/N: LBES0ZZ2LL -001



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About This Document

Murata's Type 2LL is a small and very high-performance module based on NXP IW610G combo chipset, supporting IEEE 802.11a/b/g/n/ac/ax (HE20) + Bluetooth 5.4 LE + 802.15.4. This datasheet describes Type 2LL module in detail.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product. In particular RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Murata Manufacturing Co., Ltd. Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This specification characterizes the IEEE 802.11 a/b/g/n/ac/ax (HE20) + Bluetooth 5.4 Low Energy + 802.15.4 tri-radio solution combo module.

2 Key Features

- NXP IW610G inside
- Supports IEEE 802.11a/b/g/n/ac/ax specification: Dual band 2.4 GHz and 5 GHz Wi-Fi 6
- SISO with 20 MHz channels
- Up to MCS9 data rates 114.7 Mbps
- Supports Bluetooth specification version 5.4
- Supports IEEE 802.15.4
- WLAN interface: SDIO 3.0
- Bluetooth interface: HCI UART and PCM_SYNC for BLE audio (PCM over UART)
- 802.15.4 interface: SPI
- Temperature Range: -40 °C to 85 °C
- Dimensions: 8.8 x 7.7 x 1.3 mm
- Weight: 0.223g
- MSL: 3
- Surface-mount type
- RoHS compliant
- Total FIT: 30
- NXP EdgeLockTM security technology
- IW610G targets SESIP Level 3, IEC-62443 and EU RED article 3(3)

3 Ordering Information

Table 2 describes the ordering information.

Table 2: Ordering Information

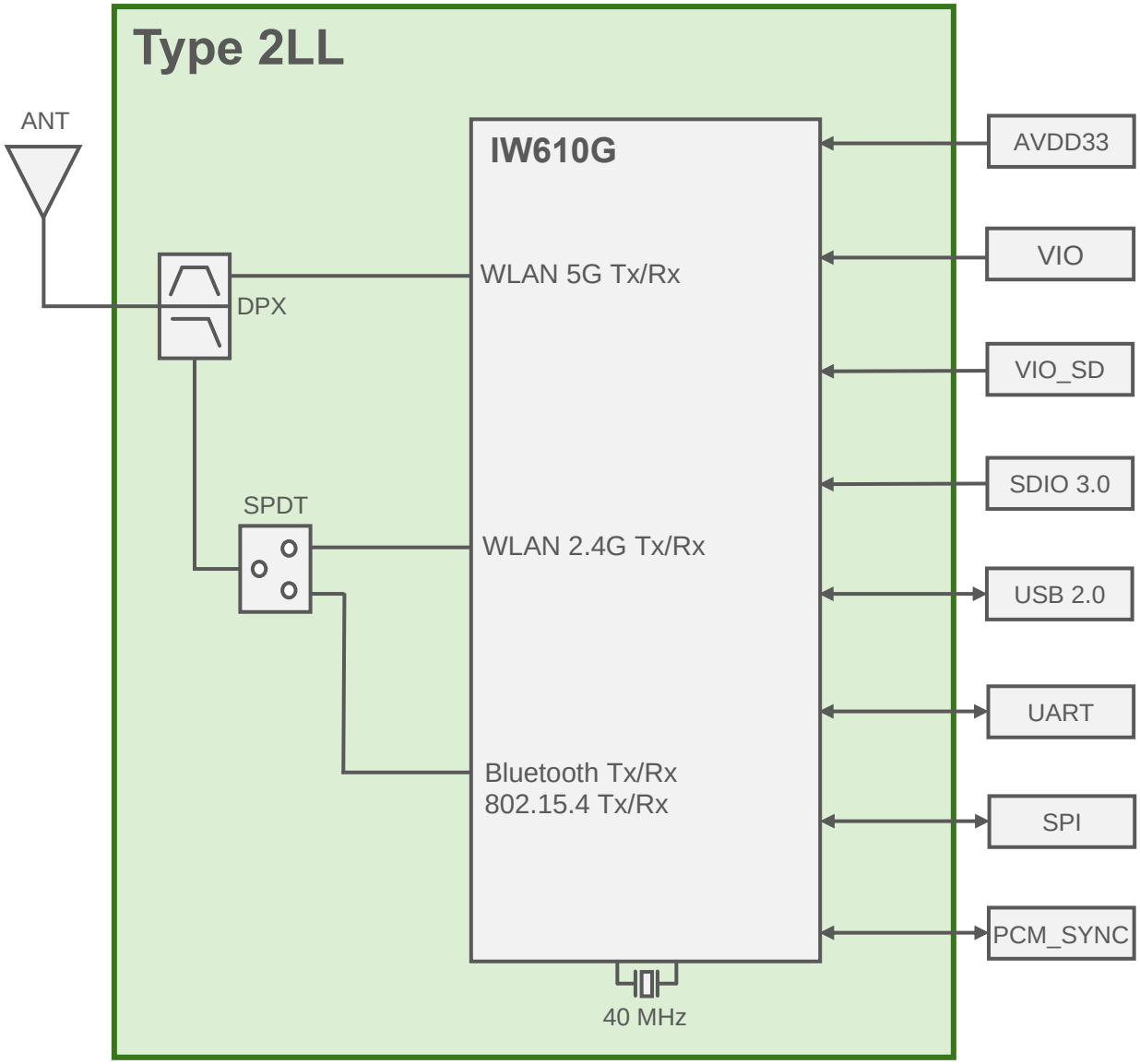
Ordering Part Number	Description
LBES0ZZ2LL-001	Module order
LBES0ZZ2LL-SMP	Sample module order (If module samples are not available through distribution, contact Murata referencing this part number)
EAR00500	Embedded Artists Type 2LL M.2 EVB (default EVB available through distribution)
LBES0ZZ2LL-EVB	Murata Type 2LL M.2 EVB (contact Murata as this is special order item)

"Type 2LL" is design name of this module. Design name may be used in certification test report.

4 Block Diagram

The Type 2LL block diagram is presented in **Figure 1.**

Figure 1: Block Diagram - Type 2LL for the shared WLAN-Bluetooth/802.15.4 antenna



5 Certification Information

This section has information about radio and Bluetooth certification.

5.1 Radio Certification

Transmit output power setting is defined by “txpower_XX.bin” The transmit power files are hosted at Murata GitHub for Linux and FreeRTOS. **Table 3**: Transmit Power Limit Files shows the transmit power file required for each region.

Table 3: Transmit Power Limit Files

Country	ID	Country Code	Tx Power Limit File	
			Linux	FreeRTOS
USA (FCC)	VPYLBES0ZZ2LL	US	txpower_US.bin	wlan_txpwrlimit_cfg_murata_2LL_US.h
Canada (IC)	772C-LBES0ZZ2LL	CA	txpower_CA.bin	wlan_txpwrlimit_cfg_murata_2LL_CA.h
Europe	EN300328/301893, EN300440 conducted test report is prepared.	DE	txpower_EU.bin	wlan_txpwrlimit_cfg_murata_2LL_DE.h
Japan	Japanese type certification is prepared. 003-250020	JP	txpower_JP.bin	wlan_txpwrlimit_cfg_murata_2LL_JP.h

5.2 Radio Regulatory Certification by Country

Murata have prepared the document about Radio Regulatory Certification separately.

This document is designed to ensure that module manufacturers correctly communicate the necessary information to host manufacturers that incorporate their modules.

Refer to 【Regulatory Information】 : Type 2LL Radio Law Approval Application Note for Radio Law Certification user manual.

If you don’t follow the rule written in Type 2LL Radio Law Approval Application Note, there is a risk of conflict Radio Law Certification.

Please be sure to check the document.

5.3 Bluetooth Qualification

- DN: Q343191
- Set Bluetooth Tx Power to Class 1 by using bt_power_config_1.sh.
- For supported Bluetooth functions, refer to Bluetooth SIG site.

6 Dimensions, Markings and Terminal Configurations

This section provides information about dimensions, markings, and terminal configuration for Type 2LL and the related parameters. **Figure 2** shows the dimensions, markings, and terminal configurations.

Figure 2: Dimensions, Markings and Terminal Configurations

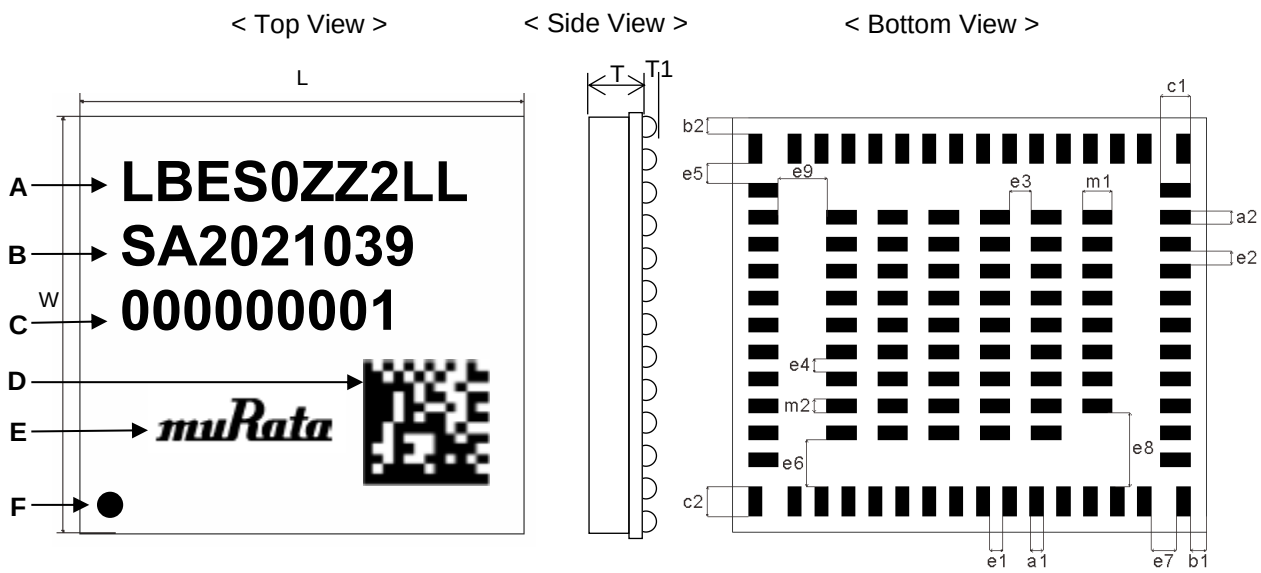


Table 4 describes the Type 2LL markings.

Table 4: Markings

Marking	Meaning
A	Module Type
B	Inspection Number
C	Serial Number
D	2D code
E	Murata Logo
F	Pin 1 Marking

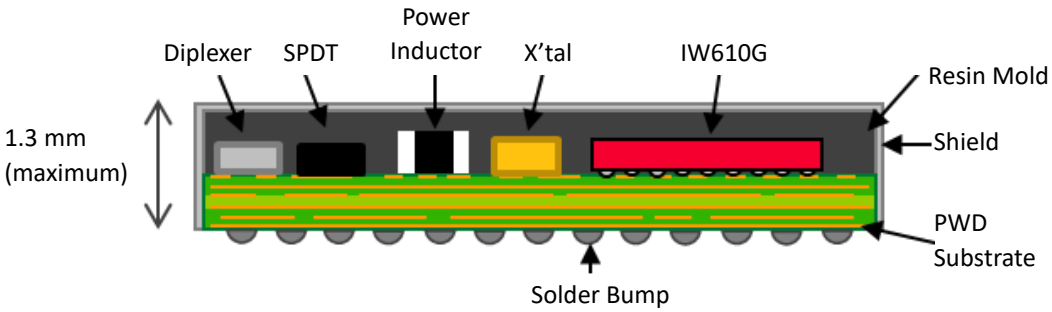
Table 5 describes the Type 2LL dimensions.

Table 5: Dimensions

Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)
L	8.8 +/- 0.2	W	7.7 +/- 0.2		
T	1.3 maximum	T1	0.04 typical (Bump)		
a1	0.25 +/- 0.1	a2	0.25 +/- 0.1	b1	0.3 +/- 0.2
b2	0.3 +/- 0.2	c1	0.55 +/- 0.1	c2	0.55 +/- 0.1
e1	0.25 +/- 0.1	e2	0.25 +/- 0.1	e3	0.4 +/- 0.1
e4	0.25 +/- 0.1	e5	0.375 +/- 0.1	e6	0.875 +/- 0.1
e7	0.475 +/- 0.1	e8	1.375 +/- 0.1	e9	0.9 +/- 0.1
m1	0.55 +/- 0.1	m2	0.25 +/- 0.1		

Figure 3 shows Type 2LL Structure.

Figure 3: Structure



The sides of the module are GND shielded. In order to avoid contact between the GND shield and the electrodes on the mother board, please carefully evaluate the standoff before use the module.

7 Module Pin Descriptions

This section includes the pin descriptions of Type 2LL and pin assignments layout descriptions.

7.1 Pin Assignments

This section describes the pin assignments to terminals. Type 2LL pin-assignment top view is presented in **Figure 4**.

Figure 4: Pin Assignments (Top View)

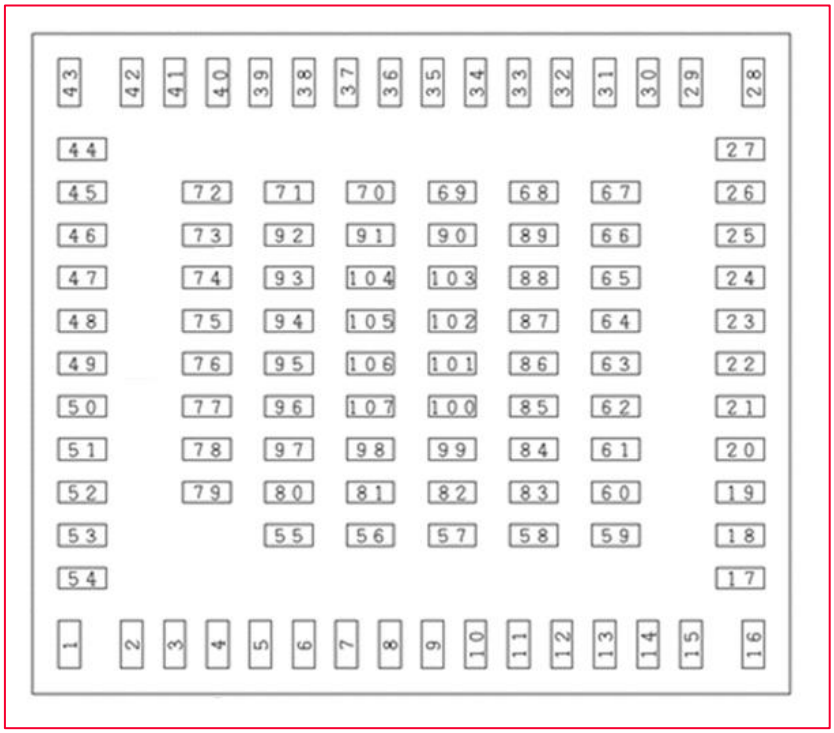


Table 6 lists the Type 2LL terminal configurations.

Table 6: Terminal Configurations

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	29	GND	57	NC	85	GND
2	GND	30	NC	58	Reserved	86	GND
3	AVDD33_USB	31	NC	59	Reserved	87	GND
4	SPI_FRMn	32	GND	60	CONFIG_HOST_BOOT[2]/SD_VOLTAGE_SEL	88	GND
5	SPI_INT	33	NC	61	NC	89	GND
6	SPI_RXD/ PCM_SYNC	34	AVDD18_USB_OUT	62	GND	90	GND
7	SPI_TXD	35	NC	63	IND_RST_WL	91	GND
8	SPI_CLK	36	AVDD18_USB_IN	64	IND_RST_BT	92	GND
9	GND	37	NC	65	EXT_GNT	93	GND
10	PDn	38	IND_RST_NB	66	EXT_REQ	94	GND
11	GND	39	GND	67	GND	95	GND
12	AVDD33	40	SD_VIO	68	GND	96	GND
13	AVDD33	41	GND	69	WCI-2_SIN/ EXT_STATE	97	GND
14	GND	42	SD_CMD	70	WCI-2_SOUT/ EXT_FREQ	98	GND
15	ANT0	43	GND	71	GND	99	GND
16	GND	44	SD_CLK	72	SD_INT/USB_VBUS_ON	100	GND
17	GND	45	SD_DAT[1]	73	WL_WAKE_OUT	101	GND
18	NC	46	SD_DAT[3]	74	WL_WAKE_IN	102	GND
19	GND	47	SD_DAT[2]	75	NB_WAKE_IN	103	GND
20	GND	48	SD_DAT[0]	76	NB_WAKE_OUT	104	GND
21	GND	49	UART_SOUT	77	USB_DP	105	GND
22	GND	50	UART_CTSn	78	USB_DM	106	GND
23	Reserved	51	UART_SIN	79	XOSC_EN	107	GND
24	NC	52	UART_RTSn	80	EXT_PRI		
25	RF_CNTL3	53	GND	81	GND		
26	RF_CNTL2	54	VIO	82	GND		
27	RF_CNTL0	55	CONFIG_HOST[0]	83	GND		
28	GND	56	CONFIG_HOST[1]	84	GND		

7.2 Pin Descriptions

Table 7 shows the pin descriptions.

Table 7: Pin Descriptions

No.	Terminal Name	Type	Connection to IC Terminal	Description
1	GND			Ground
2	GND			Ground
3	AVDD33_USB		USB_AVDD33	USB Power supply 2EL>>Not Connected
4	SPI_FRMn	I/O	SPI_FRM/GPIO[8]	**GPIO mode:** GPIO[8] (input/output) **SPI host interface mode:** SPI_FRM - SPI data frame signal (input), driven by the SPI controller. The signal is active low and also known as SPI chip select. **Bluetooth LE host trigger mode:** BLE_HOST_TRIG0 - Host trigger pin 0 for Bluetooth LE (input/output)
5	SPI_INT	I/O	CONFIG_HOST_BOOT[3]/SPI_INT	CONFIG_HOST_BOOT[3] bootstrap option pin. Internal weak pull-up. **Wake-up/interrupt mode:** SPI_INT - SPI interrupt output signal.
6	SPI_RXD/PCM_SYNC	I/O	SPI_RXD/PCM_SYNC/ GPIO[7]	**GPIO mode:** GPIO[7] (input/output) **SPI host interface mode:** SPI_RXD - SPI receive signal (input). **Bluetooth LE audio mode:** PCM_SYNC - PCM frame sync signal (input). **Bluetooth LE host trigger mode:** BLE_HOST_TRIG2 - Host trigger pin 2 for Bluetooth LE (input/output)
7	SPI_TXD	I/O	SPI_TXD/GPIO[6]	**GPIO mode:** GPIO[6] (input/output) **SPI host interface mode:** SPI_TXD - SPI transmit signal (output). **Bluetooth LE host trigger mode:** BLE_HOST_TRIG1 - Host trigger pin 1 for Bluetooth LE (input/output)
8	SPI_CLK	I/O	SPI_CLK/GPIO[9]	**GPIO mode:** GPIO[9] (input/output) **SPI host interface mode:** SPI_CLK - SPI clock signal (input) .
9	GND			Ground
10	PDn	I	PDn	Full Power-down (input) (active low) 0 = full power-down mode 1 = normal mode ・PDn can accept an input of 1.75V to 3.63V ・PDn may be driven by the host ・PDn must be high for normal operation No internal pull-up on this pin. This pin has an always-on internal weak pull-down.
11	GND			Ground
12	AVDD33	Power	AVDD33	Power supply
13	AVDD33	Power	AVDD33	Power supply

No.	Terminal Name	Type	Connection to IC Terminal	Description
14	GND			Ground
15	ANT0	I/O		ANT0 is WLAN output and it's also used for Bluetooth LE/802.15.4 output when SANT mode.
16	GND			Ground
17	GND			Ground
18	NC			Not Connected
19	GND			Ground
20	GND			Ground
21	GND			Ground
22	GND			Ground
23	Reserved			Not Connected.
24	NC			Not Connected
25	RF_CNTL3	I/O	RF_CNTL3	**RF control mode:** RF Control 3 - RF control line 3 (output)
26	RF_CNTL2	O	RF_CNTL2	**RF control mode:** RF control 2 - RF control line 2 (output)
27	RF_CNTL0	O	RF_CNTL0	**RF control mode:** RF control 0 - RF control line 1 (output)
28	GND			Ground
29	GND			Ground
30	NC			Not Connected
31	NC			Not Connected
32	GND			Ground
33	NC			Not Connected
34	AVDD18_USB_OUT			AVDD18 output from the module. Connect to AVDD18_USB_IN by >0.25mm trace.
35	NC			Not Connected
36	AVDD18_USB_IN			AVDD18 input. Connect to AVDD18_USB_OUT by >0.25mm trace.
37	NC			Not Connected
38	IND_RST_NB	I/O	IND_RST_NB/GPIO[11]	**GPIO mode:** GPIO[11] (input/output) **Software reset mode:** IND_RST_NB - independent software reset for Bluetooth LE / 802.15.4 radio (input).
39	GND			Ground
40	SD_VIO	Power		SDIO Power supply
41	GND			Ground
42	SD_CMD	I/O	SD_CMD	SDIO 4-bit mode: Command/response (input/output)

No.	Terminal Name	Type	Connection to IC Terminal	Description
43	GND			Ground
44	SD_CLK	I	SD_CLK	SDIO 4-bit mode: Clock input
45	SD_DAT[1]	I/O	SD_DAT[1]	SDIO 4-bit mode: Data line Bit[1]
46	SD_DAT[3]	I/O	SD_DAT[3]	SDIO 4-bit mode: Data line Bit[3]
47	SD_DAT[2]	I/O	SD_DAT[2]	SDIO 4-bit mode: Data line Bit[2] or read wait (optional)
48	SD_DAT[0]	I/O	SD_DAT[0]	SDIO 4-bit mode: Data line Bit[0]
49	UART_SOUT	I/O	UART_SOUT/GPIO[15]	**GPIO mode:** GPIO[15] (input/output) **UART interface mode:** UART_SOUT - UART serial output signal.
50	UART_CTSn	I/O	UART_CTSn/GPIO[12]	**GPIO mode:** GPIO[12] (input/output) **UART interface mode:** UART_CTSn clear-to-send input signal.
51	UART_SIN	I/O	UART_SIN/GPIO[14]	**GPIO mode:** GPIO[14] (input/output) **UART interface mode:** UART_SIN - UART serial input signal.
52	UART_RTSn	I/O	UART_RTSn/GPIO[13]	**GPIO mode:** GPIO[13] (input/output) **UART interface mode:** UART_RTSn request-to-send output signal.
53	GND			Ground
54	VIO	Power		IO Power supply
55	CONFIG_HOST_BOOT[0]	I	CONFIG_HOST_BOOT[0]	CONFIG_HOST_BOOT[0] bootstrap option pin. Refer to sec 7.3
56	CONFIG_HOST_BOOT[1]	I	CONFIG_HOST_BOOT[1]	CONFIG_HOST_BOOT[1] bootstrap option pin. Refer to sec 7.3
57	NC			Not Connected
58	Reserved		JTAG_TCK/GPIO[2]	**GPIO mode:** GPIO[2] (input/output) **JTAG mode:** JTAG_TCK - JTAG test clock (input).
59	Reserved		JTAG_TMS/GPIO[3]	**GPIO mode:** GPIO[3] (input/output) **JTAG mode:** JTAG_TMS - JTAG test mode select (input) (default mode) .
60	CONFIG_HOST[2]/SD_VOLTAGE_SEL		CONFIG_HOST[2]/SD_VOLTAGE_SEL	CONFIG_HOST_BOOT[2] bootstrap option pin. Refer to sec 7.3 **SDIO interface mode:** SD_VOLTAGE_SEL: SDIO voltage select signal (output).
61	NC			Not Connected
62	GND			Ground
63	IND_RST_WL	I/O	IND_RST_WL/GPIO[10]	**GPIO mode:** GPIO[10] (input/output) **Software reset mode:** IND_RST_WL - independent software reset for Wi-Fi radio (input).
64	IND_RST_NB	I/O	IND_RST_NB/GPIO[11]	**GPIO mode:** GPIO[11] (input/output) **Software reset mode:** IND_RST_NB - independent software reset for Bluetooth LE / 802.15.4 radio (input).
65	EXT_GNT	I/O	EXT_GNT/GPIO[20]	**GPIO mode:** GPIO[20] (input/output) **PTA coexistence mode:** EXT_GNT- External radio grant output signal (mandatory)
66	EXT_REQ	I/O	EXT_REQ/GPIO[19]	**GPIO mode:** GPIO[19] (input/output)

No.	Terminal Name	Type	Connection to IC Terminal	Description
				PTA coexistence mode: EXT_REQ - External radio request input signal. Request from the external radio (mandatory).
67	GND			Ground
68	GND			Ground
69	WCI-2_SIN/ EXT_STATE	I/O	WCI-2_SIN/ EXT_STATE/GPIO[22]	**GPIO mode:** GPIO[22] (input/output) **PTA coexistence mode:** EXT_STATE - External radio state input signal (optional). External radio traffic direction (Tx/Rx): ・1: Tx ・0: Rx **WCI-2 coexistence mode:** WCI-2_SIN (input).
70	WCI-2_SOUT/ EXT_FREQ	I/O	WCI-2_SOUT/ EXT_FREQ/GPIO[18]	**GPIO mode:** GPIO[18] (input/output) **PTA coexistence mode:** EXT_FREQ - External radio frequency input signal. Request from the external radio (mandatory). Frequency overlap between external radio and Wi-Fi: ・1: overlap ・0: non-overlap This signal is useful when the external radio is a frequency hopping device. **WCI-2 coexistence mode:** WCI-2_SOUT (output).
71	GND			Ground
72	SD_INT/USB_VBUS_ON	I/O	SD_INT/USB_VBUS_ON /GPIO[1]	**GPIO mode:** GPIO[1] (input/output) **USB mode:** USB voltage indicator/ USB_VBUS/ON (input). Need to pull-up in USB mode. **SDIO mode:** SD_INT - SDIO interrupt signal (output) .
73	WL_WAKE_OUT	I/O	WL_WAKE_OUT/JTAG_ TDI/GPIO[4]	**GPIO mode:** GPIO[4] (input/output) **JTAG mode:** JTAG_TDI - JTAG test data (input). **Wake-up/interrupt mode:** WL_WAKE_OUT - Out-of-band device-to-host wake-up signal (output) for the Wi-Fi radio.
74	WL_WAKE_IN	I/O	WL_WAKE_IN/GPIO[16]	**GPIO mode:** GPIO[16] (input/output) **Wake-up/interrupt mode:** WL_WAKE_IN - Out-of-band host-to-device wake-up signal for Wi-Fi radio (input).
75	NB_WAKE_IN	I/O	NB_WAKE_IN/GPIO[17]	**GPIO mode:** GPIO[17] (input/output) **Wake-up/interrupt mode:** NB_WAKE_IN - Out-of-band host-to-device wake-up signal (input) for Bluetooth LE/802.15.4 radios.
76	NB_WAKE_OUT	I/O	NB_WAKE_OUT/JTAG_ TDO/GPIO[5]	**GPIO mode:** GPIO[5] (input/output) **JTAG mode:** JTAG_TDO - JTAG test data (output) (default mode). **Wake-up/interrupt mode:** NB_WAKE_OUT - Out-of-band device-to-host wake-up signal (output) for Bluetooth LE/802.15. 4 radios.
77	USB_DP	I/O	USB_DP	USB 2.0 Serial Differential Data Plus

No.	Terminal Name	Type	Connection to IC Terminal	Description
78	USB_DM	I/O	USB_DM	USB 2.0 Serial Differential Data Minus
79	XOSC_EN		XOSC_EN/GPIO[0]	**GPIO mode:** GPIO[0] (input/output) **Oscillator enable mode:** XOSC_EN - Oscillator Enable (output) (active high). XOSC_EN signal can be used ONLY when an external sleep clock is used. Used to enable an external oscillator. 0 = disable external oscillator 1 = enable external oscillator
80	EXT_PRI		EXT_PRI/GPIO[21]	**GPIO mode:** GPIO[21] (input/output) **PTA coexistence mode:** EXT_PRI - External radio priority input signal (optional). Priority of the request from the external radio. Can support 1 bit priority (sample once) and 2 bit priority (sample twice). Can also have Tx/Rx info following the priority info if EXT_STATE is not used.
81-107	GND			Ground

- Not all GPIO pins can be used for Host-to-SoC wake-up signals.

7.3 Configuration Pins

Table 8 describes the configuration pins.

Table 8: Configuration Pins

CONFIG_ HOST[0]	CONFIG_ HOST[1]	CONFIG_ HOST[2]	WLAN	Bluetooth LE	802.15.4	Remarks
1	1	0	SDIO	UART	SPI	Default
1	0	1	USB	USB	SPI	

7.4 Pin States

Pin states information of **Table 9**: I/O State Table include:

- After firmware is downloaded, the pads (GPIO, Serial interface, RF control) are programmed in functional mode per the functionality of the pins.
- For SDIO, once the command is received from the host, the pads are configured accordingly.
- Pull-up and pull-down are only effective when the pad is in input mode.
- The power-down state shown is the default configuration. Many pads have programmable power-down values, which can be set by firmware.
- Do not need any termination to the open pins that have an Internal Pull-up/Pull-down resistor (PU/PD). Do not need any termination to the open pins in output mode.

Table 9: I/O State Table

Pin Name	Supply	No Pad Power State	Reset State	HW State	Power Down State	Power Down Prog	Internal PU/PD	Int'l Pull Value[Ω]
SPI_FRMn	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
SPI_INT	AVDD18	tristate	input	output high/ output low	tristate	no	weak PU	800kΩ
SPI_RXD/PCM_SYNC	VIO	tristate	input	input	tristate	Yes	nominal PU	100kΩ
SPI_TXD	VIO	tristate	input	input/output low	tristate	yes	nominal PU	100kΩ
SPI_CLK	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
PDn	AVDD33						weak PD	90kΩ
RF_CNTL3	VIO_RF	tristate	input	input	drive high	yes	weak PU	800kΩ
RF_CNTL2	VIO_RF	tristate	input	input	drive low	yes	weak PU	800kΩ
RF_CNTL0	VIO_RF	tristate	input	input	drive low	yes	weak PU	800kΩ
IND_RST_NB	VIO	tristate	output low	output low	tristate	yes	nominal PU	100kΩ
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	100kΩ
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	100kΩ
SD_DAT[1]	VIO_SD	tristate	input	input	tristate	no	nominal PU	100kΩ
SD_DAT[3]	VIO_SD	tristate	input	input	tristate	no	nominal PU	100kΩ
SD_DAT[2]	VIO_SD	tristate	input	input	tristate	no	nominal PU	100kΩ
SD_DAT[0]	VIO_SD	tristate	input	input	tristate	no	nominal PU	100kΩ
UART_SOUT	VIO	tristate	input	input/output high	tristate	yes	nominal PU	100kΩ
UART_CTSn	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ

Pin Name	Supply	No Pad Power State	Reset State	HW State	Power Down State	Power Down Prog	Internal PU/PD	Int'l Pull Value[Ω]
UART_SIN	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
UART_RTSn	VIO	tristate	input	input/output high	tristate	yes	nominal PU	100kΩ
CONFIG_HOST[0]	AVDD18	tristate	input	output high	tristate	no	weak PU	800kΩ
CONFIG_HOST[1]	AVDD18	tristate	input	output low	tristate	no	weak PU	800kΩ
CONFIG_HOST[2]/ SD_VOLTAGE_SEL	AVDD18	tristate	intput	input/output high/output low	tristate	no	weak PU	800kΩ
IND_RST_WL	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
IND_RST_NB	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
EXT_GNT	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
EXT_REQ	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
WCI-2_SIN/ EXT_STATE	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
WCI-2_SOUT/ EXT_FREQ	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
SD_INT/ USB_VBUS_ON	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
WL_WAKE_OUT	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
WL_WAKE_IN	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
NB_WAKE_IN	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
NB_WAKE_OUT	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
XOSC_EN	VIO	tristate	output high	output high	tristate	yes	nominal PU	100kΩ
EXT_PRI	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
USB_DP	AVDD33_USB							
USB_DM	AVDD33_USB							
Reserved (58)	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ
Reserved (59)	VIO	tristate	input	input	tristate	yes	nominal PU	100kΩ

- UART_RTSn : HW State Output high for UART interface
- SPI_TXD : HW State Output high for SPI interface
- CONFIG_HOST[2] : HW State Input low/high for SDIO interface
- CONFIG_HOST[3] : HW State Output high for SPI interface

8 Absolute Maximum Ratings

Table 10 describes the absolute maximum ratings.

Table 10: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-40	+85	°C
Supply Voltage	AVDD33		3.96	V
	AVDD33_USB		3.96	V
	SD_VIO 1.8V/3.3V		2.16	V
			3.96	V
	VIO 1.8V/3.3V		2.16	V
			3.96	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

9 Operating Conditions

9.1 Operating Conditions

Type 2LL operating conditions are described in **Table 11**.

Table 11: Operating Conditions

Parameter		Minimum	Typical	Maximum	Unit
Operating Temperature	Ta	-40	25	+85	°C
	Tj			+125	°C
Supply Voltage	AVDD33	3.14	3.3	3.46	V
	AVDD33_USB	3.14	3.3	3.46	V
	SD_VIO/VIO = 1.8V	1.71	1.8	1.89	V
	SD_VIO/VIO = 3.3V	3.14	3.3	3.46	V
Peak current	AVDD33			750	mA

- Operation beyond the recommended operating conditions is neither recommended nor guaranteed.
- Peak current happens during DPD calibration when the firmware is downloaded.

9.2 Digital I/O Requirements

The digital I/O requirements are listed in **Table 12** and **Table 13**.

Table 12: Digital I/O Requirements Parameters – 1.8V Operation

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VIO	I/O pad supply voltage		1.71	1.8	1.89	V
VIH	Input high voltage		0.7 * VIO		VIO + 0.4	V
VIL	Input low voltage		-0.4		0.3 * VIO	V
VHYS	Input hysteresis		100			mV
VOH	Output high voltage		VIO-0.4			V
VOL	Output low voltage				0.4	V

Table 13: Digital I/O Requirements Parameters – 3.3V Operation

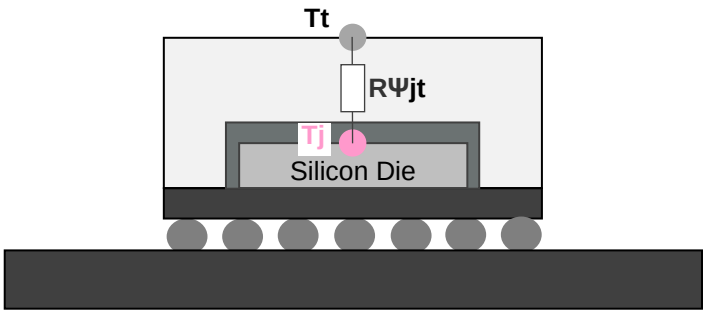
Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
VIO	I/O pad supply voltage		3.14	3.3	3.46	V
VIH	Input high voltage		0.7 * VIO		VIO + 0.4	V
VIL	Input low voltage		-0.4		0.3 * VIO	V
VHYS	Input hysteresis		100			mV
VOH	Output high voltage		VIO-0.4			V
VOL	Output low voltage				0.4	V

9.3 Package Thermal Conditions

- RΨjt：0.27 ℃/W
- RΨjt = (Tj - Tt)/P

Tj: Junction temperature (℃), Tt: Top temperature (℃), P: Total Power Consumption (W)

Figure 5: Package Thermal Conditions



10 Power Sequence

10.1 Power-On Sequence

The Type 2LL does not have power-on sequence requirements other than AVDD33 and AVDD33_USB to be powered up no later than the other external supply rails. The power-down pin (PDn) must be held low (asserted) until all power supply rails are stable.

Figure 6: Power-On Sequence Graph shows the power-on sequence graph.

Figure 6: Power-On Sequence Graph

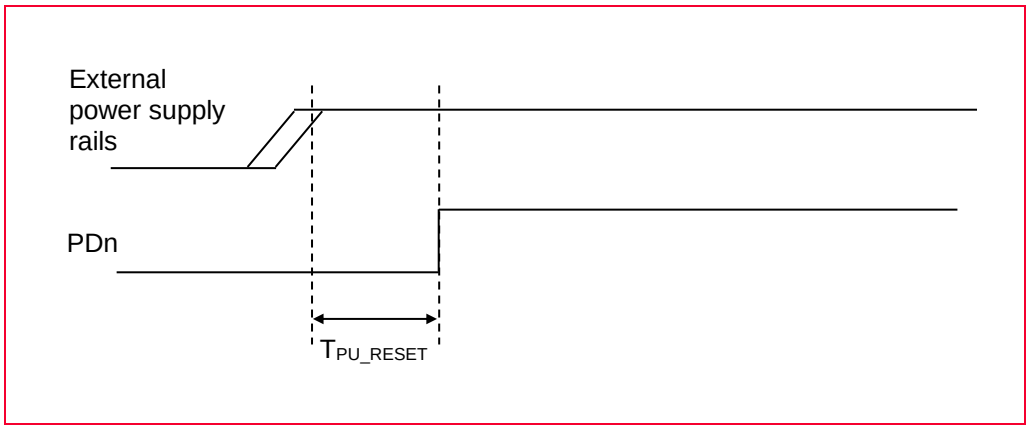


Table 14: PDn Pin Specifications shows the PDn pin (power-off) specifications. Power remains high at PDn assertion.

Table 14: PDn Pin Specifications

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{PU_RESET}	Valid power to PDn de-asserted		0			ms
V_{IH}	Input high voltage		1.75		3.63	V
V_{IL}	Input low voltage		-0.4		0.2	V

Minimum value is guaranteed for a valid rest. Smaller values may put the device in an undefined state.

10.2 Power-Off Sequence

The Type 2LL does not have power-off sequence requirements other than AVDD33 and AVDD33_USB to be powered off no later than the other external supply rails. The power-down pin (PDn) must be held low (asserted) before all power supply rails are powered off.

Figure 7 shows the power-off sequence graph.

Figure 7: Power-Off Sequence Graph

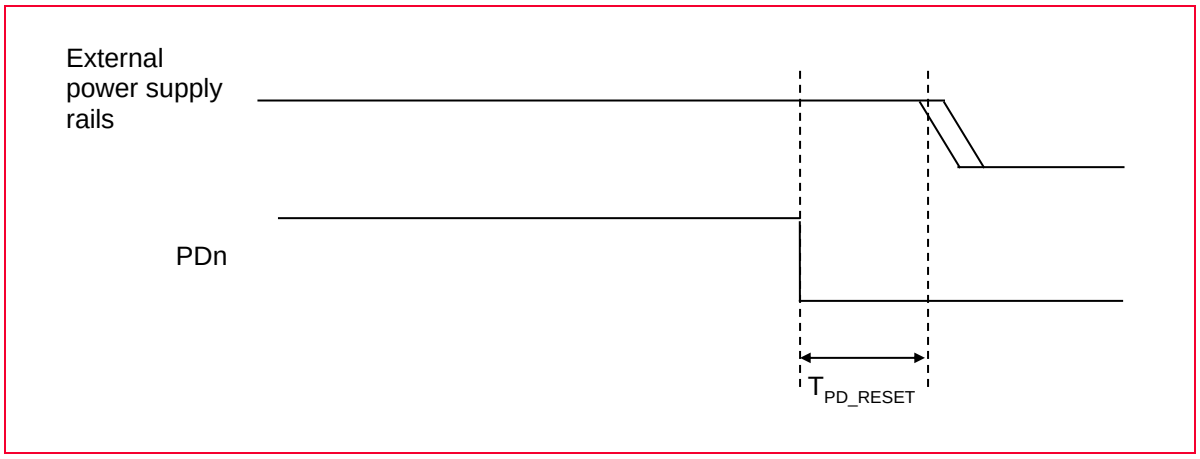


Table 15 shows the power-off sequence parameters.

Table 15: Power-Off Sequence Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{PU_RESET}	Valid power to PDn de-asserted		0			ms
V_{IH}	Input high voltage		1.75		3.63	V
V_{IL}	Input low voltage		-0.4		0.2	V

10.3 Host Reset Sequence

Figure 8 shows hot reset sequence graph.

Figure 8: Host Reset Sequence Graph

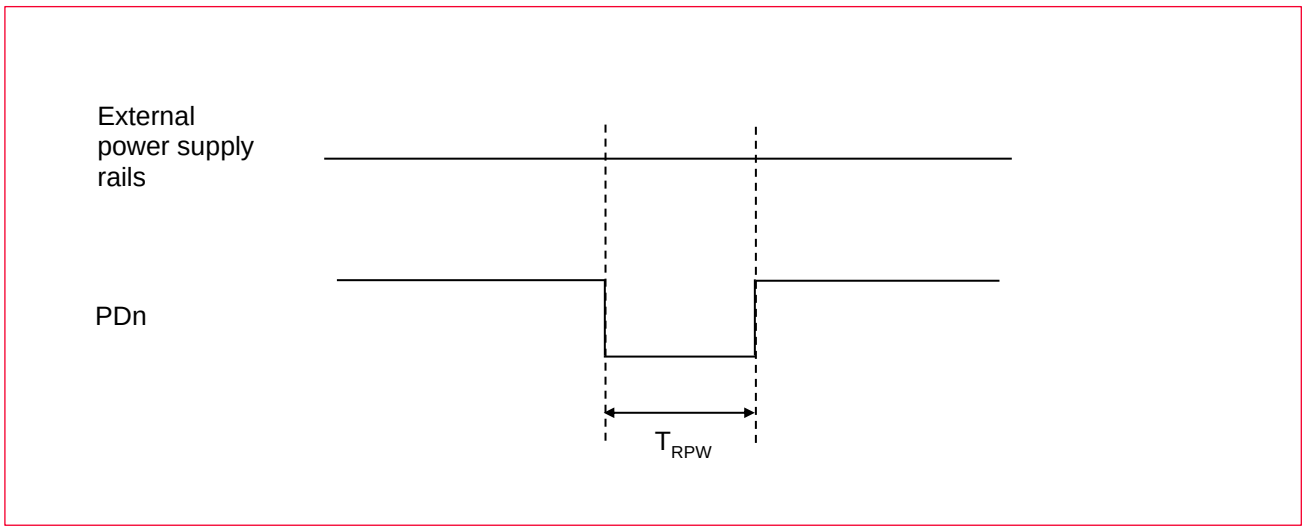


Table 16: Host Reset Sequence Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{PRW}	PDn pulse width		T_{RD}			µs
V_{IH}	Input high voltage		1.75		3.63	V
V_{IL}	Input low voltage		-0.4		0.2	V

T_{RD} : Minimum value is guaranteed for a valid rest. Smaller values may put the device in an undefined state.

11 Interface Timing

This section describes interface timings:

- SDIO timing (default and high-speed modes)
- SDIO protocol timings
- UART timing (default mode)
- Bluetooth PCM timing (master and slave mode)

11.1 SDIO Timing

11.1.1 Default Speed Mode

Figure 9 describes the SDIO protocol timing diagram in default speed mode.

Figure 9: SDIO Protocol Timing Diagram - Default Mode

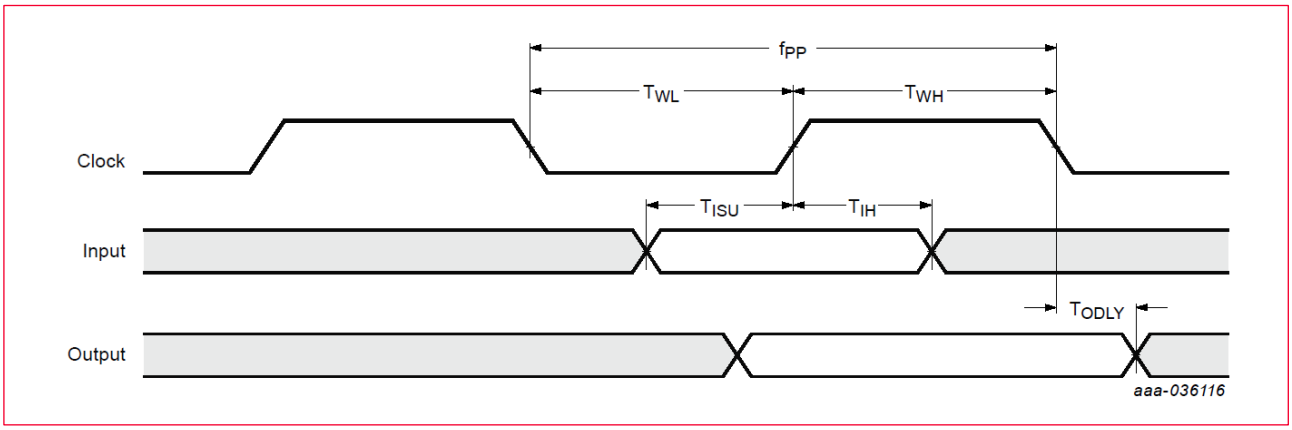


Table 17: SDIO Protocol Timing Parameters describes the parameters for SDIO protocol timing parameters.

Table 17: SDIO Protocol Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	0		25	MHz
T_{WL}	Clock low time	10			ns
T_{WH}	Clock high time	10			ns
T_{ISU}	Input setup time	5			ns
T_{IH}	Input hold time	5			ns
T_{ODLY}	Output delay time $C_L \leq 40$ pF (1 card)			14	ns

For SDIO 2.0 running at 25 MHz clock frequency, VIO_SD must be 3.3V.

11.1.2 High Speed Mode

Figure 10 describes the SDIO protocol timing diagram in high-speed mode.

Figure 10: SDIO Protocol Timing Diagram - High Speed Mode

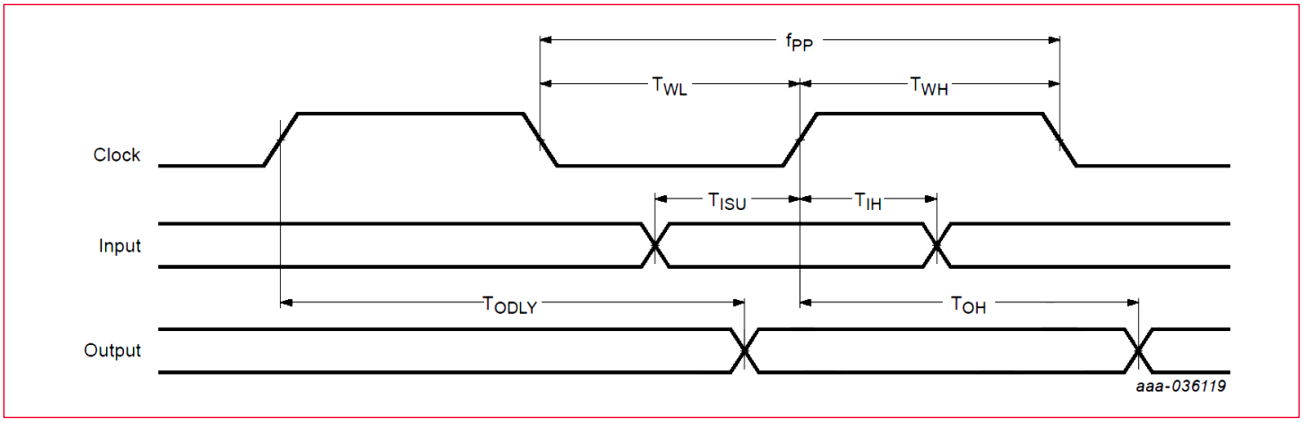


Table 18 describes the parameters for SDIO protocol timing parameters.

Table 18: SDIO Protocol Timing Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	0		50	MHz
T_{WL}	Clock low time	7			ns
T_{WH}	Clock high time	7			ns
T_{ISU}	Input setup time	6			ns
T_{IH}	Input hold time	2			ns
T_{ODLY}	Output delay time $C_L \leq 40$ pF (1 card)			14	ns
T_{OH}	Output hold time	2.5			ns

For SDIO 2.0 running at 50 MHz clock frequency, VIO_SD must be 3.3V.

11.1.3 SDR12, SDR25, SDR50 Modes (up to 100 MHz) at 1.8V

Figure 11 shows SDIO protocol timing diagram for SDR12, SDR25, SDR50 Mode (up to 100 MHz) at 1.8V.

Figure 11: SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes

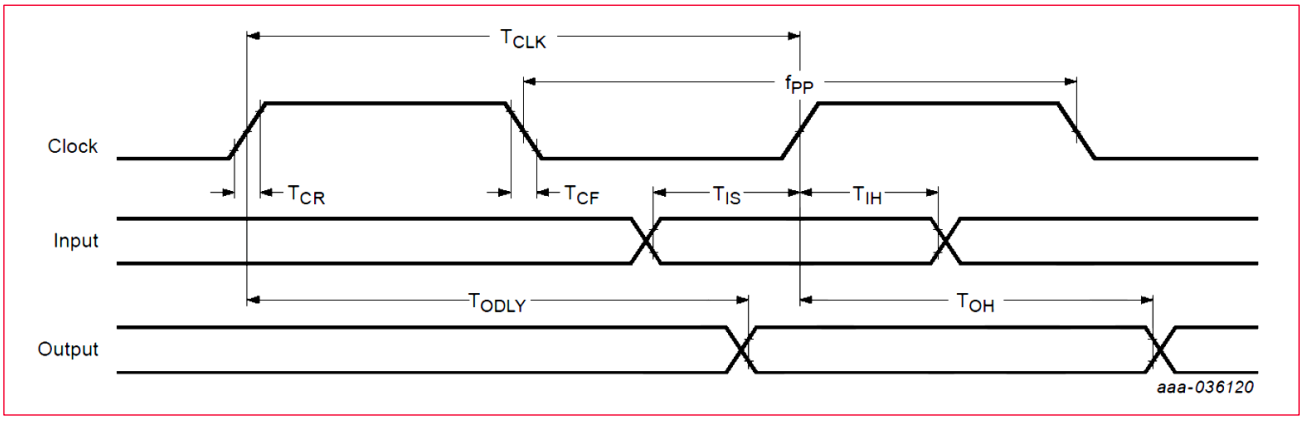


Table 19 describes SDIO protocol timing data for SDR12, SDR25, SDR50 Mode (up to 100 MHz) at 1.8V.

Table 19: SDIO Protocol Timing Parameters - SDR12, SDR25, SDR50 Modes

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	SDR12/25/50	25		100	MHz
T_{IS}	Input setup time	SDR12/25/50	3			MHz
T_{IH}	Input hold time	SDR12/25/50	0.8			ns
T_{CLK}	Clock time	SDR12/25/50	10		40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 2 ns (maximum) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50			0.2*T_{CLK}	ns
T_{ODLY}	Output delay time $C_L \leq 30$ pF	SDR12/25			14	ns
		SDR50			7.5	ns
T_{OH}	Input setup time $C_L \leq 15$ pF	SDR12/25/50	1.5			ns

11.1.4 SDR104 Modes (up to 208 MHz) at 1.8V

Figure 12: SDIO Protocol Timing Diagram - SDR104 Mode shows SDIO protocol timing diagram for SDR104 Mode (up to 208 MHz) at 1.8V.

Figure 12: SDIO Protocol Timing Diagram - SDR104 Mode

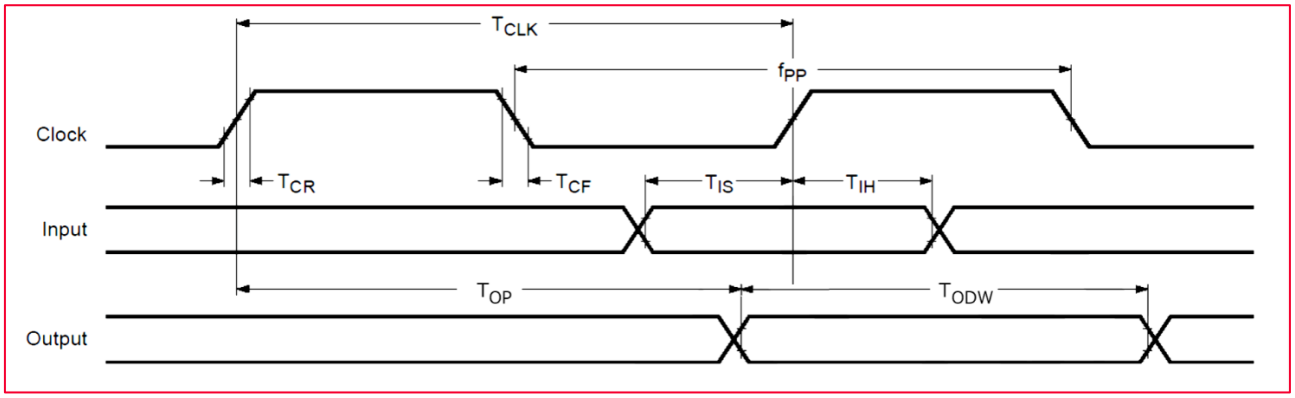


Table 20: SDIO Protocol Timing Parameters – SDR208 Mode describes SDIO protocol timing data for SDR104 Mode (up to 208 MHz) at 1.8V.

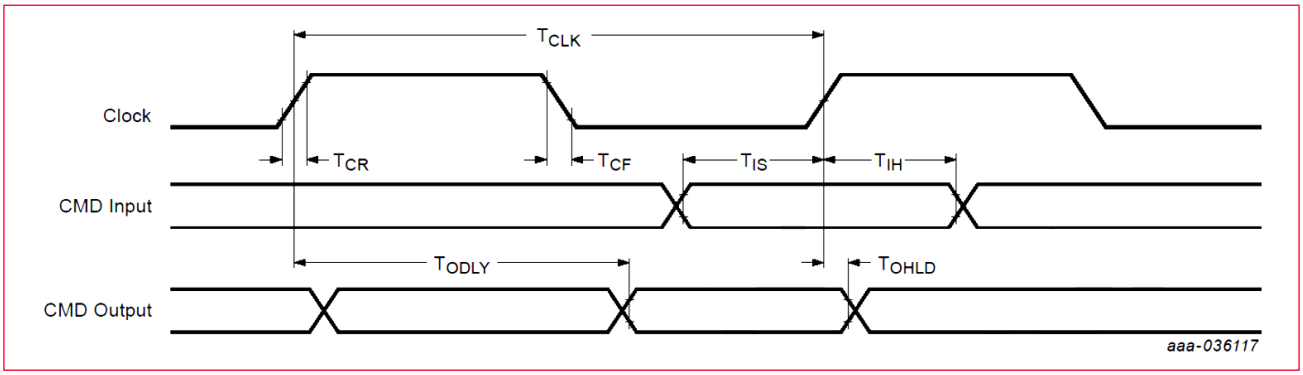
Table 20: SDIO Protocol Timing Parameters – SDR208 Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	SDR104	0		208	MHz
T_{IS}	Input setup time	SDR104	1.4			MHz
T_{IH}	Input hold time	SDR104	0.8			ns
T_{CLK}	Clock time	SDR104	4.8			ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 0.96 ns (maximum) at 208 MHz C_{CARD} = 10 pF	SDR104			0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0		10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88			ns

11.1.5 DDR50 Mode at 50 MHz (1.8V)

Figure 13 shows the SDIO CMD timing diagram for DDR50 mode at 50 MHz.

Figure 13: SDIO CMD Timing Diagram - DDR50 Mode



In DDR50 mode, DAT [3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Figure 14 shows the SDIO data timing diagram for DDR50 Mode.

Figure 14: SDIO Data Timing Diagram - DDR50 Mode

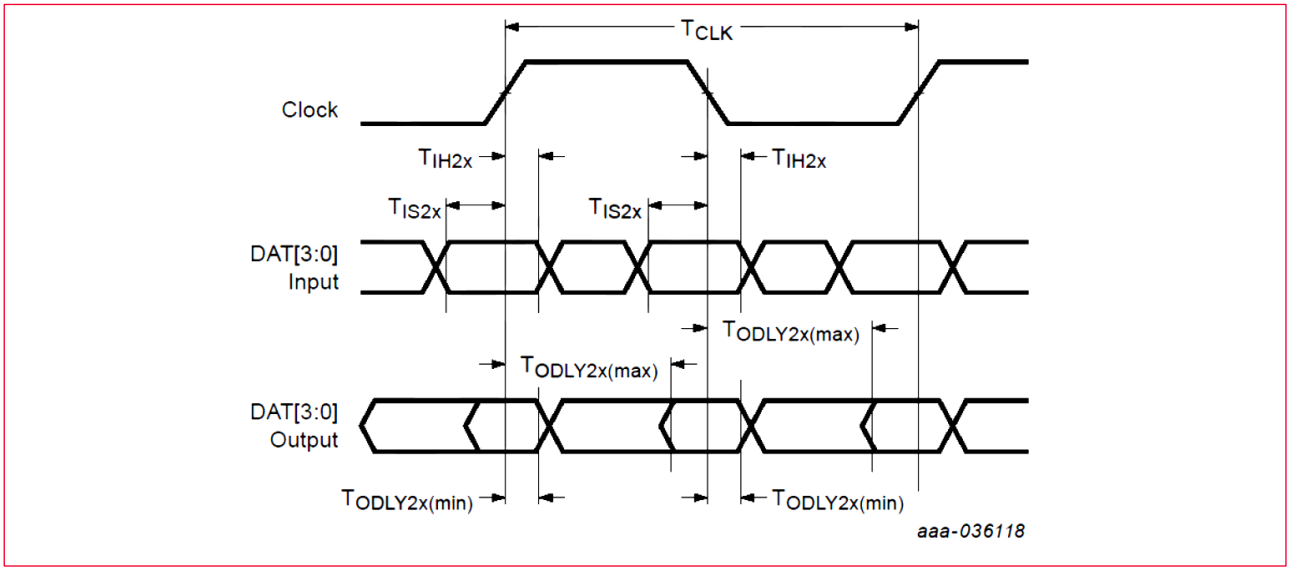


Table 21 describes the parameters for SDIO data timing for DDR50 mode.

Table 21: SDIO Data Timing Parameters - DDR50 Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Clock						
T_{CLK}	Clock time 50 MHz (maximum) between rising edge	DDR50	20			ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns(maximum) at 50 MHz	DDR50			0.2*T_{CLK}	ns
		DDR50	45		55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1card)	DDR50	6			ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1card)	DDR50	0.8			ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode CL ≤ 30 pF (1card)	DDR50			13.7	ns
T_{OHLD}	Output hold time CL ≤ 30 pF (1card)	DDR50	1.5			ns
DAT[3:0] Input (referenced to clock rising and falling edges)						
T_{IS2X}	Input setup time C_{CARD} ≤ 10 pF (1card)	DDR50	3			ns
T_{IH2X}	Input hold time C_{CARD} ≤ 10 pF (1card)	DDR50	0.8			ns
DAT[3:0] Output (referenced to clock rising and falling edges)						
$T_{OLD2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50			7.0	ns
$T_{OLDY2x\ (min)}$	Output hold time C_L ≤ 15 pF (1 card)	DDR50	1.5			ns

11.2 UART Timing (Default Mode)

Default bard rate is 115200 bps. Baud rate is configurable by the host stack.

Figure 15 shows UART timing diagram for default mode.

Figure 15: UART Timing Diagram - Default Mode

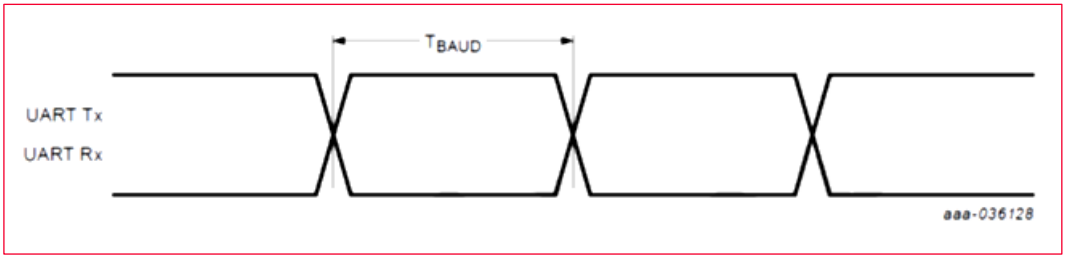


Table 22 describes the UART timing parameters for default mode.

Table 22: UART Timing Parameters - Default Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{BAUD}	Baud rate	38.4 MHz	250			ns

The acceptable deviation from the UART Rx target baud rate is ±3%.

11.3 802.15.4 SPI Timing

Figure 16 shows 802.15.4 SPI timing graph.

Figure 16: 802.15.4 SPI Timing Graph

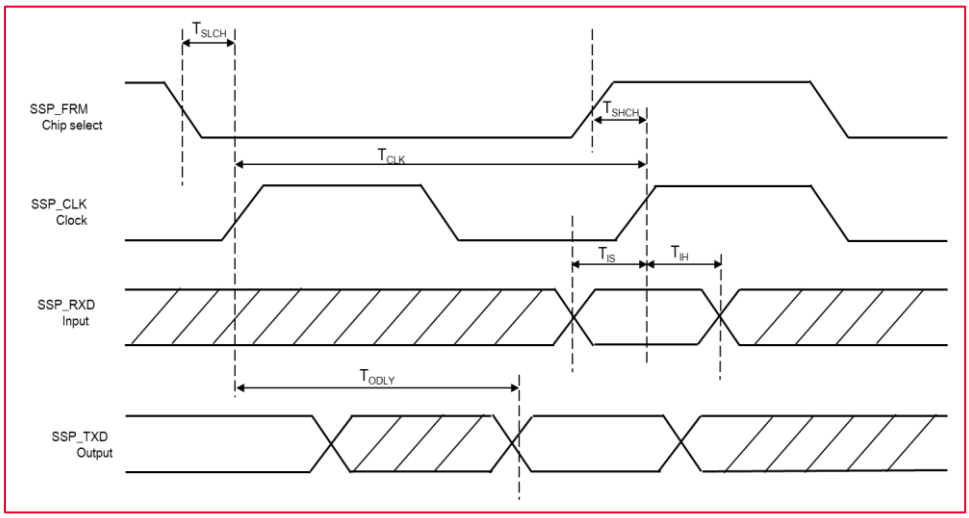


Table 23 describe 802.15.4 SPI timing parameters.

Table 23 : 802.15.4 SPI Timing Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{SLCH}	Chip select setup time		12			ns
T_{SHCH}	Chip select hold time		12			ns
T_{CLK}	Clock period[1]		100			ns
T_{IS}	Input setup time		12			ns
T_{IH}	Input hold time		0			ns
T_{ODLY}	Output delay				12	ns

[1] The maximum SPI clock frequency is limited to 1MHz for Open thread implementations.

11.4 USB Timing

11.4.1 USB Low Speed Timing

Figure 17: USB Low Speed Timing Graph shows the USB waveforms diagram for Low Speed mode.

Figure 17: USB Low Speed Timing Graph

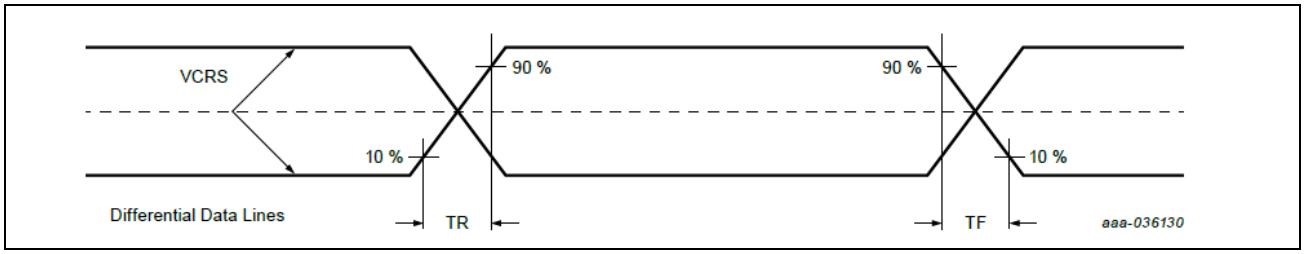


Table 24 : USB Low Speed Timing Parameters describes the USB timing parameter for Low Speed mode.

Table 24 : USB Low Speed Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
BR	Baud rate	--	1.5	--	Mbit/s
BR_PPM	Baud rate tolerance	-15000.0	--	15000.0	ppm
Driver specifications					
V_OH	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	--	3.6	V
V_OL	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground.	0.0	--	0.3	V
V_CRS	Output single crossover voltage See Figure 21 "USB LS/FS data rise and fall time diagram".	1.3	--	2.0	V
T_LR	Data fall time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	--	300.0	ns
T_LF	Data rise time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0	--	300.0	ns
T_LRFM	Rise and fall time matching	80.0	--	125.0	%
T_UDJ1	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-95.0	--	95.0	ns
T_UDJ2	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-150.0	--	150.00	ns
Receiver specifications					
V_IH	Input single ended high	2.0	--	--	V
V_IL	Input single ended low	--	--	0.8	V
V_DI	Differential input sensitivity	0.2	--	--	V

- In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.
- Over full range of values specified in Section 9 "Recommended operating conditions", unless otherwise specified.
- The load is 100Ω differential for these parameters, unless other specified.

11.4.2 USB Full Speed Timing

Figure 18: USB Full Speed Timing Graph shows the USB waveforms diagram for Full Speed mode.

Figure 18: USB Full Speed Timing Graph

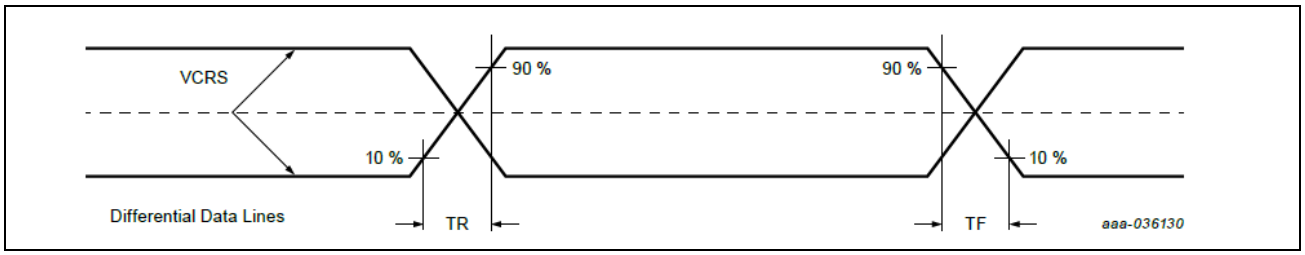


Table 25 : USB Full Speed Timing Parameters describes the USB timing parameter for Full Speed mode.

Table 25 : USB Full Speed Timing Parameters

Symbol	Parameter	Min	Typ	Max	Unit
BR	Baud rate	--	12.0	--	Mbit/s
BR_{PPM}	Baud rate tolerance	-2500.0	--	2500.0	ppm
Driver specifications					
V_{OH}	Output single ended high Defined with 1.425 kΩ pull-up resistor to 3.6V.	2.8	--	3.6	V
V_{OL}	Output single ended low Defined with 1.425 kΩ pull-down resistor to ground.	0.0	--	0.3	V
V_{CRS}	Output single crossover voltage See Figure 21 "USB LS/FS data rise and fall time diagram".	1.3	--	2.0	V
T_{FR}	Output rise time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	--	20.0	ns
T_{FL}	Output fall time • See Figure 21 "USB LS/FS data rise and fall time diagram". • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0	--	20.0	ns
T_{DJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-3.5	--	3.5	ns

T_{DJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-4.0	--	4.0	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition Defined at crossover point of differential data signals.	-2.0	--	5.0	ns
Receiver specifications					
V_{IH}	Input single ended high	2.0	--	--	V
V_{IL}	Input single ended low	--	--	0.8	V
V_{DI}	Differential input sensitivity	0.2	--	--	V
T_{JR1}	Receiver jitter: to next transition Defined at crossover point of differential data signals.	-18.5	--	18.5	ns
T_{JR2}	Receiver jitter: for paired transitions Defined at crossover point of differential data signals.	-9.0	--	9.0	ns

- In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.
- Over full range of values specified in Section 9 "Recommended operating conditions", unless otherwise specified.
- The load is 100Ω differential for these parameters, unless other specified.

11.4.3 USB High Speed Timing

Figure 19: USB High Speed Timing Graph shows the USB Tx eye diagram for High Speed mode.

Figure 19: USB High Speed Timing Graph

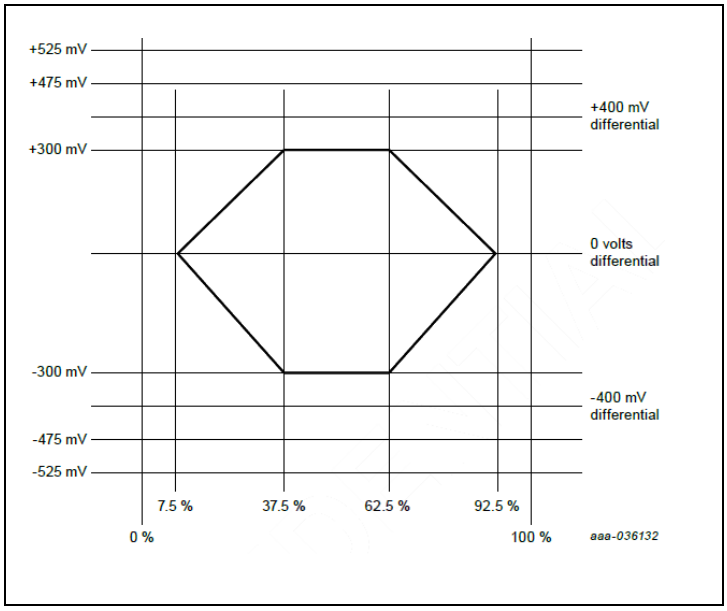


Figure 20: USB High Speed Timing Graph shows the USB Rx eye diagram for High Speed mode.

Figure 20: USB High Speed Timing Graph

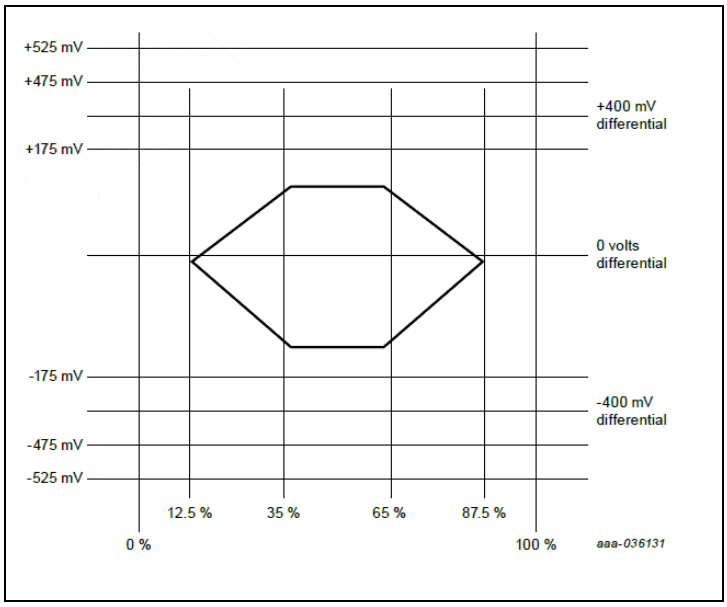


Table 26 : USB High Speed Timing Parameter describes the USB timing parameter for High Speed mode.

Table 26 : USB High Speed Timing Parameter

Symbol	Parameter	Min	Typ	Max	Unit
BR	Baud rate	--	480.0	--	Mbit/s
BR_{PPM}	Baud rate tolerance	-500.0	--	500.0	ppm
Driver specifications					
V_{HSOH}	Data signaling high	360.0	--	440.0	mV
V_{HSOL}	Data signaling low	-10.0	--	10.0	mV
T_{HSR}	Data rise time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	500.0	--	--	ns
T_{HSF}	Data fall time Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-500.0	--	--	ns
--	Source jitter See Figure 22 "USB HS Tx eye diagram pattern template diagram".	--	--	--	--
Receiver specifications					
--	Differential input signaling levels See Figure 22 "USB HS Tx eye diagram pattern template diagram".	--	--	--	--
V_{HSCM}	Input single ended low	-50	--	500.00	mV
--	Receiver jitter tolerance. See Figure 22 "USB HS Tx eye diagram pattern template diagram".	--	--	--	--

- In accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.
- Over full range of values specified in Section 9 "Recommended operating conditions", unless otherwise specified.
- The load is 100Ω differential for these parameters, unless other specified.

12 DC/RF Characteristics

All DC/RF characteristics are defined by the following files:

Table 27: DC/RF Characteristics Files

Names	Country	Country Code	Configuration Files
WLAN Tx power configuration files	USA	US	txpower_US.bin
	Canada	CA	txpower_CA.bin
	Europe	DE	txpower_EU.bin
	Japan	JP	txpower_JP.bin
WLAN OFDMA RU Tx power configuration files	USA	US	rutxpower_US.bin
	Canada	CA	rutxpower_CA.bin
	Europe	DE	rutxpower_EU.bin
	Japan	JP	rutxpower_JP.bin
WLAN Regulatory Limit	-	-	db.txt
Energy Detect	-	-	ed_mac.bin
Bluetooth Power	USA	US	bt_power_config_US_CA_JP.sh
	Canada	CA	bt_power_config_US_CA_JP.sh
	Europe	DE	bt_power_config_EU.sh
	Japan	JP	bt_power_config_US_CA_JP.sh

12.1 DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Figure 21 shows the burst current definition.

Figure 21: Burst Current Definition

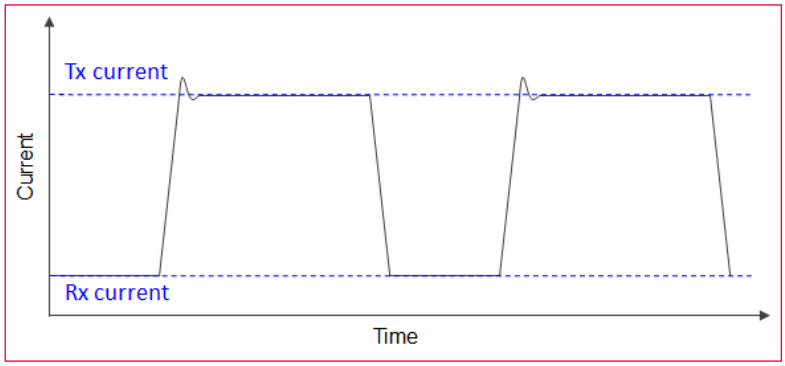


Table 28: Characteristic Values for IEEE 802.11b - 2.4 GHz

Contents	Items
Specification	IEEE 802.11b
Mode	DSSS / CCK
Channel Frequency	2412 to 2472 MHz
Data Rate	1, 2, 5.5, 11 Mbps

12.1.1 High-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 17 dBm at module pad, 11 Mbps mode.

Table 29: High-Rate Condition for IEEE 802.11b - 2.4 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		270	340	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	15	17	19	dBm
Spectrum Mask Margin				
• 1st side lobes (-30dBr)	0			dB
• 2nd side lobes (-50dBr)	0			dB
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm

• 87.5 - 118 MHz (BW =100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-76	dBm
Maximum Input Level (FER ≤ 8%)	-10			dBm
Adjacent Channel Rejection (FER < 8%)	35			dB

12.1.2 Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 17 dBm at module pad, 1 Mbps mode

Table 30: Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		270	340	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	15	17	19	dBm
Spectrum Mask Margin				
• 1st side lobes (-30dBr)	0			dB
• 2nd side lobes (-50dBr)	0			dB
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-80	dBm
Maximum Input Level (FER ≤ 8%)	-4			dBm
Adjacent Channel Rejection (FER< 8%)	35			dB

12.2 DC/RF Characteristics for IEEE 802.11g - 2.4 GHz

Table 31: Characteristic Values for IEEE 802.11g - 2.4 GHz

Contents	Items
Specification	IEEE 802.11g
Mode	OFDM
Channel Frequency	2412 to 2472 MHz
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.2.1 High-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, 54 Mbps mode

Table 32: High-Rate Condition for IEEE 802.11g - 2.4 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		250	320	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM)			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 -74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 8 7.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER < 10%)			-65	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

12.2.2 Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 16 dBm at module pad, 6 Mbps mode

Table 33: Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		260	330	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	14	16	18	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER < 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	16			dB

12.3 DC/RF Characteristics for IEEE 802.11n - 2.4 GHz

Table 34: Characteristic Values for IEEE 802.11n - 2.4 GHz

Contents	Items
Specification	IEEE 802.11n
Mode	OFDM
Channel Frequency	2412 to 2472 MHz
Data Rate	MCS0-MCS7

12.3.1 High-Rate Condition for IEEE 802.11n(HT20) - 2.4 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 14 dBm at module pad, MCS7 mode

Table 35: High-Rate Condition for IEEE 802.11n - 2.4 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		240	310	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	12	14	16	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.3.2 Low-Rate Condition for IEEE 802.11n(HT20) - 2.4 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS0 mode

Table 36: Low-Rate Condition for IEEE 802.11n - 2.4 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		250	320	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
7. Minimum Input Level (PER ≤ 10%)			-82	dBm
8. Maximum Input Level (PER < 10%)	-20			dBm
9. Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.4 DC/RF Characteristics for IEEE802.11ax (HE20) - 2.4GHz

Table 37: Characteristic Values for IEEE802.11ax (HE20) – 2.4GHz

Contents	Items
Specification	IEEE 802.11ax
Mode	OFDM
Channel Frequency	2412 to 2472 MHz
Data Rate	MCS0-MCS9

12.4.1 High-Rate Condition for IEEE802.11ax (HE20) – 2.4GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 13 dBm at module pad, MCS9 mode

Table 38: High-Rate Condition for IEEE802.11ax (HE20) – 2.4GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		230	300	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	11	13	15	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-35	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-52	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-14			dB

12.4.2 Low-Rate Condition for IEEE802.11ax (HE20) – 2.4GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS0 mode

Table 39: Low-Rate Condition for IEEE802.11ax (HE20) – 2.4GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		250	320	mA
• Rx mode Current 3.3V		60	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	16			dB

12.6 DC/RF Characteristics for IEEE 802.11a - 5 GHz

Table 40: Characteristic Values for IEEE 802.11a - 5 GHz

Contents	Items
Specification	IEEE 802.11a
Mode	OFDM
Channel Frequency	5180 to 5240 MHz, 5260 to 5320 MHz, 5500 to 5720 MHz, 5745 to 5825 MHz
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.6.1 High-Rate Condition for IEEE 802.11a - 5 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, 54 Mbps mode

Table 41: High-Rate Condition for IEEE 802.11a - 5 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		410	560	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-65	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.6.2 Low-Rate Condition for IEEE 802.11a - 5 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 16 dBm at module pad, 6 Mbps mode

Table 42: Low-Rate Condition for IEEE 802.11a - 5 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		420	570	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	14	16	18	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.7 DC/RF Characteristics for IEEE 802.11n (HT20) - 5 GHz

Table 43: Characteristic Values for IEEE 802.11n (HT20) - 5 GHz

Contents	Items
Specification	IEEE 802.11n
Mode	OFDM
Channel Frequency	5180 to 5240 MHz, 5260 to 5320 MHz, 5500 to 5720 MHz, 5745 to 5825 MHz
Data Rate	MCS0 - MCS7

12.7.1 High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 14 dBm at module pad, MCS7 mode

Table 44: High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Item	Contents			
DC Characteristics	Minimum	Typical	Maximum	Unit
DC Current				
• Tx mode Current 3.3V		390	540	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	12	14	16	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.7.2 Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS0 mode

Table 45: Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		400	550	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.8 DC/RF Characteristics for IEEE 802.11ac (VHT20) - 5 GHz

Table 46: Characteristic Values for IEEE 802.11ac (VHT20) - 5 GHz

Contents	Items
Specification	IEEE 802.11ac
Mode	OFDM
Channel Frequency	5180 to 5240 MHz, 5260 to 5320 MHz, 5500 to 5720 MHz, 5745 to 5825 MHz
Data Rate	MCS0 - MCS8

12.8.1 High-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 13 dBm at module pad, MCS8 mode

Table 47: High-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		380	530	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	11	13	15	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-30	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-59	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-7			dB

12.8.2 Low-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS0 mode

Table 48: Low-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		400	550	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-30	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-7			dB

12.9 DC/RF Characteristics for IEEE802.11ax (HE20) - 5GHz

Table 49: Characteristics Values for IEEE802.11ax (HE20) - 5GHz

Contents	Items
Specification	IEEE 802.11ax
Mode	OFDM
Channel Frequency	5180 to 5240 MHz, 5260 to 5320 MHz, 5500 to 5720 MHz, 5745 to 5825 MHz
Data Rate	MCS0 – MCS9

12.9.1 High-Rate Condition for IEEE802.11ax (HE20) – 5GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 13 dBm at module pad, MCS9 mode

Table 50: High-Rate Condition for IEEE802.11ax (HE20) - 5GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		380	530	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	11	13	15	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-35	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-52	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-7			dB

12.9.2 Low-Rate Condition for IEEE802.11ax (HE20) – 5GHz

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS0 mode

Table 51: Low-Rate Condition for IEEE802.11ax (HE20) – 5GHz

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		400	550	mA
• Rx mode Current 3.3V		75	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (Measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-7			dB

12.10 DC/RF Characteristics for Bluetooth Low Energy

Table 52: Characteristics Values for Bluetooth Low Energy

Contents	Items
Bluetooth Specification (power class)	Version 5.3 (Class 1.5)
Channel Frequency (spacing)	2402 to 2480 MHz (2 MHz)
Number of RF Channel	40

12.10.1 1 Mbps PHY Condition

Conditions: 25 °C, AVDD33 = 3.3V, VIO = 1.8V

Table 53: 1 Mbps PHY Condition

Item	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode Current 3.3V		55	80	mA
• Rx mode Current 3.3V		20	40	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output power	7	10	13	dBm
In-band emission				
• f_{TX} +/-2 MHz			-20	dBm
• f_{TX} +/-[3+n] MHz; n = 0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	225		275	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Stable Modulation Characteristics				
• $\Delta f1_{avg}$	247.5		252.5	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier Frequency Offset and Drift				
• Frequency offset (f_n); n = 0,1, 2, 3…k	-150		150	kHz
• Frequency drift ($\lvert f_0-f_n \rvert$); n = 2, 3, 4…k			50	kHz
• Drift Rate				
• $\lvert f_1 - f_0 \rvert$			23	kHz
• $\lvert f_n-f_{n-5} \rvert$; n = 6, 7, 8... k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm

Item	Contents			
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-97	-70	dBm
Maximum input signal level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

12.10.2 2 Mbps PHY Condition

Conditions: 25°C, AVDD33 = 3.3V, VIO = 1.8V

Table 54: 2 Mbps PHY Condition

Item	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode Current 3.3V		55	80	mA
• Rx mode Current 3.3V		20	40	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output power	7	10	13	dBm
In-band emission				
• f_{TX} +/-4 MHz			-20	dBm
• f_{TX}+/-5 MHz			-20	dBm
• f_{TX}+/-[6+n] MHz; n=0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	450		550	kHz
• $\Delta f2_{max}$ (at 99.9%)	370			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Stable Modulation Characteristics				
• $\Delta f1_{avg}$	495		505	kHz
• $\Delta f2_{max}$ (at 99.9%)	370			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier Frequency Offset and Drift				
• Frequency offset (f_n); n = 0, 1, 2, 3…k	-150		150	kHz
• Frequency drift ($\|f_0-f_n\|$); n = 2, 3, 4…k			50	kHz
• Drift Rate				
• |f1-f0|			23	kHz
• fn-fn-5|; n = 6, 7, 8…k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm

Item	Contents			
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-97	-70	dBm
Maximum input signal level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

12.11 DC/RF Characteristics for 802.15.4

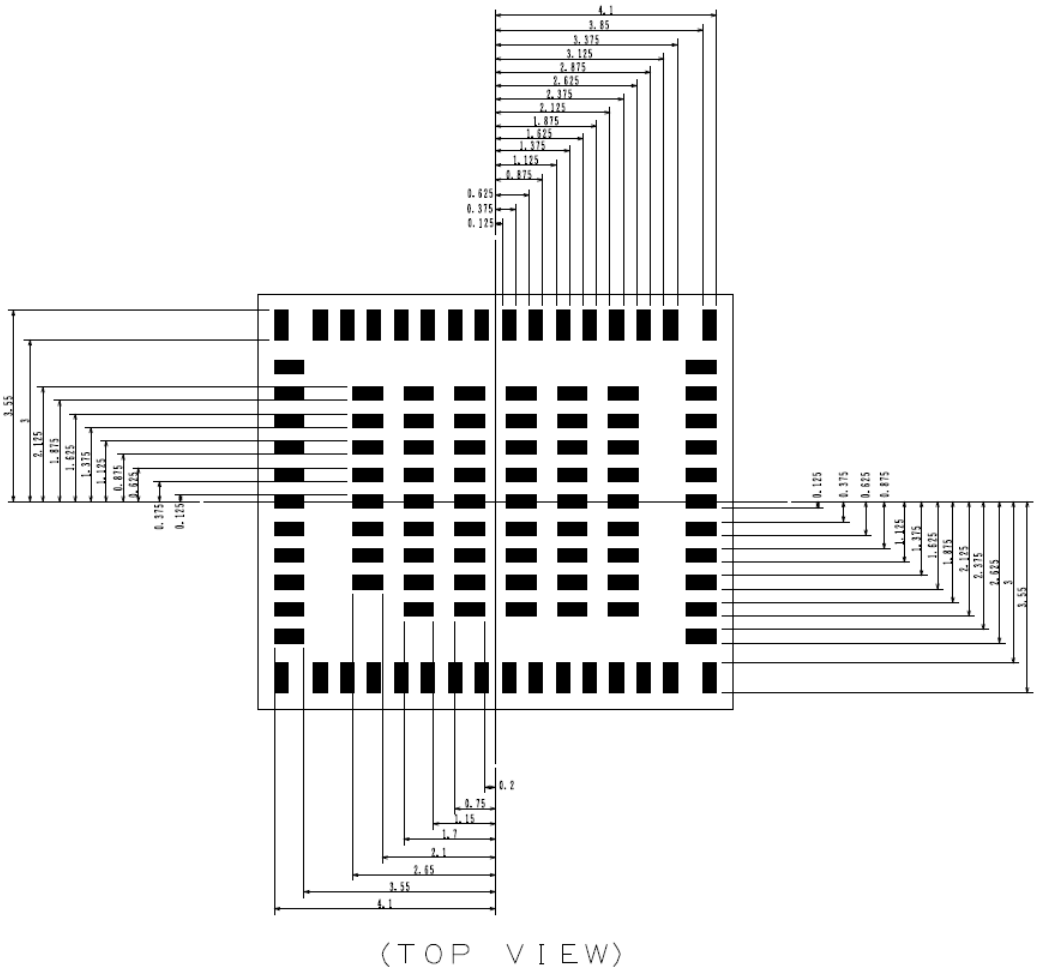
Table 55: 802.15.4

Item	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC Current				
• Tx mode Current 3.3V		55	80	mA
• Rx mode Current 3.3V		20	40	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	7	10	13	dBm
Spectrum Mask Margin				
Transmit power spectral density (PSD) mask	-	-	-30	dB
Modulation Accuracy	-	-	35	%
Frequency Tolerance	-40		40	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW =100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 1%)	-	-	-85	dBm
Maximum Input Level (FER ≤ 1%)	-20	-	-	dBm
Adjacent Channel Rejection (FER < 1%)	0	-	-	dB

13 Land Pattern

Figure 22 shows land pattern of Type 2LL.

Figure 22: Land Pattern (Unit: mm)



To avoid the short-circuit between the side shielding and a solder on the module land after the reflow, please locate the module land at 0.2 mm away from module outline as above figure.

14 Tape and Reel Packing

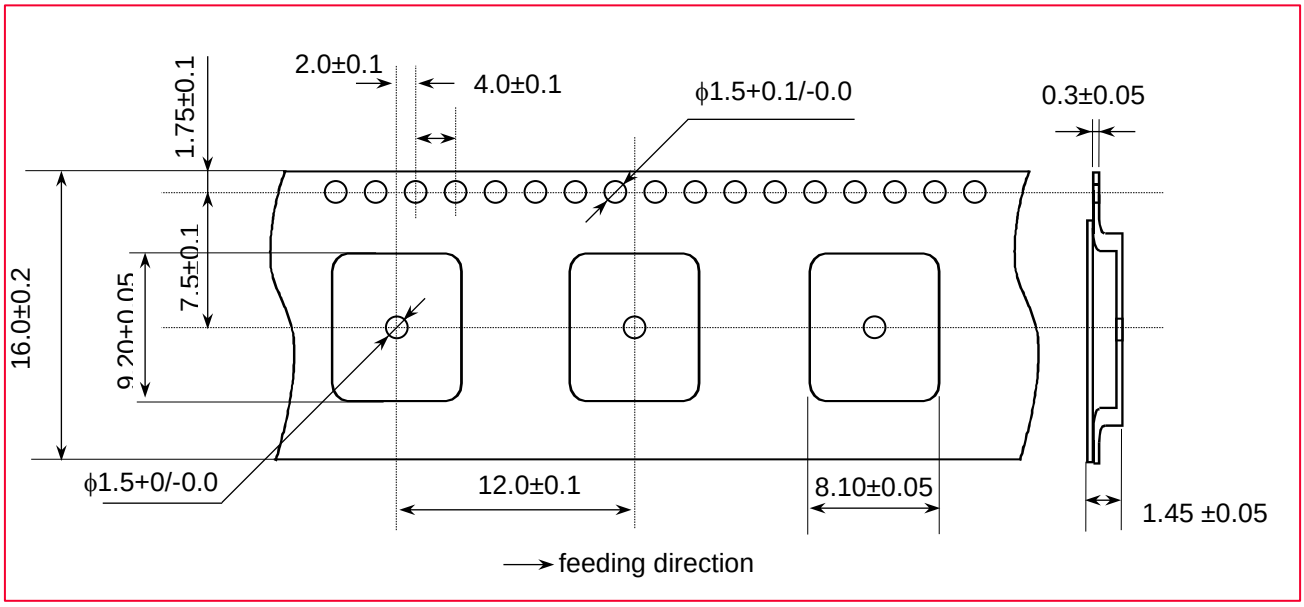
This section contains the following topics:

- Dimensions of Tape (Plastic tape)
- Dimensions of Reel
- Taping Diagrams
- Leader and tail tape
- Packaging

14.1 Dimensions of Tape (Plastic Tape)

Figure 23 is a graphical representation of the tape dimension (plastic tape)[2].

Figure 23: Dimensions of Tape (Plastic Tape)

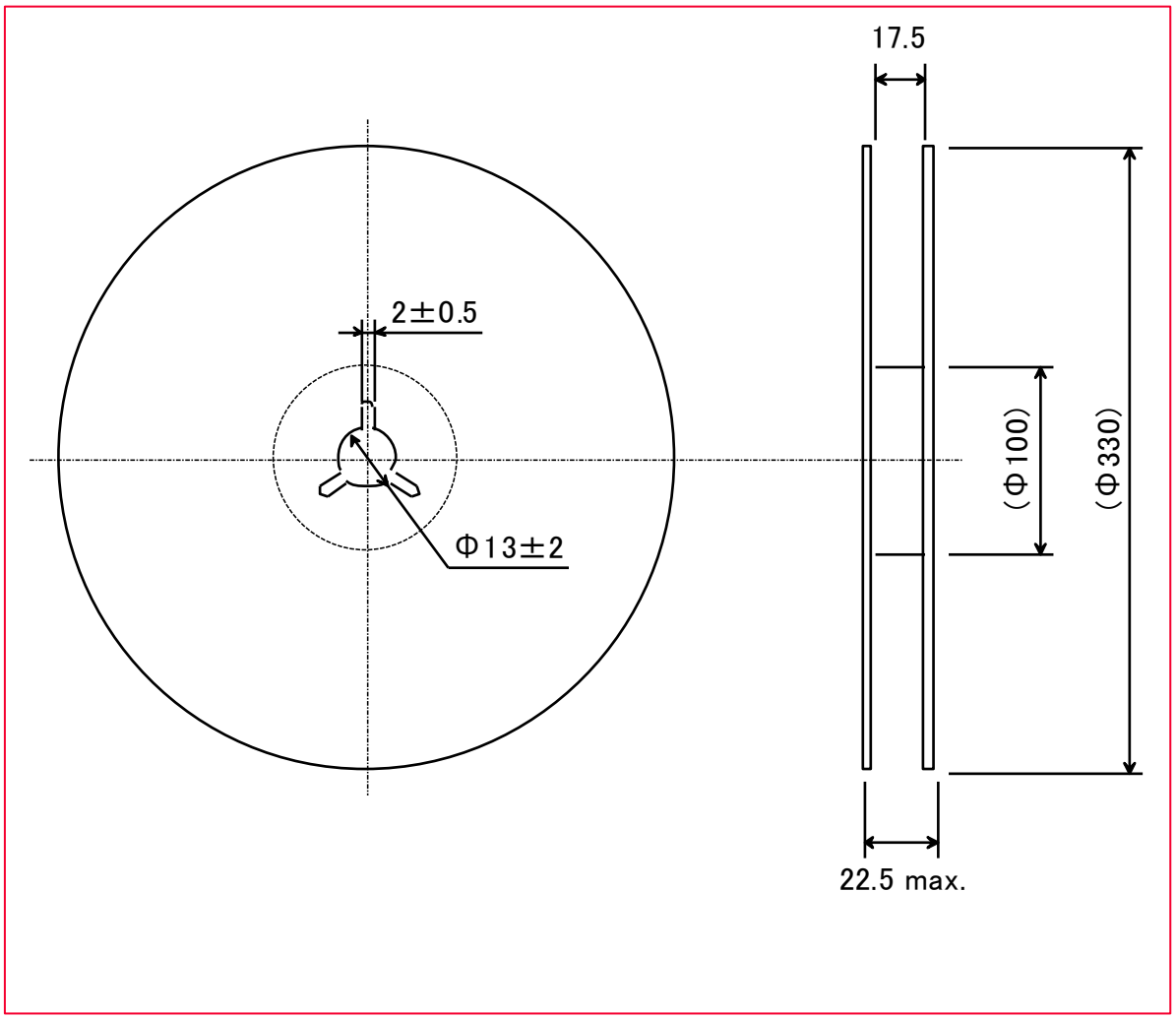


[2] Cumulative tolerance of maximum 40 +/- 0.15 mm for every 10 pitches.

14.2 Dimensions of Reel

Figure 24 shows the reel dimensions.

Figure 24: Dimensions of Reel (Unit: mm)



14.3 Taping Diagrams

Figure 25 shows the taping diagrams.

Figure 25: Taping Diagrams

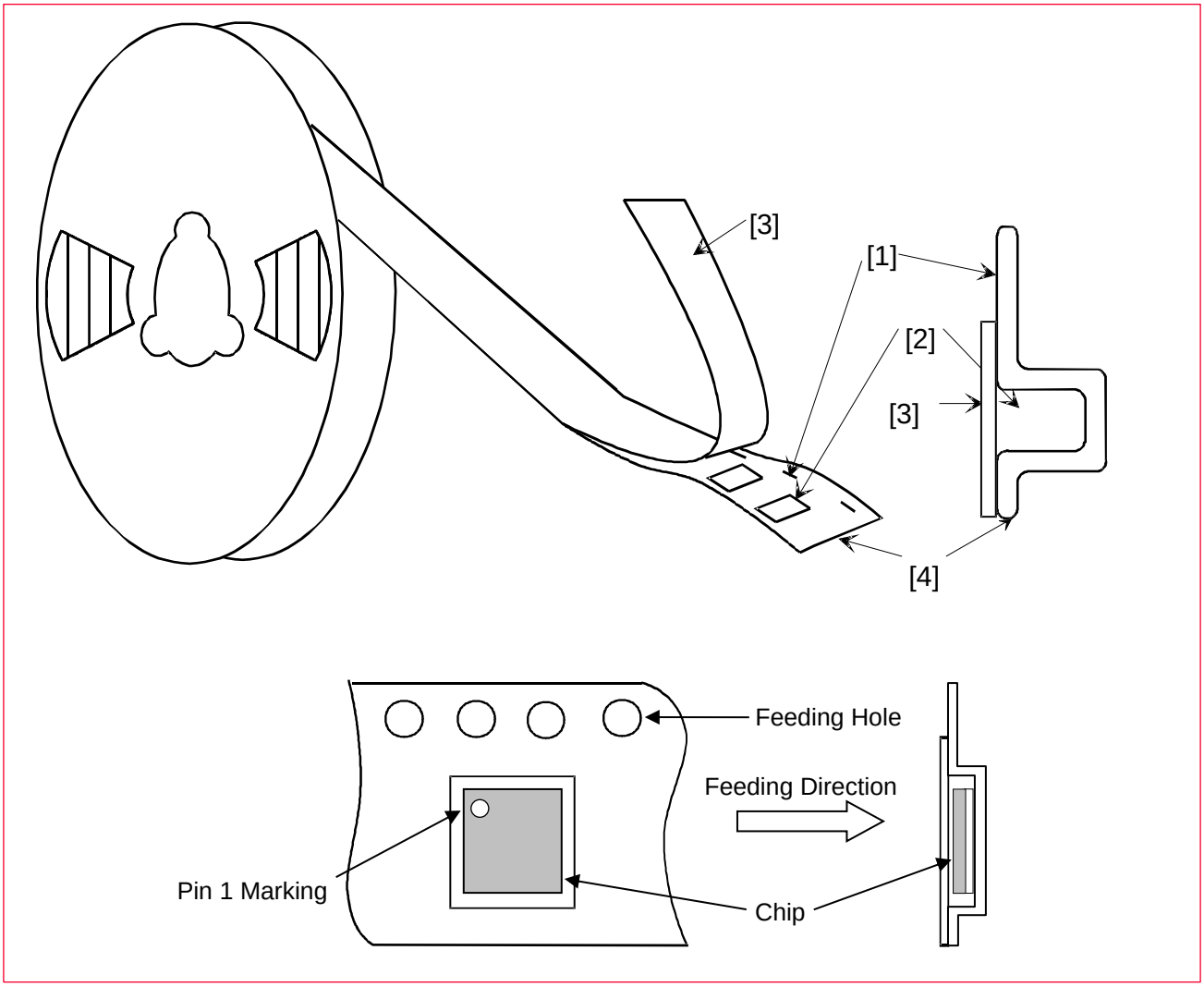


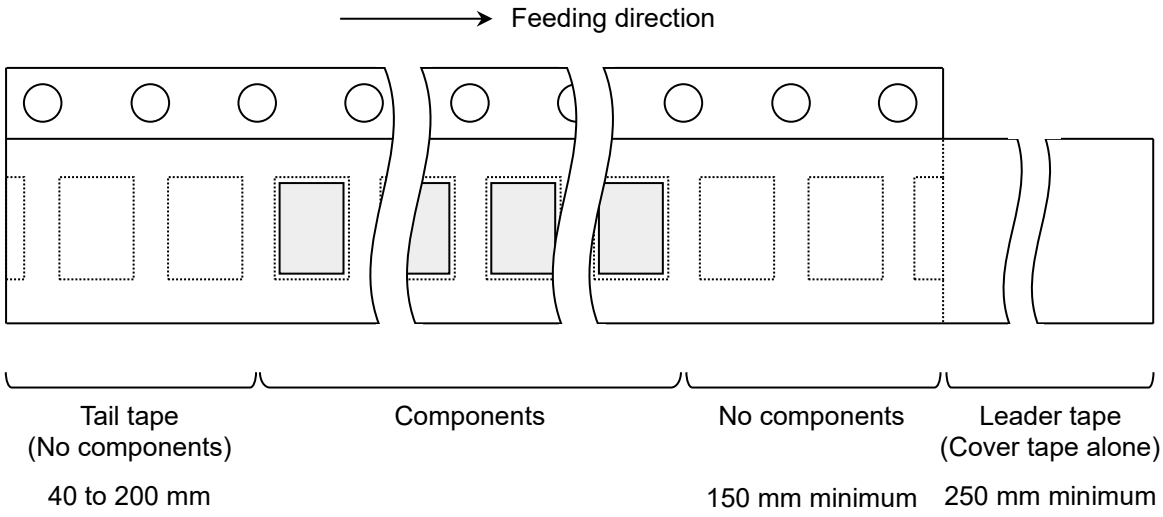
Table 56: Taping Specifications

Mark	Description
1	Feeding Hole. As specified in Dimensions of Tape (Plastic Tape).
2	Hole for chip. As specified in Dimensions of Tape (Plastic Tape).
3	Cover tape. 62 µm in thickness.
4	Base tape. As specified in Dimensions of Tape (Plastic Tape).

14.4 Leader and Tail Tape

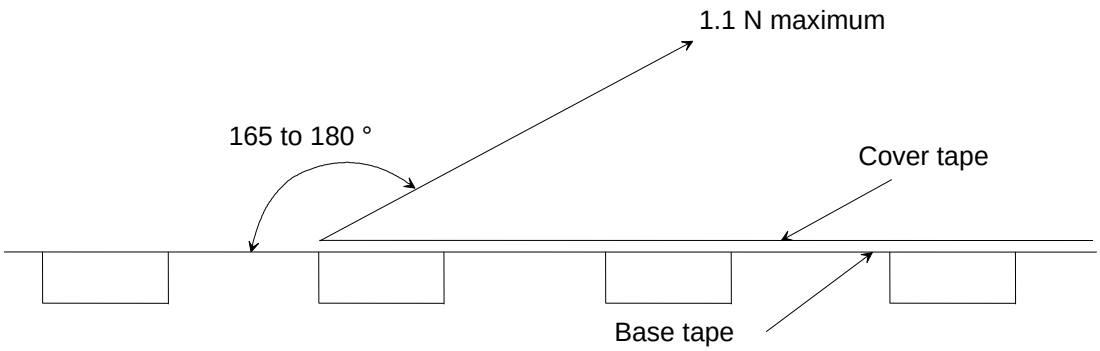
The leader and tail tape are shown in **Figure 26**

Figure 26: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape: 5 N minimum.
- Packaging unit: 1000 pcs./ reel
- Material
  - Base tape: Plastic
  - Real: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling off force: 1.1 N maximum. in the direction of peeling as shown in **Figure 27**

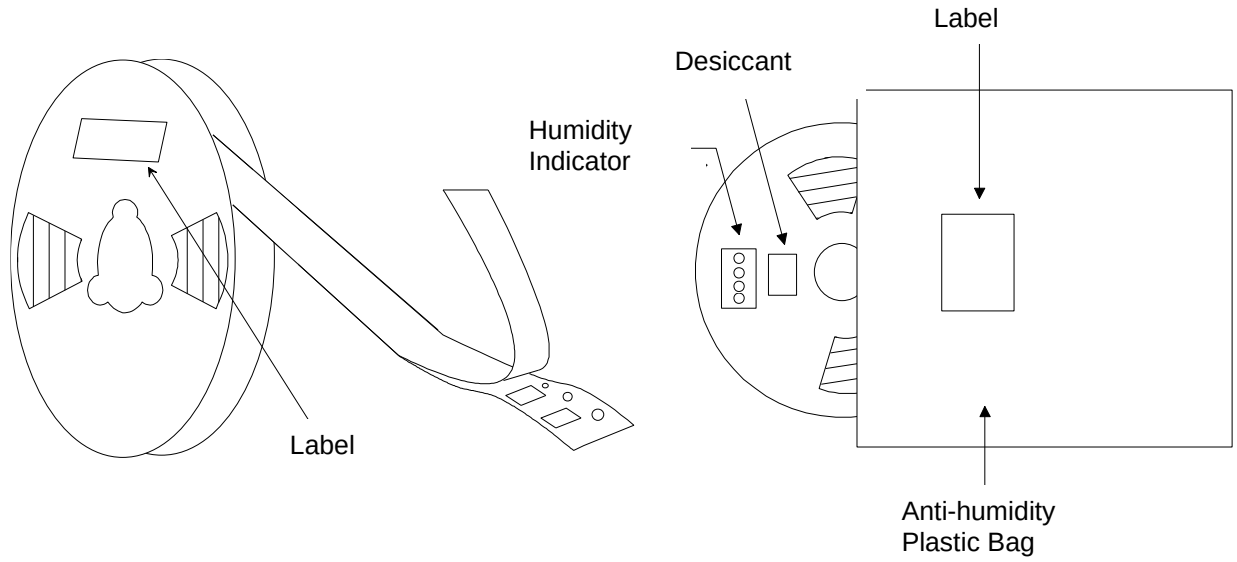
Figure 27: Peeling Force



14.5 Packaging (Humidity Proof Packing)

The packaging is shown in **Figure 28**

Figure 28: Humidity Proof Packing



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

15 Notice

15.1 Storage Conditions

- Please use this product within 6 months after receipt.
  - The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (Packing materials, in particular, may be deformed at the temperature over 40 °C).
  - The product left more than 6 months after reception; it needs to be confirmed the solderability before used.
  - The product shall be stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
  - Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object, and dropping the product, shall not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)
  - After the packing opened, the product shall be stored at <30 °C / <60 %RH and the product shall be used within 168 hours.
  - When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products shall be baked on the heat-resistant tray because the materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

15.2 Handling Conditions

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

15.3 Standard PCB Design (Land Pattern and Dimensions)

- All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.
- The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

15.4 Notice for Chip Placer

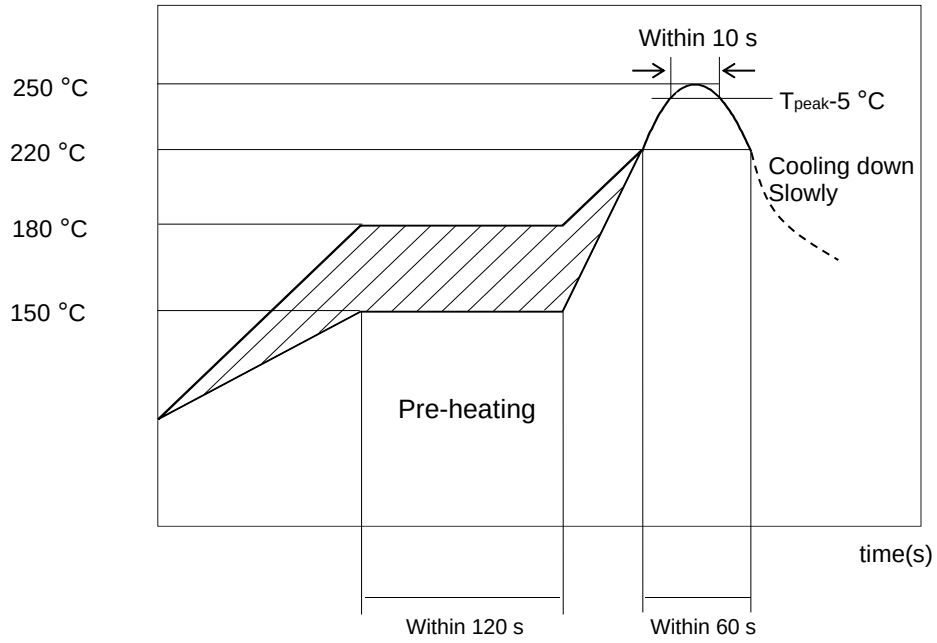
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

15.5 Soldering Conditions

The recommendation conditions of soldering are shown in **Figure 29**.

Soldering must be carried out by the above-mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Figure 29: Reflow soldering standard conditions (Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt. % or less.

15.6 Cleaning

This product is moisture sensitive; therefore, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

15.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_X, NO_X etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

16 Precondition to Use Our Products

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

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Revision History

Revision Code	Date	Changed Item	Comments
1 (A)	2024.11.1	First Issue	Initial draft version (Base IC datasheet revision : 6)
2	2025.02.4	Official release 2. Key Features 3. Ordering Information 5.1 Radio Certification 5.3 Bluetooth Qualification 6. Dimensions, Markings.. 7.2 Pin Descriptions 7.4 Pin States 8 Absolute Maximum Rating 9.1 Operating Conditions 9.2 Digital I/O Requirements 9.3 Package Thermal Conditions 10.2 Power-Off Sequence 10.3 Host Reset Sequence 11.1.1 Default Speed Mode 11.1.2 High Speed Mode 11.1.3 SDR12/25/50 Modes 12. DC/RF Characteristics	• Added Security, Weight and Total FIT • Added M.2 EVB Part number • Added IDs • Added DN • Added warning message • Changed UART1 to UART • Updated PDn, CONFIG_HOST[0/1], USB_DP/DM • Added information • Changed Storage temperature • Defined Tj, Peak current • Update VOH, VOL • Added RΨjt • Removed information • Remove t_{INT}, Added information • Updated Table 17 • Updated Table 18 • Updated Table 19 • Updated Output power • Defined Current consumption • Corrected typo of MCS in HE20 • Corrected typo of spectrum mask (Base IC datasheet revision : 7)