Datasheet

Type 2DS Wi-Fi™ Module

NXP 88W8801 Chipset for 802.11b/g/n Datasheet - Rev. 11

- Design Name: Type 2DS
- P/N: LBWA0ZZ2DS-688

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About This Document

Type 2DS is a small and high-performance module (integrated PCB antenna) based on NXP 88W8801 chipset, supporting IEEE 802.11b/g/n. This datasheet describes Type 2DS module in detail.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product. In particular, RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	**Warning Note** Indicates very important note. Users are strongly recommended to review.
	**Info Note** Intended for informational purposes. Users should review.
	**Menu Reference** Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery 
	**External Hyperlink** This symbol indicates a hyperlink to an external document or website. **Example**: Embedded Artists AB  Click on the text to open the external link.
	**Internal Hyperlink** This symbol indicates a hyperlink within the document. **Example**: Scope  Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This specification characterizes the IEEE 802.11b/g/n module.

2 Key Features

- NXP 88W8801 inside
- Supports IEEE 802.11b/g/n specification: Single band 2.4 GHz
- SISO with 20 MHz channels
- Up to MCS 7 data rates (72.2 Mbps)
- WLAN Interface: SDIO 2.0 and USB 2.0
- Dimensions: 25.0 x 14.0 x 2.32 mm
- Weight: 1.07 mg
- MSL: 3
- Surface-mount type
- RoHS compliant
- Total Fit: 29

Optional WLAN-USB interface may not be supported.
Refer to Type 2DS webpage or check 2DS Community Forum page.

3 Ordering Information

Table 2: Ordering Information

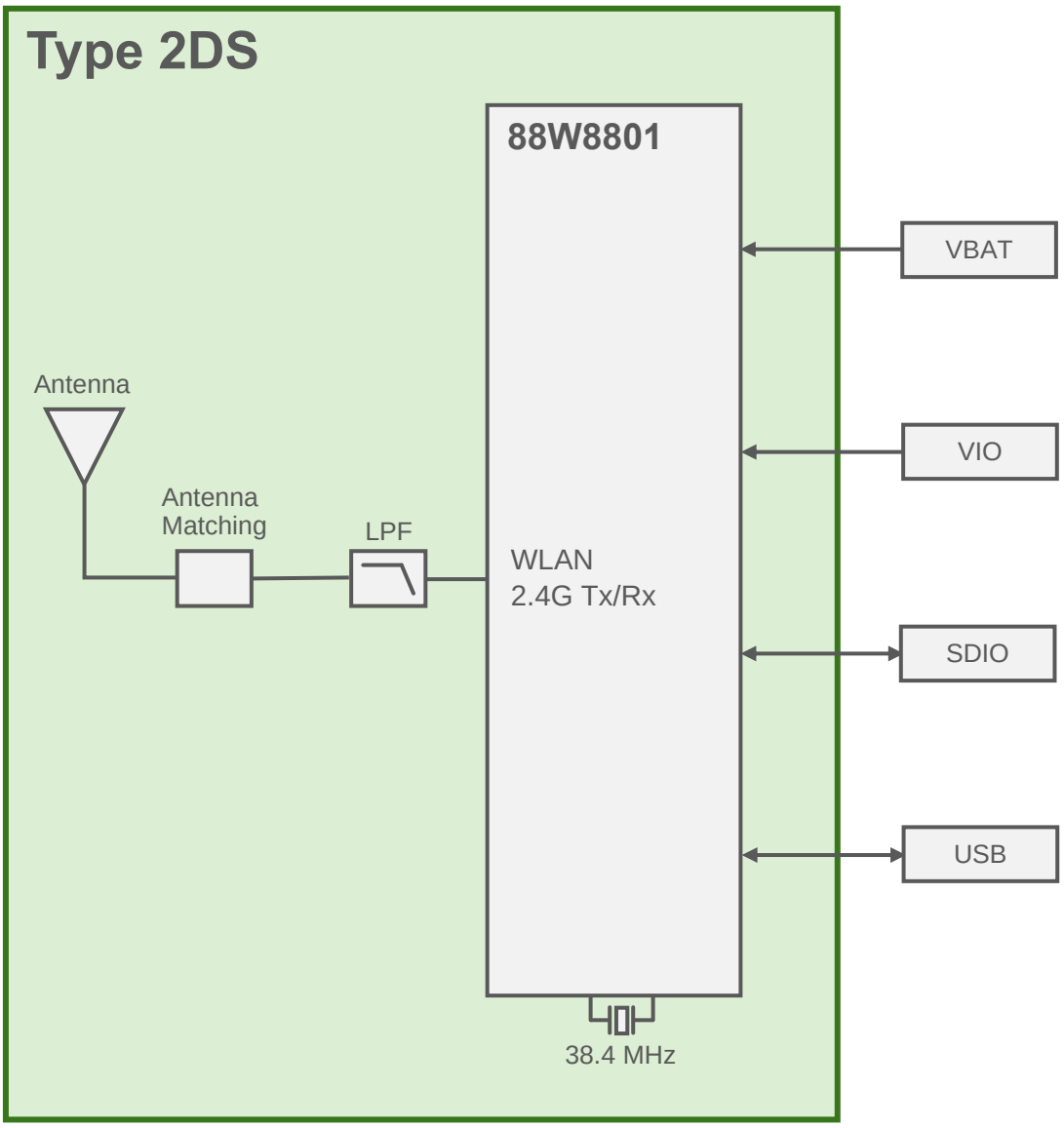
Ordering Part Number	Description
LBWA0ZZ2DS-688	Module order
LBWA0ZZ2DS-SMP	Sample module order (If module samples are not available through distribution, contact Murata referencing this part number)
EAR00386	Embedded Artists Type 2DS M.2 EVB (default EVB available through distribution)

"LBWA0ZZ2DS" is used in certification test report.

4 Block Diagram

The Type 2DS block diagram is presented in **Figure 1**.

Figure 1: Block Diagram



Optional WLAN-USB interface may not be supported.

Refer to Type 2DS webpage or check 2DS Community Forum page.

5 Certification Information

This section has information about radio certification.

5.1 Radio Certification

All regulatory testing is on-going

Transmit output power setting is defined by "txpower_XX.bin" (XX is country code). The transmit power files are hosted at Murata GitHub for Linux and FreeRTOS. **Table 3** shows the transmit power file required for each region.

Table 3: Transmit Power Limit Files

Country	ID	Country Code	Tx Power Limit File	
			Linux	FreeRTOS
USA (FCC)	VPYLBWA0ZZ2DS	US	txpower_US.bin	wlan_txpwrlimit_cfg_murata_2DS_US.h
Canada (IC)	772C-LBWA0ZZ2DS	CA	txpower_CA.bin	wlan_txpwrlimit_cfg_murata_2DS_CA.h
Europe	EN300328/301893, EN300440 conducted test report is prepared.	DE	txpower_EU.bin	wlan_txpwrlimit_cfg_murata_2DS_EU.h
Japan	Japanese type certification is prepared. ® 001-P01579	JP	txpower_JP.bin	wlan_txpwrlimit_cfg_murata_2DS_JP.h

Each country code is defined by Murata's db.txt file. Please ask your contact person from Murata.

6 Dimensions, Marking and Terminal Configurations

This section provides information about dimensions, markings, and terminal configuration for Type 2DS.

Figure 2: Dimensions, Marking and Terminal Configurations

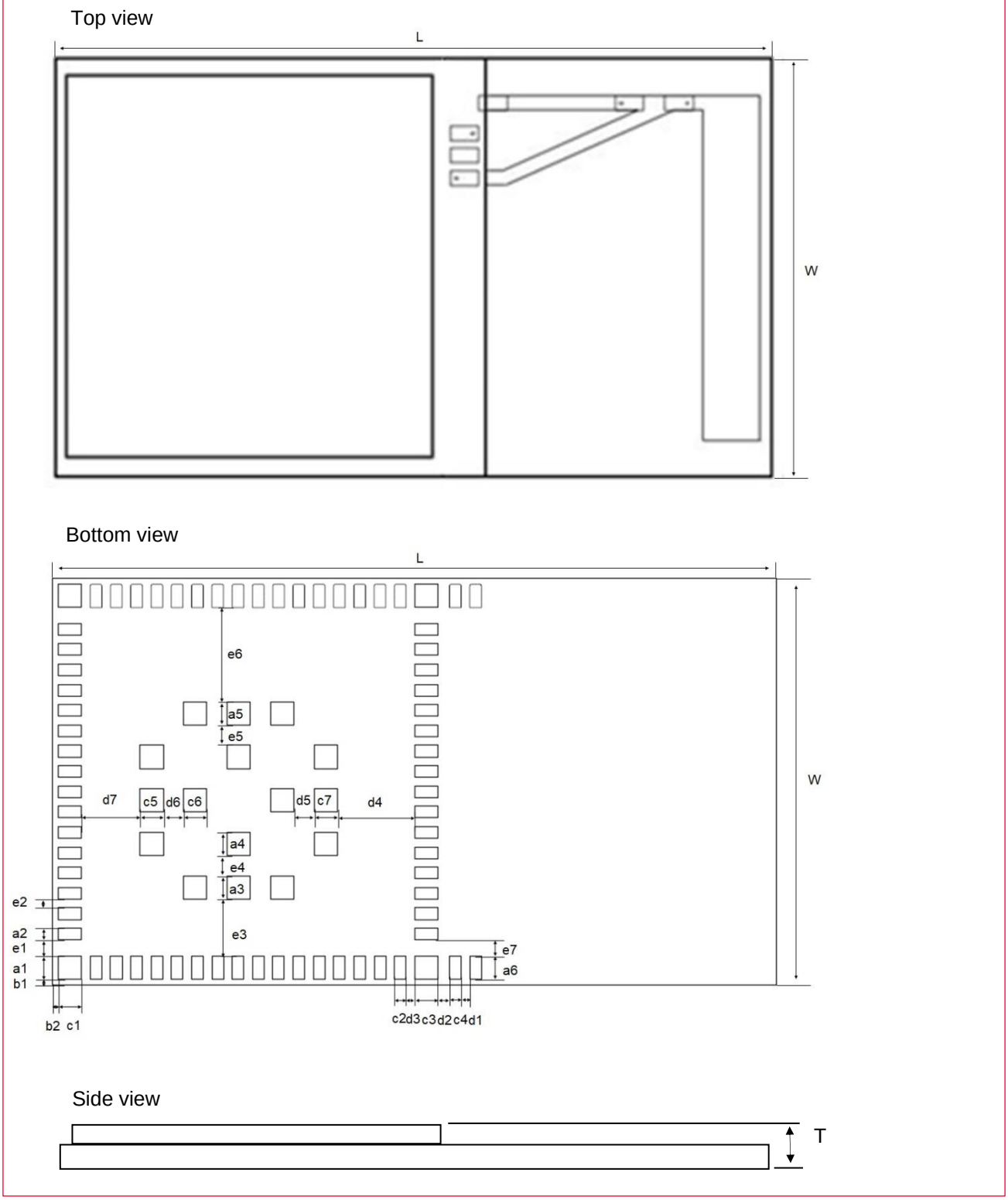


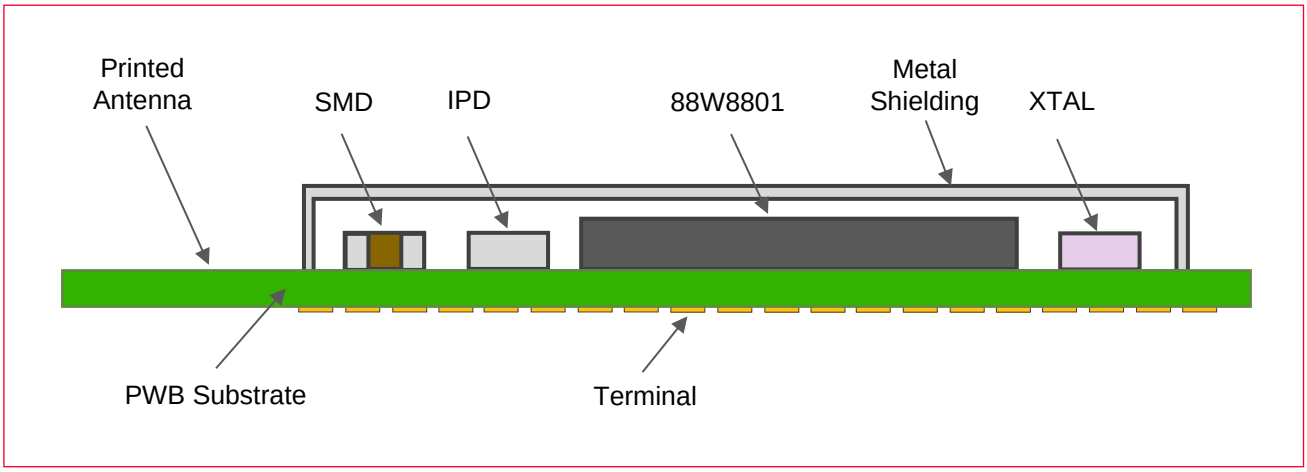
Table 4: Dimensions

Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)
L	25.0 ± 0.2	W	14.0 ± 0.2	T	2.32 maximum	a1	0.8 ± 0.1
a2	0.4 ± 0.1	a3	0.8 ± 0.2	a4	0.8 ± 0.1	a5	0.8 ± 0.1
a6	0.8 ± 0.1	b1	0.2± 0.2	b2	0.2 ± 0.2	c1	0.8 ± 0.1
c2	0.4 ± 0.1	c3	0.8 ± 0.1	c4	0.4 ± 0.1	c5	0.8 ± 0.1
c6	0.8 ± 0.1	c7	0.8 ± 0.1	d1	0.3 ± 0.1	d2	0.4 ± 0.1
d3	0.3 ± 0.1	d4	2.675 ± 0.1	d5	0.7 ± 0.1	d6	0.7 ± 0.1
d7	2.025 ± 0.1	e1	0.55 ± 0.1	e2	0.3 ± 0.1	e3	1.95 ± 0.1
e4	0.7 ± 0.1	e5	0.7 ± 0.1	e6	3.25 ± 0.1	e7	0.55 ± 0.1

6.1 Structure

The structure for Type 2DS module is shown in **Figure 3.**

Figure 3: Structure



6.2 Marking

The marking for Type 2DS module is shown in **Figure 4.**

Figure 4: Markings

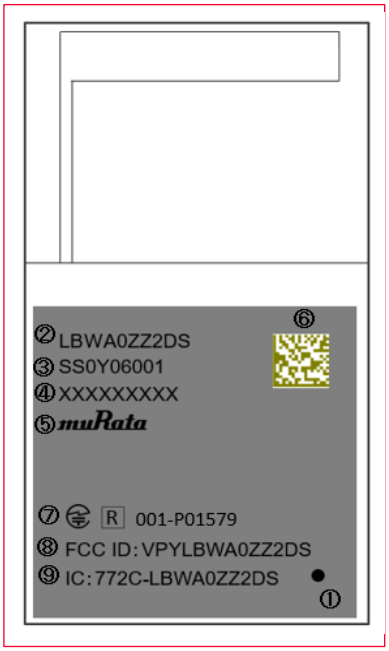
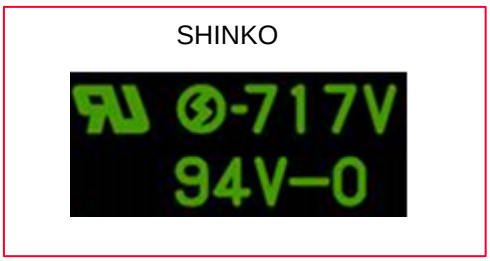


Table 5: Markings

Marking	Meaning
1	Pin 1 Marking
2	Module Type
3	Inspection Number
4	Serial Number
5	Murata Logo
6	2D code
7	TELEC Mark/ID
8	FCC ID
9	IC ID

UL mark and factory code of one of below two PCB factories shall be displayed on the PCB.

Figure 5: UL Marks and Factory Codes



Revocation of UL V-0 Certification. UL V-0 has been revoked but UL certification of boards with UL V-0 notation on the market is valid. Contact SHINKO on any inquiries on UL V-0 Certification.

<Contact>

Shinkoh Manufacturing Co., Ltd.

Sales department

E-MAIL : Sales_Shinko@smm-g.com

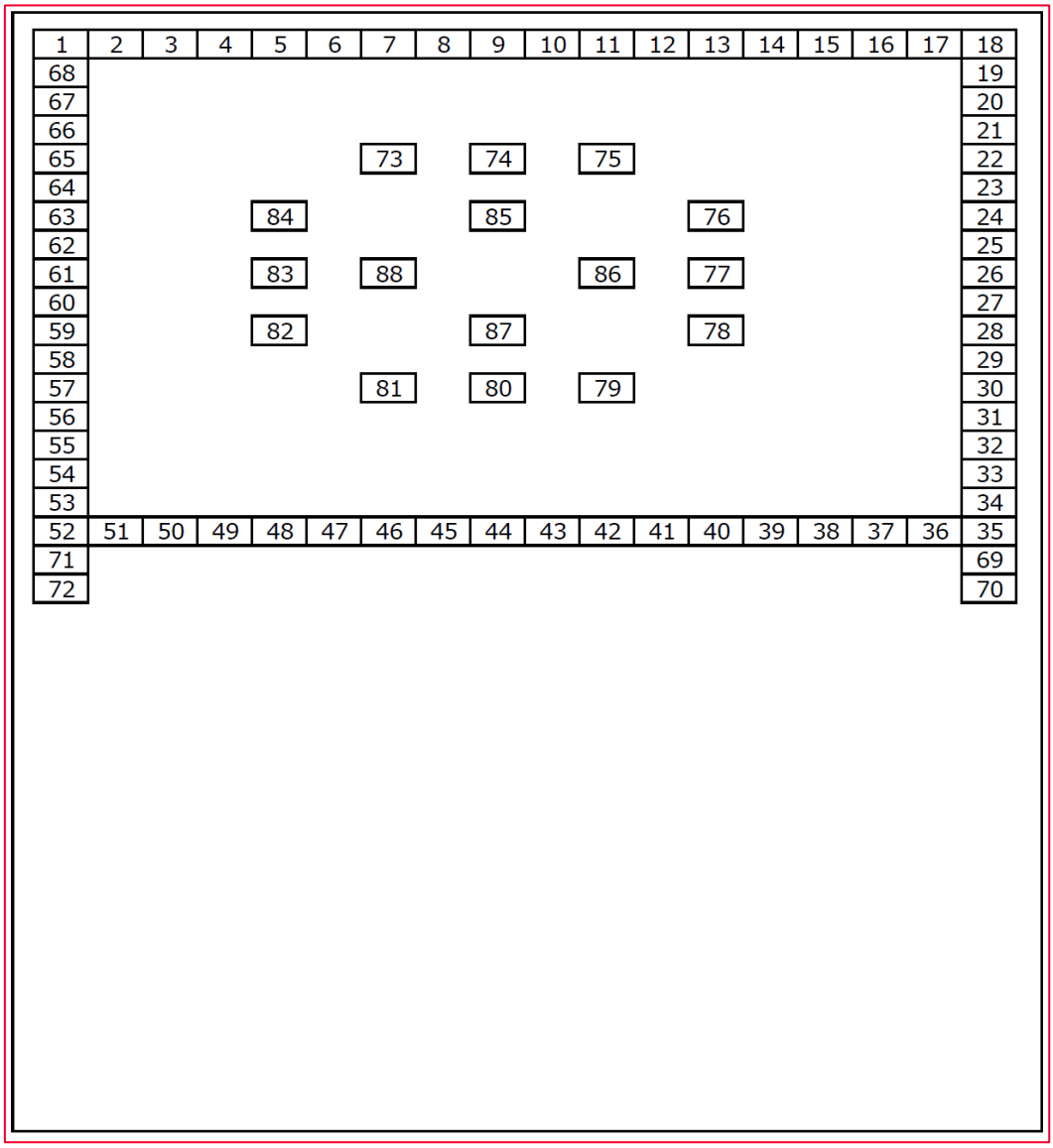
7 Module Pin Descriptions

This section has the pin descriptions and pin assignments layout descriptions of Type 2DS.

7.1 Pin Assignments

The pin assignment layout is shown in **Figure 6**.

Figure 6: Pin Assignment - Top view



The terminal configurations are listed in **Table 6**.

Table 6: Terminal Configurations

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	18	GND	35	GND	52	GND
2	GND	19	GND	36	GND	53	GND
3	USB_DMNS	20	GND	37	GND	54	GND
4	USB_DPLS	21	GND	38	GND	55	VIO
5	GND	22	GND	39	GND	56	GPIO3
6	GND	23	GND	40	GND	57	GPIO2
7	GND	24	GND	41	VBAT	58	GPIO1
8	PDN	25	GND	42	GND	59	GPIO0
9	GND	26	GND	43	GND	60	GND
10	GND	27	GND	44	GND	61	VIO_SD
11	GND	28	GND	45	GND	62	SD_CLK
12	GND	29	NC	46	Reserved	63	SD_CMD
13	NC (REF_CLK_OUT)	30	GND	47	Reserved	64	SD_DAT3
14	CON0	31	Reserved	48	NC (TMS)	65	SD_DAT2
15	CON1	32	GND	49	NC (TDO)	66	SD_DAT1
16	NC (HOST_WAKE)	33	GND	50	NC (TCLK)	67	SD_DAT0
17	GND	34	GND	51	NC (TDI)	68-88	GND

7.2 Pin Descriptions

- Do not need any termination to the open pins in input mode that have an Internal Pull-up/Pull-down resistor (PU/PD). Do not need any termination to the open pins in output mode. Do not need any termination to the USB pins if do not use USB.

Table 7 describes the Type 2DS pins.

Table 7: Pin Descriptions

No.	Pin Name	Type	Connection to IC Pin Name	Supply	Internal PU/PD	Int'l Pull Value [Ω]	Description
1	GND	GND					Ground
2	GND	GND					Ground
3	USB_DMNS	I/O	USB_DMNS	VBAT			USB Serial Differential Data Negative
4	USB_DPLS	I/O	USB_DPLS	VBAT			USB Serial Differential Data Positive

No.	Pin Name	Type	Connection to IC Pin Name	Supply	Internal PU/PD	Int'l Pull Value [Ω]	Description
5	GND	GND					Ground
6	GND	GND					Ground
7	GND	GND					Ground
8	PDN	I	PDn	V_{PD}			Full Power-Down (active low) 0 = full power-down mode 1 = normal mode • Connect to power-down pin of host or 3.3V/1.8V • External host required to drive this pin high for normal operation No internal pull-up on this pin.
9	GND	GND					Ground
10	GND	GND					Ground
11	GND	GND					Ground
12	GND	GND					Ground
13	NC	A,O	REF_CLK_OUT	AVDD18			NC
14	CON0	I	CON[0]	AVDD18	weak PU enable	600K	Configuration Pin (CON[0]) See Configuration Pins
15	CON1	I	CON[1]	AVDD18	weak PU enable	600K	Configuration Pin (CON[1]) See Configuration Pins
16	NC (HOST_WAKE)	I	HOST_WAKE	AVDD18	weak PD enable	700K	NC
17	GND	GND					Ground
18	GND	GND					Ground
19	GND	GND					Ground
20	GND	GND					Ground
21	GND	GND					Ground
22	GND	GND					Ground
23	GND	GND					Ground
24	GND	GND					Ground
25	GND	GND					Ground
26	GND	GND					Ground
27	GND	GND					Ground
28	GND	GND					Ground
29	NC	GND					NC
30	GND	GND					Ground
31	NC						Ground
32	GND	GND					Ground
33	GND	GND					Ground
34	GND	GND					Ground
35	GND	GND					Ground
36	GND	GND					Ground

No.	Pin Name	Type	Connection to IC Pin Name	Supply	Internal PU/PD	Int'l Pull Value [Ω]	Description
37	GND	GND					Ground
38	GND	GND					Ground
39	GND	GND					Ground
40	GND	GND					Ground
41	VBAT	Power	VDD33				3.3V Digital Power Supply
42	GND	GND					Ground
43	GND	GND					Ground
44	GND	GND					Ground
45	GND	GND					Ground
46	NC	O	RF_CNTL1_P-		weak PU enable	600k	NC
47	NC	O	RF_CNTL0_N-		weak PU enable	600k	NC
48	NC	I	TMS		nominal PU enable	100k	NC
49	NC	O	TDO		nominal PU enable	100k	NC
50	NC	I	TCK		nominal PU enable	100k	NC
51	NC	I	TDI		nominal PU enable	100k	NC
52	GND	GND					Ground
53	GND	GND					Ground
54	GND	GND					Ground
55	VIO	Power	VIO				1.8V/3.3V Digital I/O Power Supply
56	GPIO3	I/O	GPIO[3]	VIO	nominal PU enable	100k	GPIO Mode: GPIO[3]
57	GPIO2	I/O	GPIO[2]	VIO	weak PU enable	600k	GPIO Mode: GPIO[2]
58	GPIO1	I/O	GPIO[1]	VIO	weak PU enable	600k	GPIO Mode: GPIO[1] Host Wakeup: SoC-to-Host wakeup (output)
59	GPIO0	I/O	GPIO[0]	VIO	nominal PU enable	100k	GPIO Mode: GPIO[0]
60	GND	GND					Ground
61	VIO_SD	Power	VIO_SD				1.8V/3.3V Digital I/O SDIO Power Supply
62	SD_CLK	I	SD_CLK	VIO_SD	nominal PU enable	100k	SDIO 4-bit Mode: Clock input SDIO 1-bit Mode: Clock input SDIO SPI Mode: Clock input
63	SD_CMD	I/O	SD_CMD/ USB_VBUS_ON	VIO_SD	nominal PU enable	100k	SDIO 4-bit Mode: Command/response (input/output) SDIO 1-bit Mode: Command line

No.	Pin Name	Type	Connection to IC Pin Name	Supply	Internal PU/PD	Int'l Pull Value [Ω]	Description
							SDIO SPI Mode: Data input USB Mode: USB_VBUS_ON (input)
64	SD_DAT3	I/O	SD_DAT[3]	VIO_SD	nominal PU enable	100k	SDIO 4-bit Mode: Data line Bit[3] SDIO 1-bit Mode: Reserved SDIO SPI Mode: Card select (active low)
65	SD_DAT2	I/O	SD_DAT[2]	VIO_SD	nominal PU enable	100k	SDIO 4-bit Mode: Data line Bit[2] or read wait (optional) SDIO 1-bit Mode: Read wait (optional) SDIO SPI Mode: Reserved
66	SD_DAT1	I/O	SD_DAT[1]	VIO_SD	nominal PU enable	100k	SDIO 4-bit Mode: Data line Bit[1] SDIO 1-bit Mode: Interrupt SDIO SPI Mode: Interrupt SDO is tristate when SCSn is inactive. Enables multiple devices driving SDO line.
67	SD_DAT0	I/O	SD_DAT[0]	VIO_SD	nominal PU enable	100k	SDIO 4-bit Mode: Data line Bit[0] SDIO 1-bit Mode: Data line SDIO SPI Mode: Data output
68 - 88	GND	GND					Ground

7.3 Configuration Pins

Table 8 shows the configuration pins for Type 2DS module.

Table 8: Configuration Pins

Configuration Bits	Pin Name	Configuration Function
CON[1]	CONFIG_HOST[1]	Firmware Boot Options 00 = reserved 01 = reserved 10 = SDIO 11 = USB
CON[0]	CONFIG_HOST[0]	

7.4 SDIO Pin Descriptions

Table 9 shows the SDIO pin descriptions.

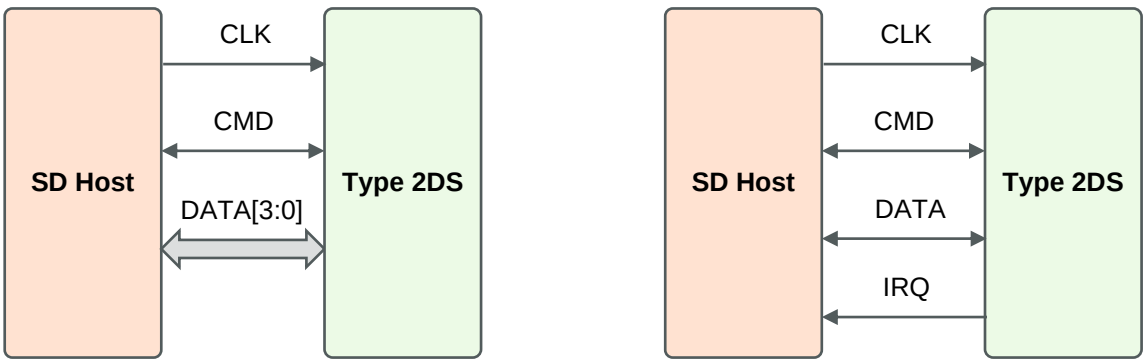
Table 9: SDIO Pin Descriptions

No.	Pin Name	(i) SD 4-bit Mode		(ii) SD 1-bit Mode	
62	SDI_CLK	CLK	Clock input	CLK	Clock input
67	SD_DAT0	DATA0	Data line 0	DATA	Data line
66	SD_DAT1	DATA1	Data line 1	IRQ	Interrupt

No.	Pin Name	(i) SD 4-bit Mode		(ii) SD 1-bit Mode	
65	SD_DAT2	DATA2	Data line 2 or read wait (optional)	RW	Read wait (optional)
64	SD_DAT3	DATA3	Data line 3	NC	Reserved
63	SD_CMD	CMD	Command/response (input/output)	CMD	Command line

Figure 7 shows the different SDIO modes.

Figure 7: SDIO Modes



(i) SD 4-bit Mode

(ii) SD 1-bit Mode

8 Absolute Maximum Ratings

The absolute maximum ratings are shown in **Table 10: Absolute Maximum Ratings**.

Table 10: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-40	+85	°C
Supply Voltage	VBAT		4.0	V
	VIO		4.0	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

9 Operating Condition

9.1 Operating Condition

The operating conditions are shown in **Table 11**.

Table 11: Operating Conditions

Parameter			Minimum	Typical	Maximum	Unit
Operating Temperature Range		Ta	-40	+25	+85	°C
		Tj			+125	°C
Supply Voltage	VBAT		2.97	3.3	3.63	V
	VIO		1.62	1.8	1.98	V
			2.97	3.3	3.63	V
Internal 1.8V	AVDD18		1.71	1.8	1.89	V
IO Current	VIO			0.1	0.5	mA
Peak current[1]	VBAT			430	550	mA

Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

9.2 Digital I/O Requirements

Table 12: Digital I/O Requirements

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage		0.7 * VIO		VIO + 0.4	V
V_{IL}	Input low voltage		-0.4		0.3 * VIO	V
V_{HYS}	Input hysteresis		100			mV
V_{OH}	Output high voltage		VIO - 0.4			V
V_{OL}	Output low voltage				0.4	V
V_{PDH}	Input high voltage		1.4		5.5	V
V_{PDL}	Input low voltage		-0.4		0.5	V

9.3 Package Thermal Conditions

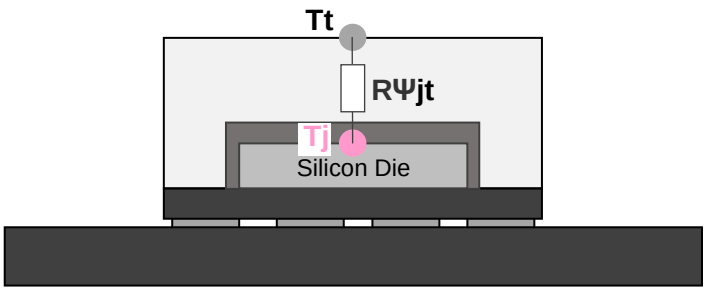
The package thermal conditions as shown in **Figure 8** are as below:

- RΨjt: 7.09 °C/W
- RΨjt = (Tj - Tt)/P

Tj: Junction temperature (℃), Tt: Top temperature (℃), P: Total Power Consumption (W)

[1] Peak current of VBAT (RF portion) occurs during DPD calibration when the firmware is downloaded.

Figure 8: Package Thermal Conditions



10 Power Sequence

This section describes the power-on and power-off sequences along with their parameters.

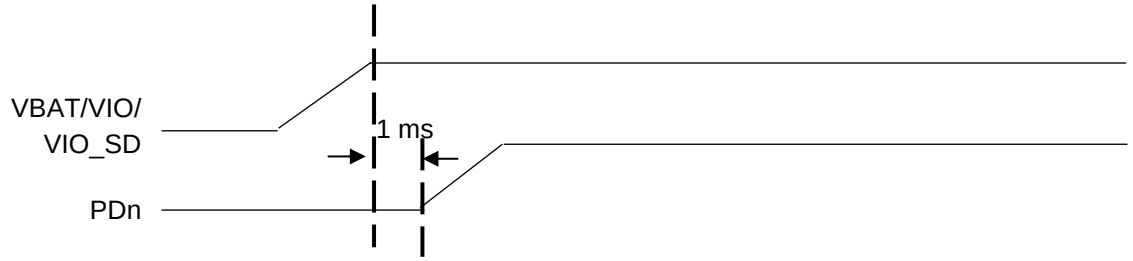
10.1 Power-On Sequence

Option 1

- External VBAT/VIO/VIO_SD from host.
- PDn driven by host

Figure 9 shows the power-on sequence graph for PDn driven by host.

Figure 9: Power-On Sequence Graph (PDn driven by Host)



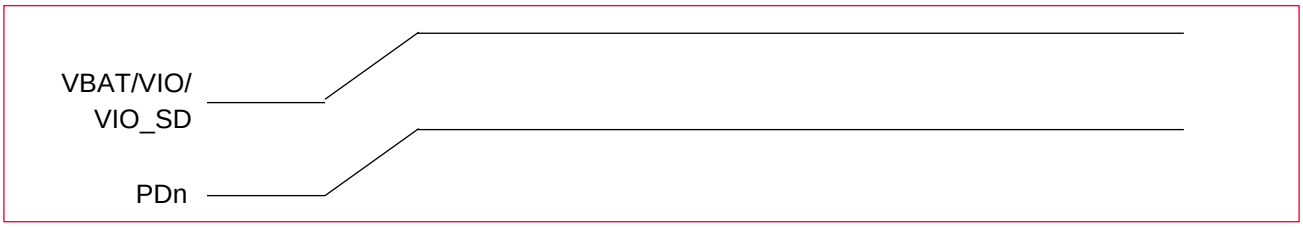
- Assert PDn low (active) during VBAT/VIO/VIO_SD ramp-up.
- Continue to assert low for a minimum of 1 ms after VBAT/VIO/VIO_SD are stable.

Option 2

- External VBAT/VIO/VIO_SD from host.
- PDn is tied to VBAT.

Figure 10 shows the power-on sequence graph for PDn tied to VBAT.

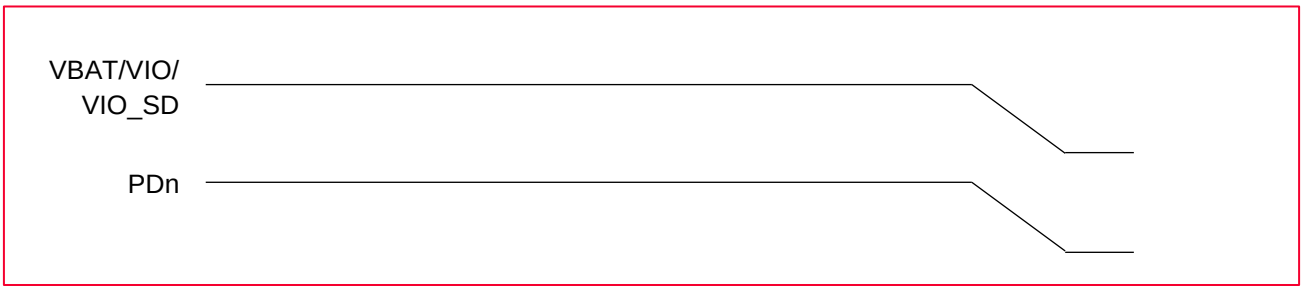
Figure 10: Power-On Sequence Graph (PDn tied to VBAT)



10.2 Power-Off Sequence

Figure 11 shows the power-off sequence graph.

Figure 11: Power-Off Sequence Graph



All power rails can be powered off. In this case, the state of the PDn Pin is irrelevant.

11 Interface Timing

This section describes the SDIO/USB timing for different modes.

11.1 SDIO Specifications

- The SDIO host interface pins are powered from the VIO_SD voltage supply.
- The SDIO electrical specifications are identical for 1-bit SDIO and 4-bit SDIO modes.

11.1.1 Normal, High Speed Modes

Figure 12 shows the SDIO protocol timing diagram in normal mode.

Figure 12: SDIO Protocol Timing Diagram - Normal Mode

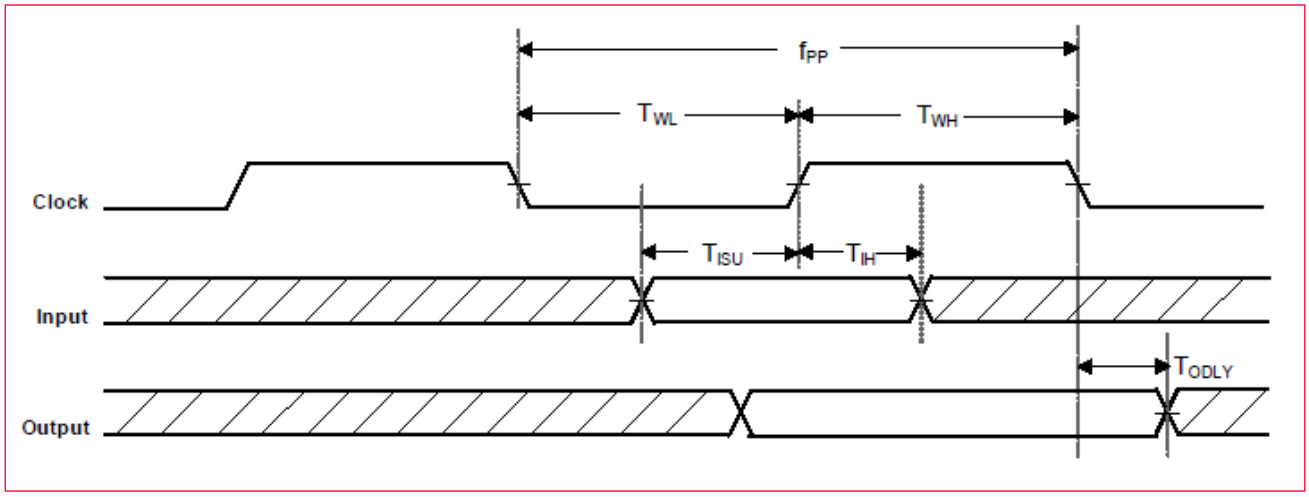


Figure 13 shows the SDIO protocol timing diagram in high speed mode (3.3V).

Figure 13: SDIO Protocol Timing Diagram - High Speed Mode (3.3V)

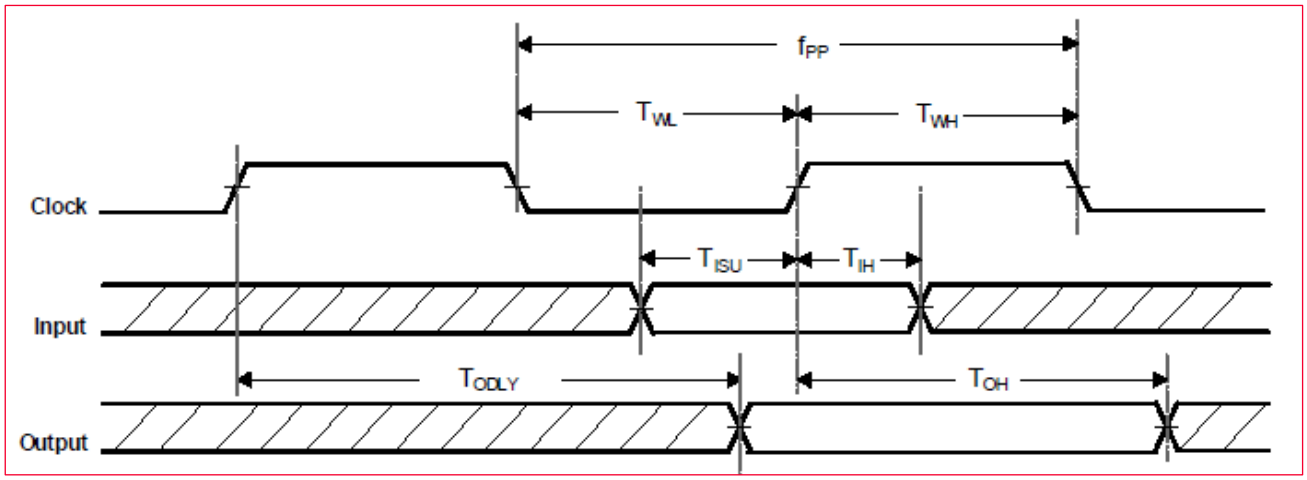


Table 13 describes the SDIO timing data for normal and high speed modes[2].

Table 13: SDIO Timing Data - Normal, High Speed Modes

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	Normal	0		25	MHz
		High speed	0		50	MHz
T_{WL}	Clock low time	Normal	10			ns
		High speed	7			ns
T_{WH}	Clock high time	Normal	10			ns
		High speed	7			ns
T_{ISU}	Input setup time	Normal	5			ns
		High speed	6			ns
T_{IH}	Input hold time	Normal	5			ns
		High speed	2			ns

[2] The SDIO-SPI CS signal timing is identical to all other SDIO inputs.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{ODLY}	Output delay time	Normal			14	ns
		High speed			14	ns
T_{OH}	Output hold time	High speed	2.5			ns

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

11.2 USB Specifications

The USB device interface is compliant with the Universal Serial Bus Specification, Revision 2.0, April 27, 2000. A USB host uses the USB cable bus and the USB 2.0 device interface to communicate with the chip.

Main features of the USB device interface include:

- High/full speed operation (480/12 Mbps)
- Suspend/host resume/device resume (remote wake-up)
- Built-in DMA engine that reduces interrupt loads on the embedded processor and reduces the system bus bandwidth requirement for serving the USB device operation
- Supports Link Power Management (LPM), corresponding host resume, or device resume (remote wakeup) to exit from L1 sleep state

The USB 2.0 device interface is designed with 3.3V signal level pads.

Table 14: Interface Signal Description

Module signal name	USB2.0 spec name	Type	Description
VBAT	VBUS		USB Bus Power Supply On-board regulator regulates voltage from VBUS level to voltage levels used by USB PHY.
SD_CMD/USB_VBUS_ON		I	USB Vbus On USB power valid indication
	GND		USB Bus Ground Common ground on SoC device
USB_DPLS	D+	I/O	USB Bus Data Plus 1 of the differential data pair.
USB_DMNS	D-	I/O	USB Bus Data Minus 1 of the differential data pair.

USB 2.0 device host interface pins are powered from the VBAT voltage supply.

11.2.1 USB Electrical Characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 15: USB Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
Supply Current						
I_{CCHPF}	High-power function				500	mA
I_{CCLPF}	Low-power function				100	mA
I_{CCINIT}	Unconfigured function				100	mA
I_{CCSH}	Suspended high-power device				2.5	mA
I_{CCSL}	Suspended low-power device				500	µA
Input Levels for Low/Full Speed						
V_{IH}	Input high voltage (driven)		2.0			V
V_{IHZ}	Input high voltage (floating)		2.7		3.6	V
V_{IL}	Input low voltage				0.8	V
V_{DI}	Differential input sensitivity		0.2			V
V_{CM}	Differential common mode range		0.8		2.5	V
Input Levels for High Speed						
V_{HSSQ}	High speed squelch detection threshold (differential signal amplitude)		100		150	mV
V_{HSDSC}	High speed disconnect detection threshold (differential signal amplitude)		525		625	mV
-	High speed differential input signaling levels	Specified by eye pattern templates; see Section 7.1.7.2 in the USB 2.0 specification.				
V_{HSCM}	High speed data signaling common mode voltage range		-50		500	mV
Output Levels for Low/Full Speed						
V_{OL}	Output low voltage		0.0		0.3	V
V_{OH}	Output high voltage (driven)		2.8		3.6	V
V_{OSE1}	Output SE1 voltage		0.8			V
V_{CRS}	Output signal crossover voltage		1.3		2.0	V
Output Levels for High Speed						
V_{HSOI}	High speed idle level		-10.0		10.0	mV
V_{HSOH}	High speed data signaling high		360		440	mV
V_{HSOL}	High speed data signaling low		-10.0		10.0	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700		1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		-900		-500	mV
Decoupling Capacitance						
C_{RPB}	Upstream facing port bypass capacitance		1.0		10.0	µF
Input Capacitance for Low/Full Speed						
C_{INUB}	Upstream facing port capacitance (without cable)				100	pF

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
C_{EDGE}	Transceiver edge rate control capacitance				75	pF
Input Impedance for High Speed						
	TDR spec for high speed termination	Differential impedance	80		100	W
Terminations						
R_{PUI}	Bus pull-up resistor on upstream port (idles bus)		0.900		1.575	kΩ
R_{PUA}	Bus pull-up resistor on upstream port (receiving)		1.425		3.090	kΩ
Z_{INP}	Input impedance exclusive of pull-up/pull-down (for low/full speed)		300			kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up resistor (R_{PU})		3.0		3.6	V
Terminations in High Speed						
V_{HSTERM}	Termination voltage in high speed		-10		10	mV

11.2.2 High Speed Source Electrical Characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 16: High Speed Source Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
Driver Characteristics						
T_{HSR}	Rise Time (10% - 90%)		500			ps
T_{HSF}	Fall Time (10% - 90%)		500			ps
-	Driver waveform requirements	Specified by eye pattern templates in Section 7.1.2 in the USB 2.0 specification.				
Z_{HSDRV}	Driver output resistance (also serves as high speed termination)		40.5		49.5	W
Clock Timings						
T_{HSDRAT}	High speed data rate		479.760		480.240	Mb/s
T_{HSFRAM}	Micro frame interval		124.9375		125.0625	µs
T_{HSRFI}	Consecutive micro frame interval difference				4 high speed bit times	
High Speed Data Timings						
	Data source jitter	Specified by eye pattern templates in Section 7.1.2.2 in the USB 2.0 specification.				
	Received jitter tolerance	Specified by eye pattern templates in				

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
		Section 7.1.2.2 in the USB 2.0 specification.				

11.2.3 Full Speed Source Electrical Characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 17: Full Speed Source Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
Driver Characteristics						
T_{FR}	Rise time		4		20	ns
T_{FF}	Fall time		4		20	ns
T_{FRFM}	Differential rise and fall time matching	T_{FR}/T_{FF}	90		111.11	%
Clock Timings						
$T_{FDRATHS}$	Full speed data rate	Average bit rate	11.9940		12.0060	Mb/s
T_{FDRATE}	Frame interval		0.9995		1.00005	ms
T_{RFI}	Consecutive frame interval difference	No clock adjustment			42	ms
Full Speed Data Timings						
T_{DJ1}	Source jitter total to next transition (including frequency tolerance)		-3.5		3.5	ns
T_{DJ2}	Source jitter total for paired transitions (including frequency tolerance)		-4		4	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition		-2		5	ns
T_{JR1}	Receiver jitter to next transition		-18.5		18.5	ns
T_{JR2}	Receiver jitter to next transition		-9		9	ns
T_{FEOPT}	Source SE0 interval of EOP		160		175	ns
T_{FEOPR}	Receiver SE0 interval of EOP		82			ns
T_{FST}	Width of SE0 interval during differential transition				14	ns

11.2.4 Device Event Timing Characteristics

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

Table 18: Device Event Timing Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
T_{SIGATT}	Time from internal power good to device pulling D+/D- beyond V_{IHZ} (minimum) (signaling attach)				100	ms
T_{ATTDB}	Debounce interval provided by USB system software after attach				100	ms
T_{2SUSP}	Maximum time a device can draw power > suspend power when bus is continuously in idle state				10	ms
$T_{SUSAVGI}$	Maximum duration of a suspend averaging interval				1	s
T_{WTRSM}	Period of idle bus before device can initiate resume	Device must be remote-wake-up enabled	5			ms
T_{DRSMUP}	Duration of driving resume upstream		1		15	ms
T_{RSMCY}	Resume recovery time	Provided by USB system software	10			ms
T_{RSTRCY}	Reset recovery time				10	ms
T_{IPD}	Inter-packet delay (for low/full speed)		2			bit times
$T_{RSPIPD1}$	Inter-packet delay for device response with detachable cable for low/full speed				6.5	bit times
$T_{RSPIPD2}$	Inter-packet delay for device response with captive cable for low/full speed				7.5	bit times
$T_{DSETADDR}$	SetAddress() completion time				50	ms
$T_{DRQCMPLTND}$	Time to complete standard request with no data				50	ms
$T_{DRETDATA1}$	Time to deliver first and subsequent (except last) data for standard request				500	ms
$T_{DRETDATAN}$	Time to deliver last data for standard request				50	ms
$T_{HSRSPIPD2}$	Inter-packet delay for device response with captive cable (high speed)				192 bit times + 52 ns	
Reset Handshake Protocol						
$F_{FILTSE0}$	Time for which a suspended high speed capable device must see a continuous SE0 before beginning the high speed detection handshake		2.5			µs
$T_{WTRSTFS}$	Time for which a high speed capable device operating in non-suspended full speed must wait		2.5		3000	µs

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
	after start of SE0 before beginning the high speed detection handshake					
T_{WTREV}	Time for which a high speed capable device operating in high speed must wait after start of SE0 before reverting to full speed		3.0		3.125	ms
$T_{WTRSTHS}$	Time for which a device must wait after reverting to full speed before sampling the bus state for SE0 and beginning the high speed detection handshake		100		875	µs
T_{UCH}	Minimum duration of a Chirp K from a high speed capable device within the reset protocol		1.0			ms
T_{UCHEND}	Time after start of SE0 by which a high speed device capable device is required to have completed its Chirp K within the reset protocol				7.01	ms
T_{WTHS}	Time after end of upstream chirp at which device enters the high speed default state if downstream chirp is detected				500	µs
T_{WTFS}	Time after end of upstream chirp at which device reverts to full speed default state if no downstream chirp is detected		1.0		2.5	ms

11.2.5 LPM Timing Characteristics

Table 19: LPM Timing Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
$TL1_{Residency}$	L1 residency		50		>50	µs
$TL1_{TokenRetry}$	Device delay before transitioning to L1 after transmitting ACK		8		10	µs
$TL1_{HubDrvResume1}$	Host initiated L1 exit host drives resume time		50 ± 1		1200 ± 1	µs
$TL1_{DevDrvResume}$	Device initiated L1 exit Device drives resume time		50 ± 1			µs
$TL1_{ExitDevRecovery}$	L1 exit device recovery time		10			µs
$TL1_{ExitLatency1}$	L1 exit latency (host initiated)		60		1210	µs
$TL1_{ExitLatency2}$	L1 exit latency (device initiated)		70		1000	µs

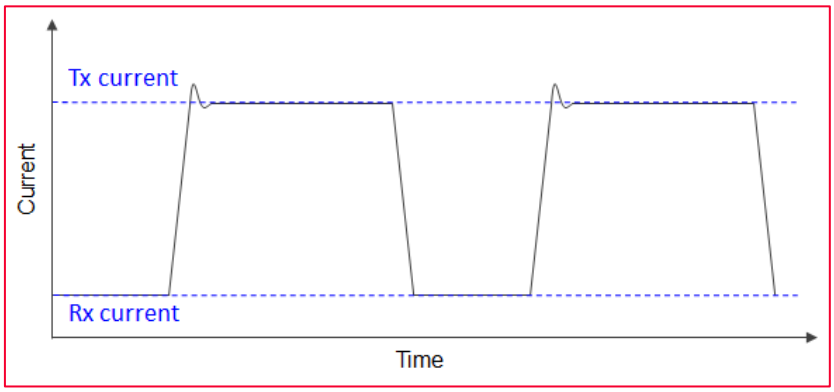
12 DC/RF Characteristics

ALL DC/RF characteristics are defined by following files.

Table 20: DC/RF Characteristics and Files

Characteristic	Filenames
WLAN Tx Power	txpower_US.bin, txpower_CA.bin, txpower_EU.bin, txpower_JP.bin
WLAN Regulatory Limit	db.txt
Energy Detect	ed_mac.bin

Figure 14: Burst Current Definition



12.1 DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Table 21: Characteristics Values for IEEE 802.11b - 2.4 GHz

Items	Contents
Specification	IEEE 802.11b – 2.4 GHz
Mode	DSSS / CCK
Channel Frequency	2412 - 2472 MHz (5 MHz)
Data rate	1, 2, 5.5, 11 Mbps

12.1.1 High-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, Output power setting = 17 dBm at module pad, 11 Mbps mode

Table 22: High-Rate Condition for IEEE 802.11b - 2.4 GHz

Items	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC current				
• Tx mode		330	408	mA
• Rx mode		69	92	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	14.5	17.0	19.5	dBm
Spectrum Mask Margin				
• 1st side lobes (-30 dBr)	0			dB
• 2nd side lobes (-50 dBr)	0			dB
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency tolerance	-25		25	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-76	dBm
Maximum Input Level (FER ≤ 8%)	-10			dBm
Adjacent Channel Rejection (FER < 8%)	35			dB

12.1.2 Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, Output power setting = 17 dBm at module pad, 1 Mbps mode

Table 23: Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Items	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC current				
• Tx mode		335	417	mA
• Rx mode		69	91	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	14.5	17.0	19.5	dBm
Spectrum Mask Margin				
• 1st side lobes (-30 dBr)	0			dB
• 2nd side lobes (-50 dBr)	0			dB
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency tolerance	-25		25	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-80	dBm
Maximum Input Level (FER ≤ 8%)	-4			dBm
Adjacent Channel Rejection (FER < 8%)	35			dB

12.2 DC/RF Characteristics for IEEE 802.11g - 2.4 GHz

Table 24: Characteristics Values for IEEE 802.11g - 2.4 GHz

Items	Contents
Specification	IEEE 802.11g
Mode	OFDM
Channel Frequency	2412 - 2472 MHz
Data rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.2.1 High-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, Output power setting = 14 dBm at module pad, 54 Mbps mode

Table 25: High-Rate Condition for IEEE 802.11g - 2.4 GHz

Items	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC current				
• Tx mode		302	376	mA
• Rx mode		72	94	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	11.5	14.0	16.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM)			-25	dB
Frequency tolerance	-25		25	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER < 10%)			-65	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

12.2.2 Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, Output power setting = 15 dBm at module pad, 6 Mbps mode

Table 26: Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Items	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC current				
• Tx mode		313	391	mA
• Rx mode		71	93	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	12.5	15.0	17.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM)	-		-5	dB
Frequency tolerance	-25		25	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
• Minimum Input Level (PER < 10%)			-82	dBm
• Maximum Input Level (PER < 10%)	-20			dBm
• Adjacent Channel Rejection (PER < 10%)	-1			dB

12.3 DC/RF Characteristics for IEEE 802.11n - 2.4 GHz

Table 27: Characteristics Values for IEEE 802.11n - 2.4 GHz

Items	Contents
Specification	IEEE 802.11n
Mode	OFDM
Channel Frequency	2412 - 2472 MHz
Data rate	MCS0 - MCS7

12.3.1 High-Rate Condition for IEEE 802.11n - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, Output power setting = 13 dBm at module pad, MCS7 mode

Table 28: High-Rate Condition for IEEE 802.11n - 2.4 GHz

Items	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC current				
• Tx mode		302	378	mA
• Rx mode		72	94	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	11.5	14.0	16.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-27	dB
Frequency tolerance	-25		25	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
• Minimum Input Level (PER ≤ 10%)			-64	dBm
• Maximum Input Level (PER < 10%)	-20			dBm
• Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.3.2 Low-Rate Condition for IEEE 802.11n - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, Output power setting = 15 dBm at module pad, MCS0 mode

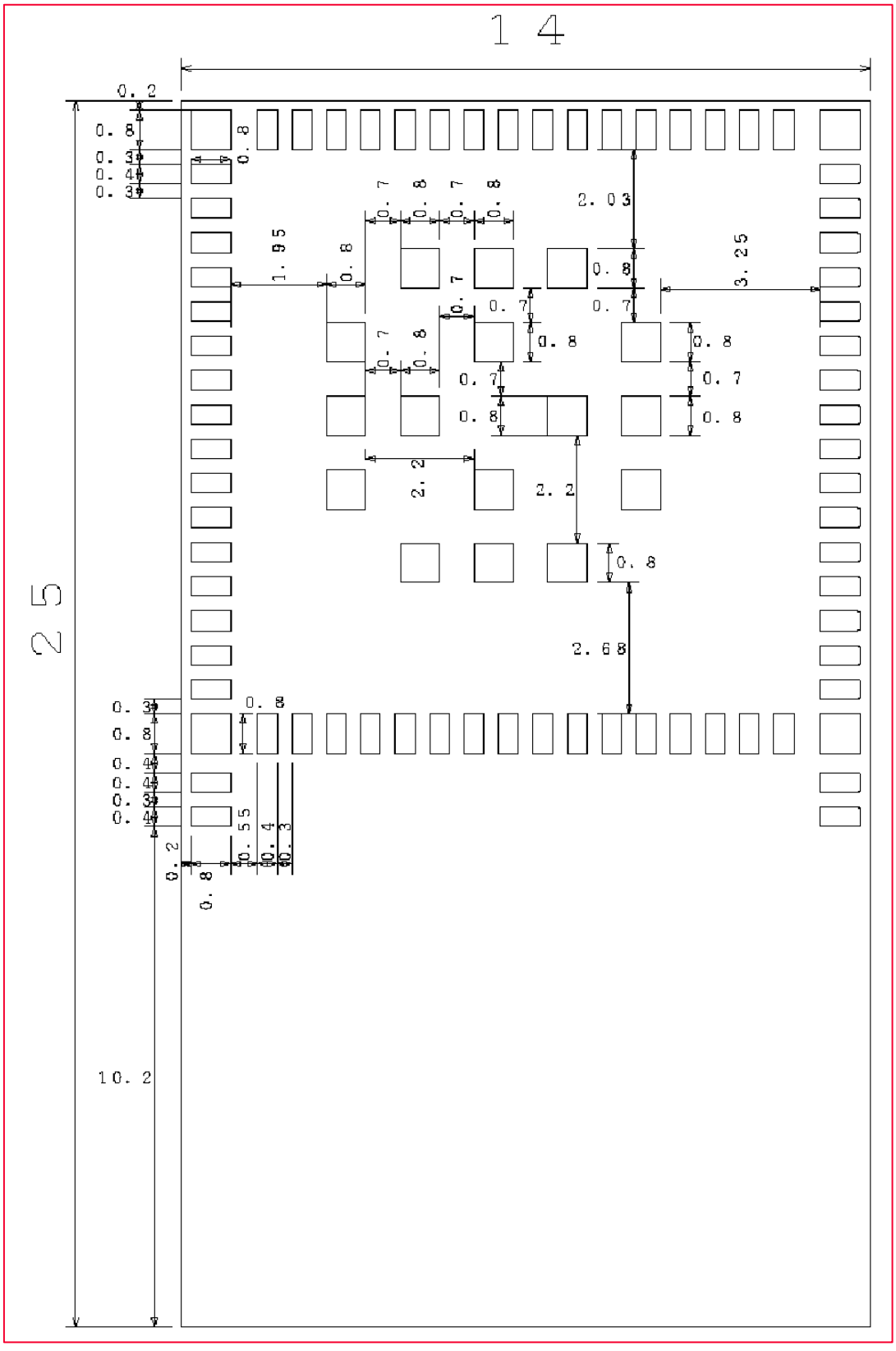
Table 29: Low-Rate Condition for IEEE 802.11n - 2.4 GHz

Items	Contents			
DC Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
DC current				
• Tx mode		315	392	mA
• Rx mode		71	93	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	12.5	15.0	17.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-5	dB
Frequency tolerance	-25		25	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
• Minimum Input Level (PER ≤ 10%)			-82	dBm
• Maximum Input Level (PER < 10%)	-20			dBm
• Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

13 Land Pattern

The Land Pattern is shown in **Figure 15**.

Figure 15: Land Pattern



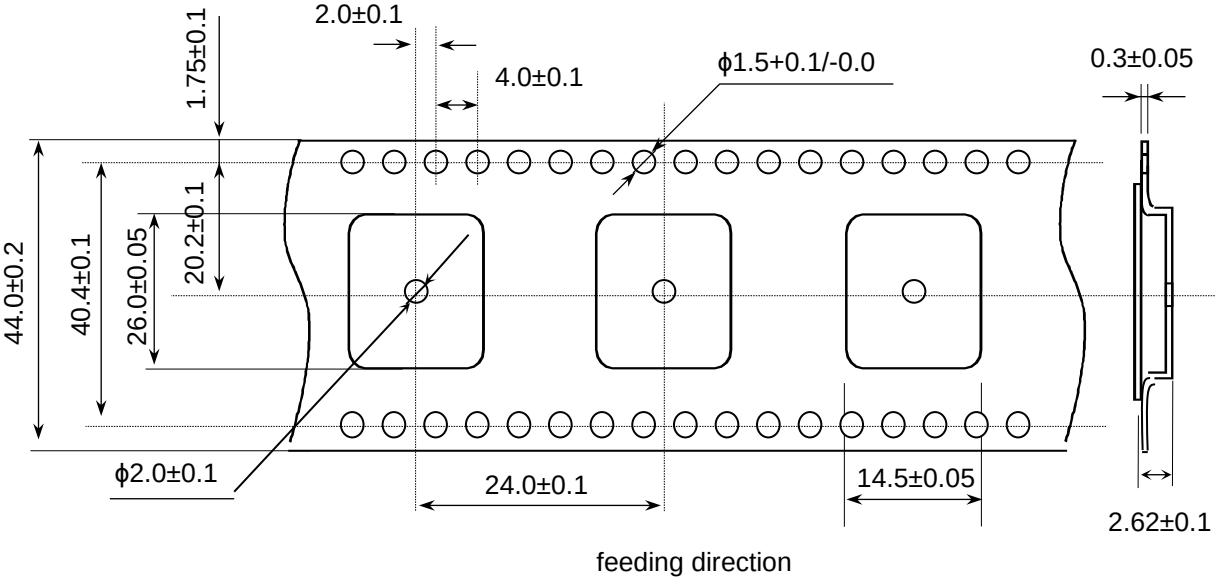
14 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

14.1 Dimensions of Tape (Plastic tape)

Figure 16 is a graphical representation of the tape dimension (plastic tape)[3].

Figure 16: Dimensions of Tape (Unit: mm)

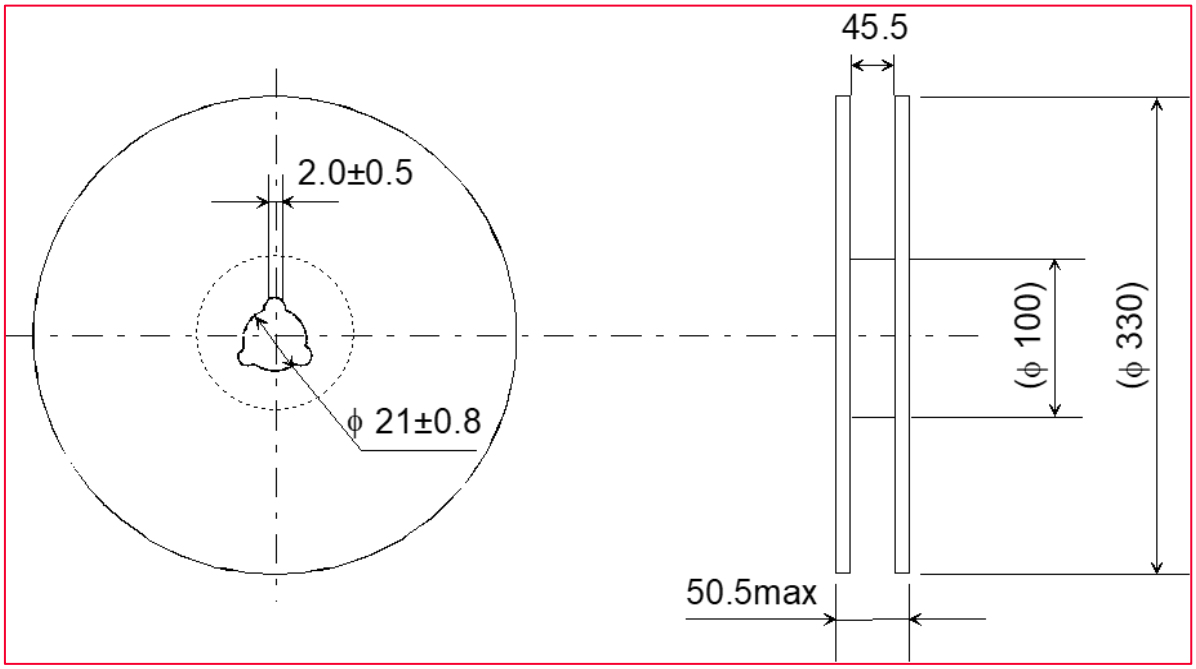


[3] Cumulative tolerance of maximum 40 +/- 0.15 mm for every 10 pitches.

14.2 Dimensions of Reel

Figure 17 shows the reel dimensions.

Figure 17: Dimensions of Reel (Unit: mm)



14.3 Taping Diagrams

Figure 18 shows the taping diagrams.

Figure 18: Taping Diagrams

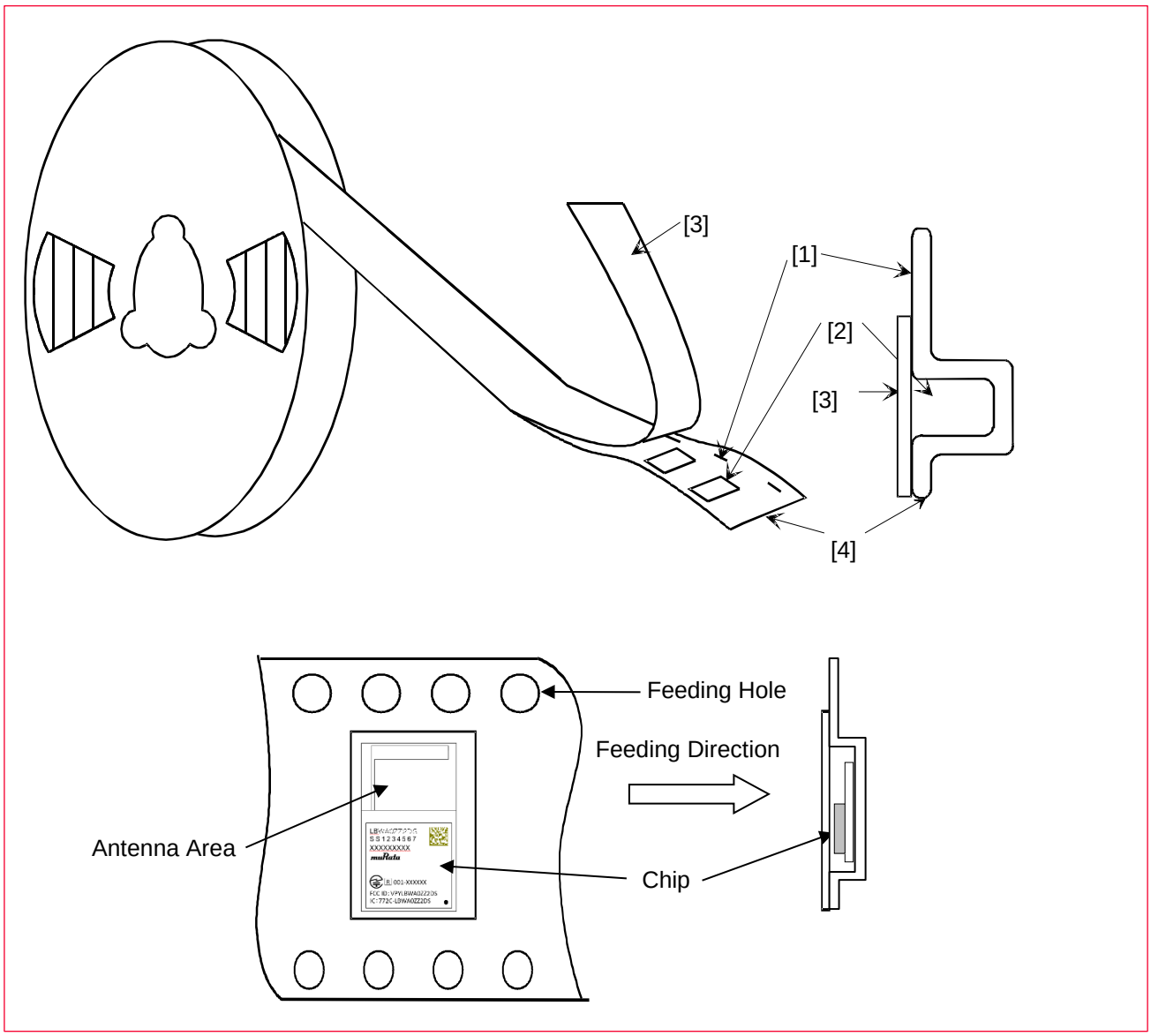


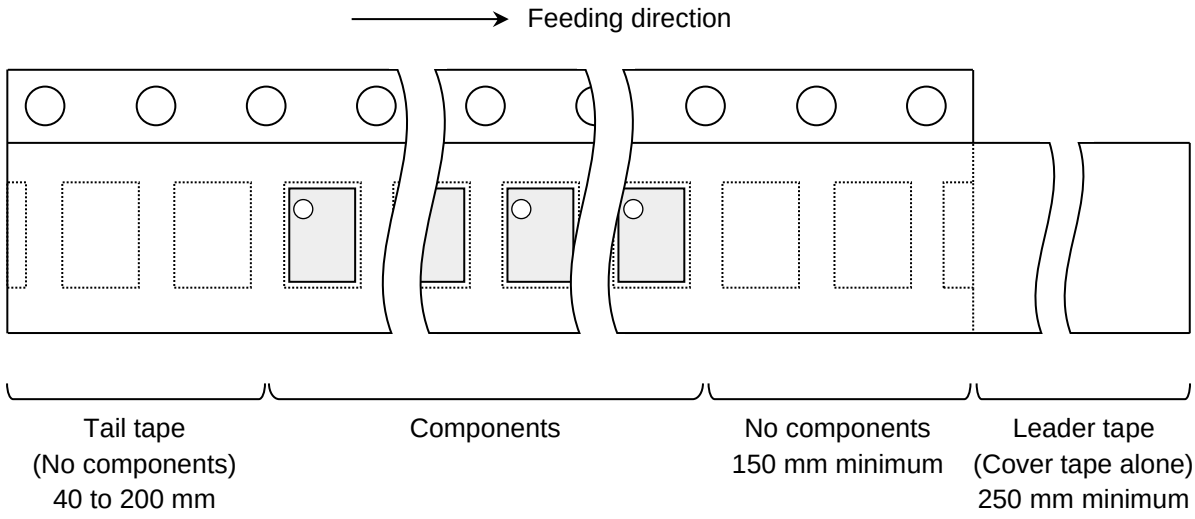
Table 30: Taping Specifications

Mark	Description
1	Feeding Hole. As specified in Dimensions of Tape (Plastic tape).
2	Hole for chip. As specified in Dimensions of Tape (Plastic tape).
3	Cover tape. 62 µm in thickness.
4	Base tape. As specified in Dimensions of Tape (Plastic tape).

14.4 Leader and Tail tape

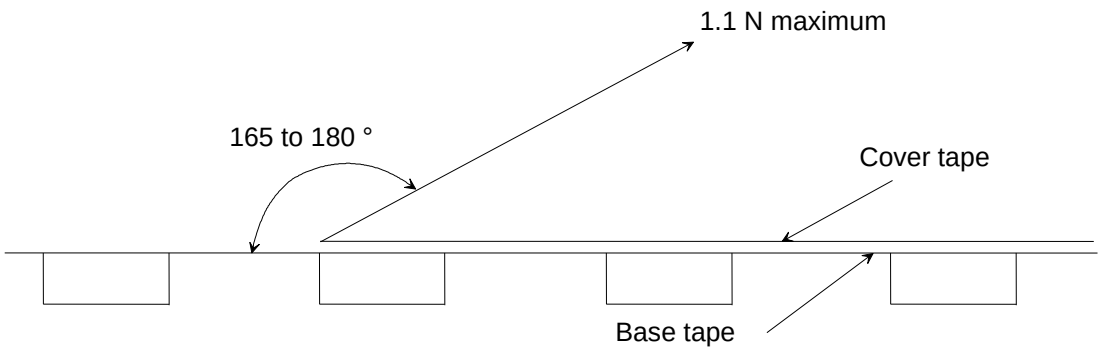
The leader and tail tape are shown in **Figure 19.**

Figure 19: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape : 5 N minimum.
- Packaging unit : 500 pcs./ reel
- Material
  - Base tape : Plastic
  - Real : Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling of force: 1.1 N maximum in the direction of peeling as shown in **Figure 20**.

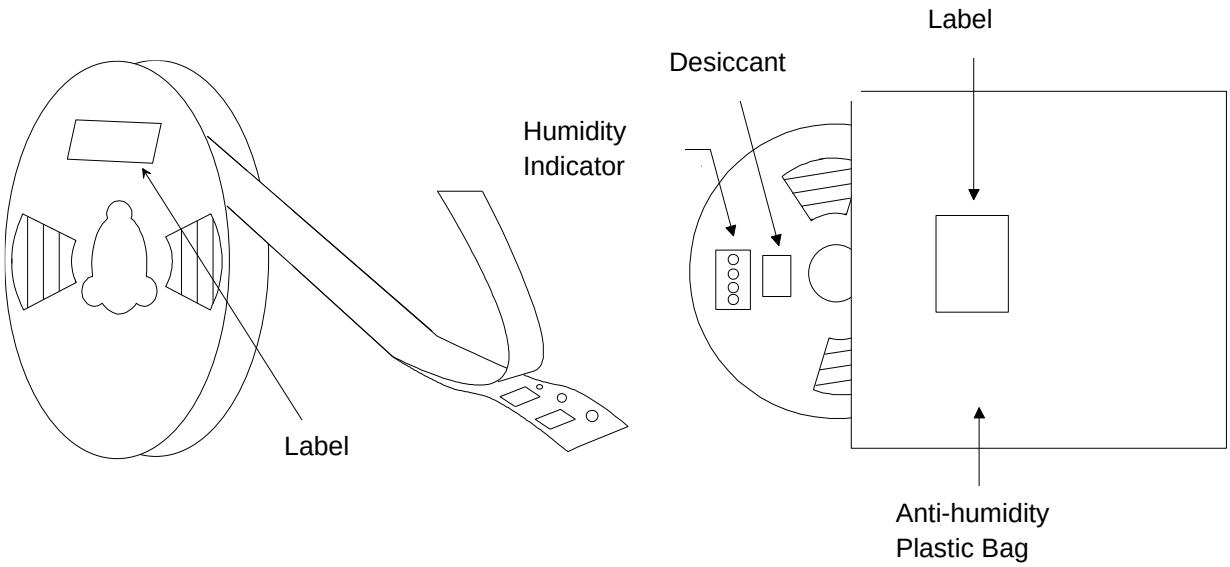
Figure 20: Peeling Off Force



14.5 Packaging (Humidity Proof Packing)

Figure 21 shows the humidity proof packaging.

Figure 21: Humidity Proof Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

15 Notice

15.1 Storage Conditions

- Please use this product within 6 months after receipt.
  - The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH.
  - (Packing materials, in particular, may be deformed at the temperature over 40 °C)
  - The product left more than 6 months after reception; it needs to be confirmed the solderability before used.
  - The product shall be stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
  - Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)
  - After the packing opened, the product shall be stored at <30 °C / <60 %RH and the product shall be used within 168 hours.
  - When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition : 125 +5/-0 °C, 24 hours, 1 time
- The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

15.2 Handling Conditions

Be careful in handling or transporting products because excessive stress or mechanical shock may break products.

Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

15.3 Standard PCB Design (Land Pattern and Dimensions)

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

15.4 Notice for Chip Placer

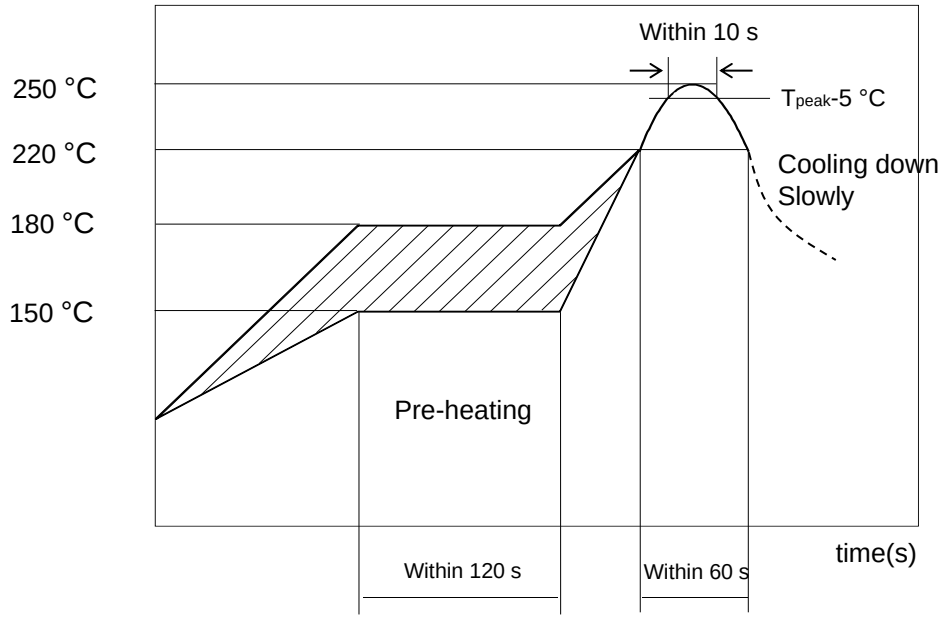
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

15.5 Soldering Conditions

The recommendation conditions of soldering are as in the following figure.

Soldering must be carried out by the above-mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Figure 22: Reflow Soldering Standard Conditions (Example)



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

15.6 Cleaning

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

15.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_X, NO_X etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

As it might be a cause of degradation or destruction to apply static electricity to products, do not apply static electricity or excessive voltage while assembling and measuring.

16 Preconditions to Use Our Products

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

WE HEREBY DISCLAIM ALL OTHER WARRANTIES REGARDING THE PRODUCTS, EXPRESS OR IMPLIED, INCLUDING WITHOUT LIMITATION ANY WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, THAT THEY ARE DEFECT-FREE, OR AGAINST INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS.

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The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment.
- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.

- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.
- We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

Even in the unlikely event that an abnormality or malfunction occurs in this product under operating conditions that conform to the specifications, be sure to add an appropriate fail-safe function to the system to prevent secondary accidents.

We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.

Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

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If you can’t agree with the above contents, please contact sales.

Revision History

Revision Code	Date	Changed Item	Comments
1	2020.07.15	-	First issue.
2 (A)	2020.12.16	7. Module Pin Descriptions 9. Operating Conditions 12. DC / RF Characteristics 14. Reference Circuit 15. Tape and Reel Packing	• Updated • Added Internal 1.8V(AVVD18) • Updated • Added • Added
3 (B)	2021.01.14	5. Certification Information 12. DC/RF Characteristics 11.2 USB Specifications	• Added certification information • Updated file name of configuration files • Added information (Section 11.2.1 to 11.2.5)
4 (C)	2021.03.15	6. Dimensions, Marking and Terminal Configurations 9. Operating Conditions 10. Power Up Sequence 12. DC/RF Characteristics 12.3.3 High Rate Conditions for IEEE 802.11n 14. Reference Circuit Appendix (Base IC datasheet revision: 5)	• Added Marking • Updated Peak current • Updated • Updated DC current • Updated Tx power. • Updated Reference Circuit • Added configuration manual
5 (D)	2021.05.19	6. Dimensions, Marking and Terminal Configurations 7.2 Pin Description	• Added Dimensional tolerance • Added Internal pull values
6 (E)	2021.08.20	5. Certification Information	• Added configuration files for FreeRTOS
7 (F)	2021.12.14	3. Ordering Information 9. Operating Conditions	• Added Updated the list • Defined IO current and Peak current
8 (G)	2022.06.09	Appendix	• Translated Japanese to English
9 (H)	2022.12.01	2. Key Features 9.3 Package Thermal Conditions Appendix	• Added Total Fit • Added • Added Europe • Changed the description of the RF power setting
10 (I)	2022.12.12	2. Key Features 3. Ordering Information 7.2 Pin Descriptions 14. Reference Circuit Appendix	• Updated information • Added Embedded Artists' M.2 module information. • Added comments on termination of open pins. • Moved section to HW app note. • Moved Appendix information into Sections 14. • Moved antenna sections to HW app note. Updated to new format
11	2025.02.14	Revision History 6.2 Marking (14. Radio Regulatory Cert…)	• Changed Revision rule • Added a warning message on UL certification. • Removed the section.

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