

# Type 2AE Wi-Fi™ + Bluetooth® Module

Infineon CYW4373E Chipset for 802.11a/b/g/n/ac +  
Bluetooth 5.2 Datasheet - Rev. 16

- Design Name: Type 2AE
- Module P/N: LBEE5PK2AE-564



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## About This Document

Type 2AE is a small and very high-performance module based on Infineon CYW4373E combo chipset which supports Wi-Fi 802.11a/b/g/n/ac + Bluetooth 5.2 BR/EDR/LE. This datasheet describes Type 2AE module in detail.



Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

## Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product; specifically RF, hardware, software, and systems engineers.

## Document Conventions

**Table 1** describes the document conventions.

**Table 1: Document Conventions**

| Conventions                                                                         | Description                                                                                                                                                                                                                                                                                                                                                                                   |
|-------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <b>Warning Note</b><br>Indicates very important note. Users are strongly recommended to review.                                                                                                                                                                                                                                                                                               |
|  | <b>Info Note</b><br>Intended for informational purposes. Users should review.                                                                                                                                                                                                                                                                                                                 |
|  | <b>Menu Reference</b><br>Indicates menu navigation instructions.<br><b>Example:</b> Insert → Tables → Quick Tables → Save Selection to Gallery                                                                                                                                                           |
|  | <b>External Hyperlink</b><br>This symbol indicates a hyperlink to an external document or website.<br><b>Example:</b> <a href="#">Murata</a> <br>Click on the text to open the external link.                                                                                                              |
|  | <b>Internal Hyperlink</b><br>This symbol indicates a hyperlink within the document.<br><b>Example:</b> <a href="#">Scope</a> <br>Click on the text to open the link.                                                                                                                                       |
| <code>Console input/output or code snippet</code>                                   | <b>Console I/O or Code Snippet</b><br>This text <b>Style</b> denotes console input/output or a code snippet.                                                                                                                                                                                                                                                                                  |
| <code># Console I/O comment<br/>// Code snippet comment</code>                      | <b>Console I/O or Code Snippet Comment</b><br>This text <b>Style</b> denotes a console input/output or code snippet comment. <ul style="list-style-type: none"> <li>• Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output.</li> <li>• Code Snippet comment (preceded by "//") may exist in the original code.</li> </ul> |

## 1 Scope

This specification characterizes the IEEE 802.11a/b/g/n/ac + Bluetooth 5.2 BR/EDR/LE combo module.

## 2 Key Features

- Infineon CYW4373E inside
- Supports IEEE 802.11a/b/g/n/ac specification: Dual band 2.4 GHz and 5 GHz
- SISO with 20 MHz, 40 MHz, and 80 MHz channels
- Up to MCS9 data rates (433 Mbps)
- Supports Bluetooth specification version 5.2
- For supported Bluetooth functions, refer to [Bluetooth SIG site](#) 
- WLAN interface: SDIO 3.0, USB 2.0 (shared)
- Bluetooth interface: HCI UART, USB 2.0 (shared) and PCM
- Reference Clock: Reference clock embedded.
- Temperature Range: -40 °C to 85 °C
- Dimensions: 8.0 x 7.8 x 1.15 mm
- Weight: 0.2 g
- MSL: 3
- Surface-mount type
- RoHS compliant
- Total Fit : 343



This product is moisture sensitive. Please check the detail in [Section 17.1 Storage Condition](#) 

## 3 Ordering Information

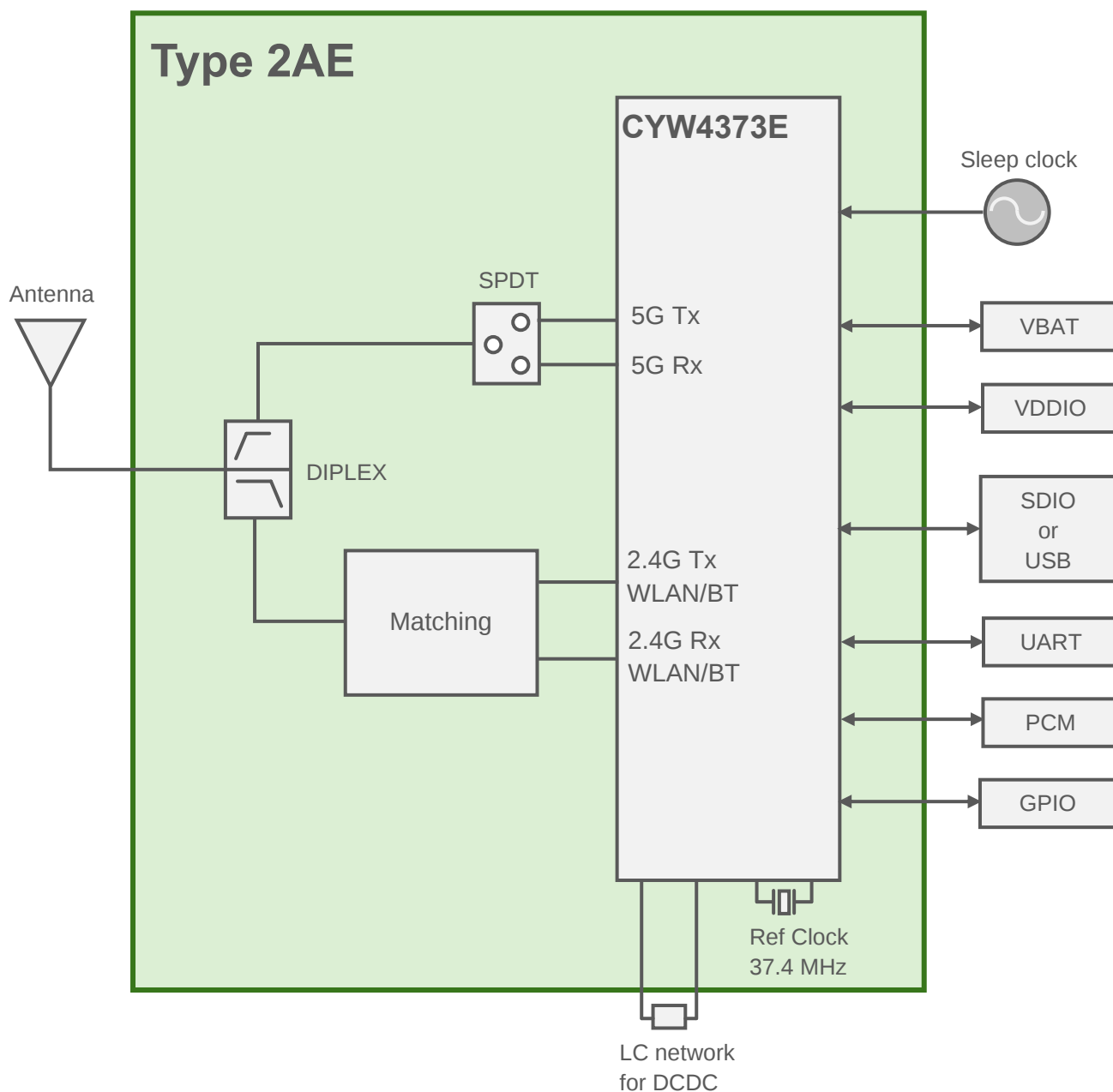
Table 2: Ordering Information

| Ordering Part Number | Description                                                                                                                 |
|----------------------|-----------------------------------------------------------------------------------------------------------------------------|
| LBEE5PK2AE-564       | Module order                                                                                                                |
| LBEE5PK2AE-SMP       | Sample module order (If module samples are not available through distribution, contact Murata referencing this part number) |
| EAR00388             | Embedded Artists Type 2AE M.2 EVB (default EVB available through distribution)                                              |

## 4 Block Diagram

Figure 1 shows the Type 2AE internal block diagram.

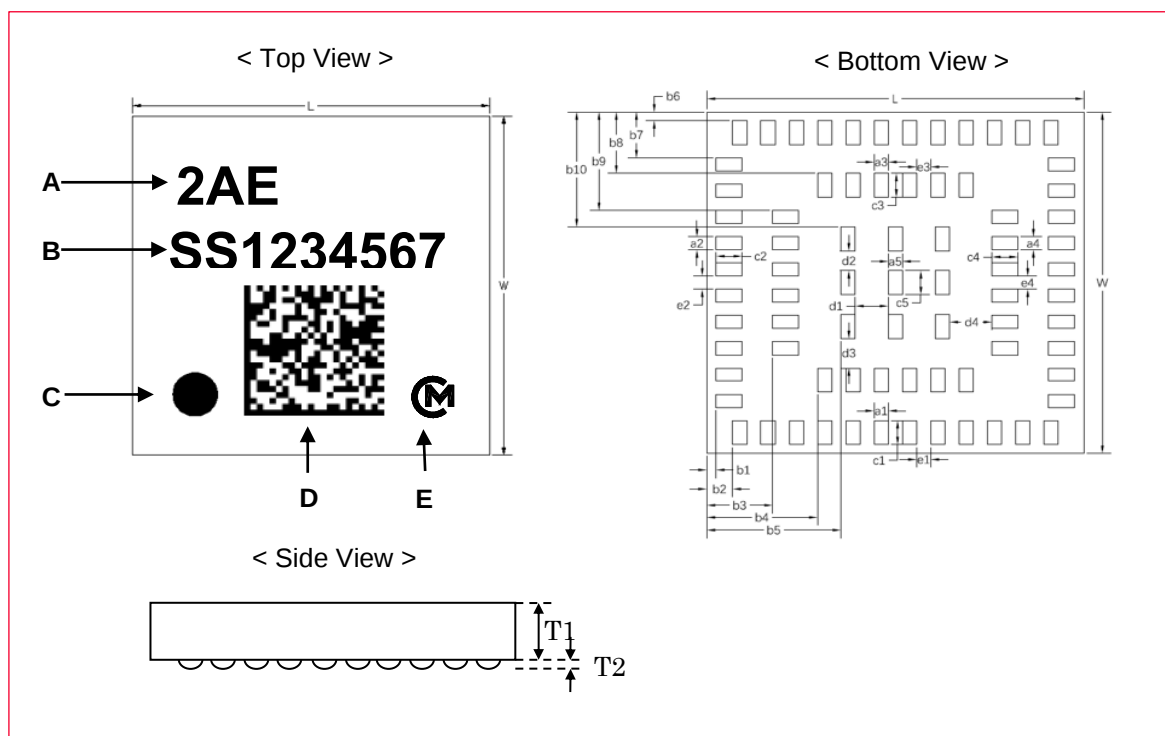
Figure 1: Block Diagram



## 5 Dimensions, Markings and Terminal Configurations

This section has information on dimensions, markings, and terminal configurations for Type 2AE.

**Figure 2: Dimensions, Markings and Terminal Configurations**



**Table 3** and **Table 4** describes the Type 2AE markings and dimensions.

**Table 3: Markings**

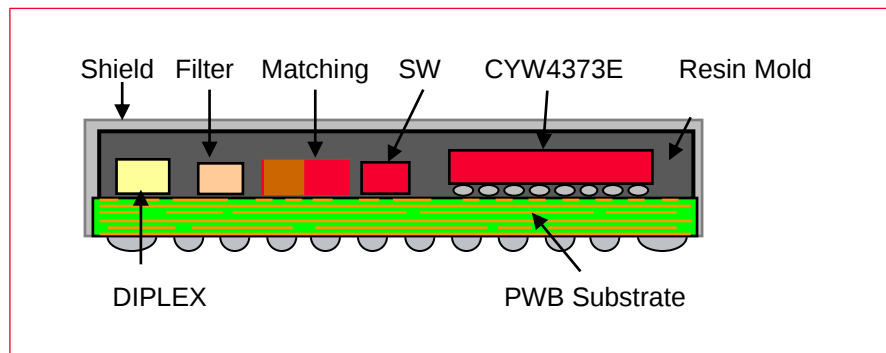
| Marking | Meaning                |
|---------|------------------------|
| A       | Module Type            |
| B       | Inspection Number      |
| C       | Pin 1 Marking          |
| D       | 2D Code (Internal Use) |
| E       | Murata Logo            |

**Table 4: Dimensions**

| Mark | Dimensions (mm) | Mark | Dimensions (mm)  | Mark | Dimensions (mm)   |
|------|-----------------|------|------------------|------|-------------------|
| L    | $8.00 \pm 0.20$ | W    | $7.80 \pm 0.20$  | T1   | 1.15 maximum      |
| a1   | $0.30 \pm 0.10$ | a2   | $0.30 \pm 0.10$  | a3   | $0.30 \pm 0.10$   |
| a4   | $0.30 \pm 0.10$ | a5   | $0.30 \pm 0.10$  | b1   | $0.30 \pm 0.15$   |
| b2   | $0.55 \pm 0.15$ | b3   | $1.50 \pm 0.15$  | b4   | $2.35 \pm 0.15$   |
| b5   | $2.85 \pm 0.15$ | b6   | $0.30 \pm 0.15$  | b7   | $1.05 \pm 0.15$   |
| b8   | $1.50 \pm 0.15$ | b9   | $2.25 \pm 0.15$  | b10  | $2.675 \pm 0.15$  |
| c1   | $0.45 \pm 0.10$ | c2   | $0.45 \pm 0.10$  | c3   | $0.45 \pm 0.10$   |
| c4   | $0.45 \pm 0.10$ | c5   | $0.45 \pm 0.10$  | d1   | $0.70 \pm 0.10$   |
| d2   | $0.55 \pm 0.10$ | d3   | $0.725 \pm 0.10$ | d4   | $0.90 \pm 0.10$   |
| e1   | $0.30 \pm 0.10$ | e2   | $0.30 \pm 0.10$  | e3   | $0.30 \pm 0.10$   |
| e4   | $0.30 \pm 0.10$ |      |                  | T2   | $0.045 \pm 0.025$ |

**Figure 3** shows the structure.

**Figure 3: Structure**



The sides of the module are GND shielded. In order to avoid contact between the GND shield and the electrodes on the mother board, please carefully evaluate the standoff before use the module.

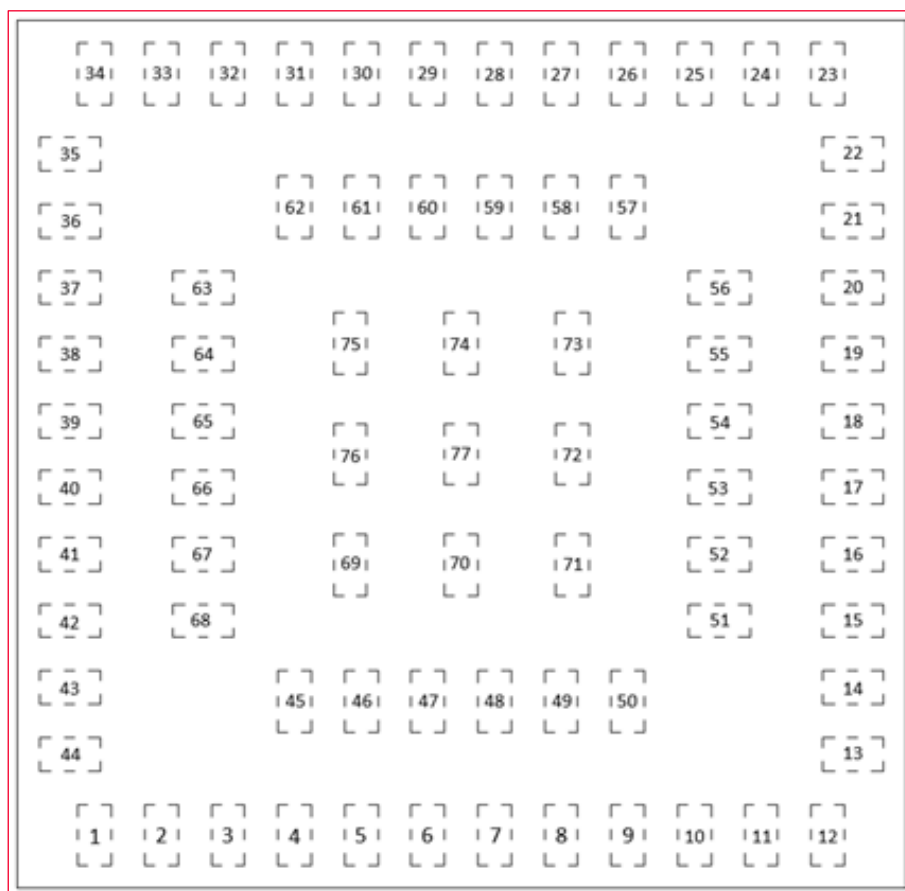
## 6 Module Pin Descriptions

This section has the pin descriptions of Type 2AE and pin assignments layout descriptions.

### 6.1 Pin Assignments

This section has the terminal configurations and pin assignments layout of Type 2AE. The pin assignment (top view) layout is shown in **Figure 4**.

**Figure 4: Pin Assignments - Top View**



**Table 5** illustrates the terminal configurations for Type 2AE.

**Table 5: Terminal Configurations**

| No. | Terminal Name | No. | Terminal Name | No. | Terminal Name | No. | Terminal Name  |
|-----|---------------|-----|---------------|-----|---------------|-----|----------------|
| 1   | GND           | 21  | GND           | 41  | GND           | 61  | NC             |
| 2   | SR_VLX        | 22  | WL_ANT        | 42  | VDDIO         | 62  | NC             |
| 3   | VBAT          | 23  | GND           | 43  | VIN_LDO       | 63  | TRST_L         |
| 4   | WL_REG_EN     | 24  | GND           | 44  | NC            | 64  | JTAG_TDI       |
| 5   | LPO_IN        | 25  | RF_SW_CTRL_5  | 45  | GPIO_1        | 65  | JTAG_TDO       |
| 6   | BT_PCM_IN     | 26  | RF_SW_CTRL_0  | 46  | USB2_DM       | 66  | JTAG_TCK/SWCLK |
| 7   | BT_PCM_CLK    | 27  | GND           | 47  | USB2_DP       | 67  | JTAG_TMS/SWDIO |
| 8   | BT_PCM_SYNC   | 28  | SDIO_CMD      | 48  | USB2_MONCDR   | 68  | BT_REG_EN      |
| 9   | BT_PCM_OUT    | 29  | SDIO_DATA_1   | 49  | USB2_AVDD33   | 69  | GND            |
| 10  | BT_UART_TXD   | 30  | SDIO_DATA_0   | 50  | USB2_RREF     | 70  | GND            |
| 11  | BT_UART_CTS_N | 31  | SDIO_DATA_3   | 51  | BT_DEV_WAKE   | 71  | GND            |
| 12  | BT_UART_RXD   | 32  | SDIO_DATA_2   | 52  | WL_HOST_WAKE  | 72  | GND            |
| 13  | BT_UART_RTS_N | 33  | SDIO_CLK      | 53  | JTAG_SEL      | 73  | GND            |
| 14  | GND           | 34  | GND           | 54  | STRAP_1       | 74  | GND            |
| 15  | NC            | 35  | NC            | 55  | STRAP_2       | 75  | GND            |
| 16  | GND           | 36  | NC            | 56  | STRAP_0       | 76  | GND            |
| 17  | BT_HOST_WAKE  | 37  | NC            | 57  | GND           | 77  | GND            |
| 18  | BT_GPIO_2     | 38  | NC            | 58  | NC            |     |                |
| 19  | BT_GPIO_3     | 39  | NC            | 59  | NC            |     |                |
| 20  | BT_GPIO_5     | 40  | NC            | 60  | NC            |     |                |

## 6.2 Pin Descriptions

**Table 6** describes Type 2AE pin descriptions.

**Table 6: Pin Descriptions**

| No. | Terminal Name | Type | Connection to IC Terminal | Description                                                                                                                                                                                                                                                                               |
|-----|---------------|------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1   | GND           |      |                           |                                                                                                                                                                                                                                                                                           |
| 2   | SR_VLX        | PO   | SR_VLX                    | CBUCK switching regulator output. Refer to Reference circuit for details of the inductor and capacitor required in this output.                                                                                                                                                           |
| 3   | VBAT          | PI   | SR_VDDBAT5V/LDO_VDDBAT5V  | Supply to internal Power source of VBAT.                                                                                                                                                                                                                                                  |
| 4   | WL_REG_EN     | I    | WL_REG_ON                 | Used by PMU to power-up or power down the internal CYW4373E regulators used by the WLAN section. Also, when de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming. |
| 5   | LPO_IN        | I    | LPO_IN                    | External Sleep clock input (32.768 kHz)                                                                                                                                                                                                                                                   |
| 6   | BT_PCM_IN     | I    | BT_PCM_IN                 | PCM data input.                                                                                                                                                                                                                                                                           |
| 7   | BT_PCM_CLK    | I/O  | BT_PCM_CLK                | PCM clock; can be master(output) or slave(input).                                                                                                                                                                                                                                         |
| 8   | BT_PCM_SYNC   | I/O  | BT_PCM_SYNC               | PCM sync; can be master(output) or slave(input).                                                                                                                                                                                                                                          |
| 9   | BT_PCM_OUT    | O    | BT_PCM_OUT                | PCM data output.                                                                                                                                                                                                                                                                          |

| No. | Terminal Name | Type | Connection to IC Terminal                                   | Description                                                                                                                                                                               |
|-----|---------------|------|-------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 10  | BT_UART_TXD   | O    | BT_UART_TXD                                                 | UART serial output. Serial data output for the HCI UART interface.                                                                                                                        |
| 11  | BT_UART_CTS_N | I    | BT_UART_CTS_N                                               | UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.                                                                                                           |
| 12  | BT_UART_RXD   | I    | BT_UART_RXD                                                 | UART serial input. Serial data input for the HCI UART interface.                                                                                                                          |
| 13  | BT_UART_RTS_N | O    | BT_UART_RTS_N                                               | UART request-to-send. Active - low request - to-send signal for the HCI UART interface.                                                                                                   |
| 14  | GND           |      |                                                             |                                                                                                                                                                                           |
| 15  | NC            |      |                                                             |                                                                                                                                                                                           |
| 16  | GND           |      |                                                             |                                                                                                                                                                                           |
| 17  | BT HOST WAKE  | I/O  | BT HOST WAKE                                                | Host wake-up. Signal from the CYW4373E to the host indicating that the CYW4373E requires attention. The polarity of this signal is software configurable and can be asserted high or low. |
| 18  | BT_GPIO_2     | I/O  | BT_GPIO_2                                                   | Bluetooth general-purpose I/O.                                                                                                                                                            |
| 19  | BT_GPIO_3     | I/O  | BT_GPIO_3                                                   | Bluetooth general-purpose I/O.                                                                                                                                                            |
| 20  | BT_GPIO_5     | I/O  | BT_GPIO_5                                                   | Bluetooth general-purpose I/O.                                                                                                                                                            |
| 21  | GND           |      |                                                             |                                                                                                                                                                                           |
| 22  | WL_ANT        | RF   |                                                             | RF output for WLAN/BT                                                                                                                                                                     |
| 23  | GND           |      |                                                             |                                                                                                                                                                                           |
| 24  | GND           |      |                                                             |                                                                                                                                                                                           |
| 25  | RF_SW_CTRL_5  | O    | RF_SW_CTRL_5                                                | Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.                                                                                   |
| 26  | RF_SW_CTRL_0  | O    | RF_SW_CTRL_0                                                | Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.                                                                                   |
| 27  | GND           | -    | -                                                           |                                                                                                                                                                                           |
| 28  | SDIO_CMD      | I/O  | SDIO_CMD                                                    | SDIO command line                                                                                                                                                                         |
| 29  | SDIO_DATA_1   | I/O  | SDIO_DATA_1                                                 | SDIO data line 1                                                                                                                                                                          |
| 30  | SDIO_DATA_0   | I/O  | SDIO_DATA_0                                                 | SDIO data line 0                                                                                                                                                                          |
| 31  | SDIO_DATA_3   | I/O  | SDIO_DATA_3                                                 | SDIO data line 3                                                                                                                                                                          |
| 32  | SDIO_DATA_2   | I/O  | SDIO_DATA_2                                                 | SDIO data line 2                                                                                                                                                                          |
| 33  | SDIO_CLK      | I    | SDIO_CLK                                                    | SDIO clock input                                                                                                                                                                          |
| 34  | GND           |      |                                                             |                                                                                                                                                                                           |
| 35  | NC            |      |                                                             |                                                                                                                                                                                           |
| 36  | NC            |      |                                                             |                                                                                                                                                                                           |
| 37  | NC            |      |                                                             |                                                                                                                                                                                           |
| 38  | NC            |      |                                                             |                                                                                                                                                                                           |
| 39  | NC            |      |                                                             |                                                                                                                                                                                           |
| 40  | NC            |      |                                                             |                                                                                                                                                                                           |
| 41  | GND           |      |                                                             |                                                                                                                                                                                           |
| 42  | VDDIO         | PI   | VDDIO/BT_VDDO                                               | Supply for PMU, BT, WLAN, SDIO.                                                                                                                                                           |
| 43  | VIN_LDO       | PI   | LDO_VDD1P5/WRF_AFE_VDD1P35/WRF_XTAL_VDD1P35/WRF_PMU_VDD1P35 | Input for:<br>LDO_VDD1P5/WRF_AFE_VDD1P35/<br>WRF_XTAL_VDD1P35/WRF_PMU_VDD1P35                                                                                                             |
| 44  | NC            |      |                                                             |                                                                                                                                                                                           |
| 45  | GPIO_1        | I/O  | GPIO_1                                                      | Programmable GPIO Pin                                                                                                                                                                     |
| 46  | USB2_DM       | I/O  | USB2_DM                                                     | Data minus of shared USB2.0 port.                                                                                                                                                         |

| No. | Terminal Name  | Type | Connection to IC Terminal | Description                                                                                                                                                                                                                                                                                                                                 |
|-----|----------------|------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 47  | USB2_DP        | I/O  | USB2_DP                   | Data plus of shared USB2.0 port.                                                                                                                                                                                                                                                                                                            |
| 48  | USB2_MONCDR    | O    | USB2_MONCDR               | CDR monitor for debug.                                                                                                                                                                                                                                                                                                                      |
| 49  | USB2_AVDD33    | PI   | USB2_AVDD33               | Power Supply for shared USB2.0.<br>When VBAT is between 3.6V to 4.8V connect to external 3.3V power supply.<br>When VBAT is 3.3V connect directly to VBAT.                                                                                                                                                                                  |
| 50  | USB2_RREF      | I/O  | USB2_RREF                 | Bandgap reference resistor.<br>4.75 kΩ +/-1% for USB.<br>DNI for SDIO.                                                                                                                                                                                                                                                                      |
| 51  | BT_DEV_WAKE    | I    | BT_DEV_WAKE               | Bluetooth device wake-up: Signal from the host to the CYW4373E indicating that the host requires attention.<br>The polarity of this signal is software configurable and can be asserted high or low.                                                                                                                                        |
| 52  | WL_HOST_WAKE   | O    | GPIO_0                    | Programmable GPIO Pin                                                                                                                                                                                                                                                                                                                       |
| 53  | JTAG_SEL       | I    | JTAG_SEL                  | JTAG select. This pin should be kept NO CONNECT or connect to ground if the JTAG interface is not used. It must be high to select SWD OR JTAG. When JTAG_SEL = 1: <ul style="list-style-type: none"> <li>• GPIO_2 is TCK</li> <li>• GPIO_3 is TMS</li> <li>• GPIO_4 is TDIO</li> <li>• GPIO_5 is TDO</li> <li>• GPIO_6 is TRST_L</li> </ul> |
| 54  | STRAP_1        | I    | STRAP_1                   | 0: SDIO only                                                                                                                                                                                                                                                                                                                                |
| 55  | STRAP_2        | I    | STRAP_2                   | USB_DISABLE <ul style="list-style-type: none"> <li>• 1: USB disable</li> <li>• 0: USB enable</li> </ul>                                                                                                                                                                                                                                     |
| 56  | STRAP_0        | I    | STRAP_0                   | SDIO_PADVDDIO sel                                                                                                                                                                                                                                                                                                                           |
| 57  | GND            |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 58  | NC             |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 59  | NC             |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 60  | NC             |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 61  | NC             |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 62  | NC             |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 63  | TRST_L         | I/O  | GPIO_6                    | GPIO_6 is TRST_L                                                                                                                                                                                                                                                                                                                            |
| 64  | JTAG_TDI       | I/O  | GPIO_4                    | GPIO_4 is TDI                                                                                                                                                                                                                                                                                                                               |
| 65  | JTAG_TDO       | I/O  | GPIO_5                    | GPIO_5 is TDO                                                                                                                                                                                                                                                                                                                               |
| 66  | JTAG_TCK/SWCLK | I/O  | GPIO_2                    | GPIO_2 is TCK/SWCLK                                                                                                                                                                                                                                                                                                                         |
| 67  | JTAG_TMS/SWDIO | I/O  | GPIO_3                    | GPIO_3 is TMS/SWDIO                                                                                                                                                                                                                                                                                                                         |
| 68  | BT_REG_EN      | I    | BT_REG_ON                 | Used by PMU to power-up or power down the internal CYW4373E regulators used by the Bluetooth section. Also, when de-asserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.                                         |
| 69  | GND            |      |                           |                                                                                                                                                                                                                                                                                                                                             |
| 70  | GND            |      |                           |                                                                                                                                                                                                                                                                                                                                             |

| No. | Terminal Name | Type | Connection to IC Terminal | Description |
|-----|---------------|------|---------------------------|-------------|
| 71  | GND           |      |                           |             |
| 72  | GND           |      |                           |             |
| 73  | GND           |      |                           |             |
| 74  | GND           |      |                           |             |
| 75  | GND           |      |                           |             |
| 76  | GND           |      |                           |             |
| 77  | GND           |      |                           |             |

## 6.3 SDIO Pin Descriptions

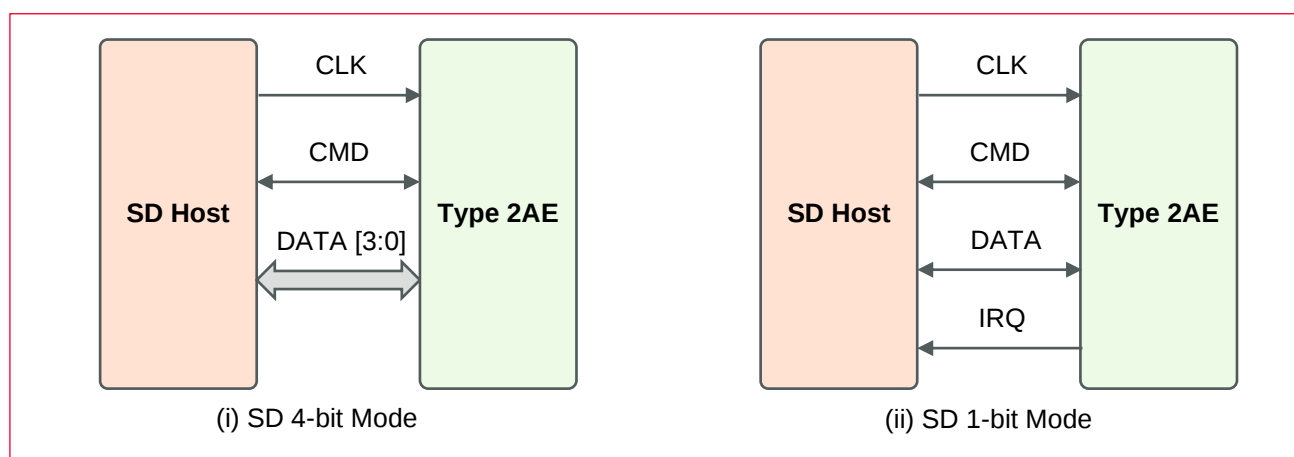
**Table 7** shows the SDIO pin descriptions.

**Table 7: SDIO Pin Descriptions**

| No. | Pin Name | (i) SD 4-bit Mode |                        | (ii) SD 1-bit Mode |              |
|-----|----------|-------------------|------------------------|--------------------|--------------|
| 33  | SDIO_CLK | CLK               | Clock                  | CLK                | Clock        |
| 30  | SDIO_D0  | DATA0             | Data line 0            | DATA               | Data line    |
| 29  | SDIO_D1  | DATA1             | Data line 1 /Interrupt | IRQ                | Interrupt    |
| 32  | SDIO_D2  | DATA2             | Data line 2            | NC                 | Not used     |
| 31  | SDIO_D3  | DATA3             | Data line 3            | NC                 | Not used     |
| 28  | SDIO_CMD | CMD               | Command line           | CMD                | Command line |

Figure 5 shows the signal connections to the SDIO modes.

**Figure 5: SDIO Modes**



## 7 Absolute Maximum Ratings

The absolute minimum and maximum ratings are shown in **Table 8**.

**Table 8: Ratings**

| Parameter           |       | Minimum | Maximum | Unit |
|---------------------|-------|---------|---------|------|
| Storage Temperature |       | -40     | +85     | °C   |
| Supply Voltage      | VBAT  | -0.5    | 5.5     | V    |
|                     | VDDIO | -0.5    | 3.9     | V    |



Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

## 8 Operating Conditions

### 8.1 Operating Conditions

The operating conditions are shown **Table 9**.

**Table 9: Operating Conditions**

| Parameter                                |       | Minimum           | Typical | Maximum          | Unit |
|------------------------------------------|-------|-------------------|---------|------------------|------|
| Operating Temperature Range <sup>1</sup> |       | -40               | +25     | +85              | °C   |
| Supply Voltage                           | VBAT  | 3.13 <sup>2</sup> | 3.3     | 3.5 <sup>3</sup> | V    |
|                                          | VDDIO | 1.62              | 1.8     | 1.98             | V    |
|                                          |       | 2.97              | 3.3     | 3.63             | V    |

## 9 External Sleep Clock Requirements

External LPO signal requirements are shown in **Table 10**.

**Table 10: External LPO Signal Requirements**

| Parameter                              | External LPO Clock      | Unit    |
|----------------------------------------|-------------------------|---------|
| Nominal input frequency                | 32.768                  | kHz     |
| Frequency accuracy                     | +/-200                  | ppm     |
| Duty cycle                             | 30-70                   | %       |
| Input signal amplitude                 | 200 - 3300              | mV, p-p |
| Signal type                            | Square-wave or sinewave |         |
| Input impedance <sup>4</sup>           | > 100k                  | Ω       |
|                                        | < 5                     | pF      |
| Clock jitter (during initial start-up) | <10,000                 | ppm     |

<sup>1</sup> Functionality is guaranteed but specifications require derating at extreme temperatures.

<sup>2</sup> CYW4373E is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for VBAT = 3.3V +/- 5%.

<sup>3</sup> The maximum continuous voltage is 4.8V

<sup>4</sup> When the power is applied or switched off.

## 10 Strapping Options

Table 11 has the strapping options for Type 2AE module pins.

**Table 11: Strapping Options**

| Mode Select | STRAP_2 | STRAP_1 | STRAP_0                                                                                      |
|-------------|---------|---------|----------------------------------------------------------------------------------------------|
| USB         | 0       | 0       | 0                                                                                            |
| SDIO only   | 1       | 0       | <ul style="list-style-type: none"> <li>0 = SDIO is 3.3V</li> <li>1 = SDIO is 1.8V</li> </ul> |

## 11 Power-On Sequence

This section describes the power-on sequences along with their parameters.

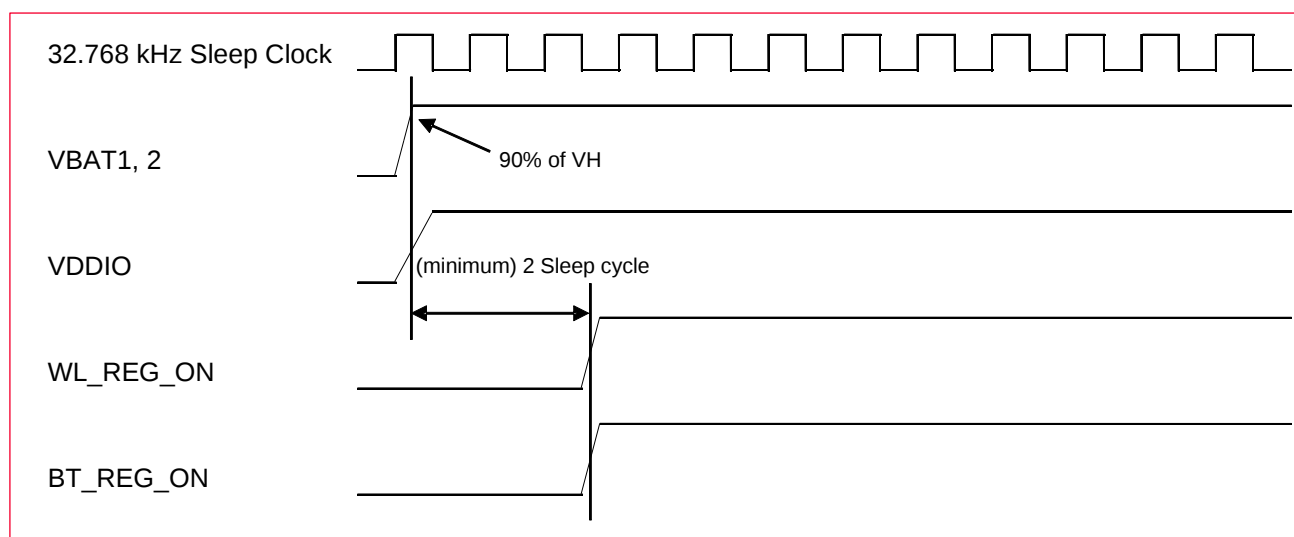
### 11.1 Power-On Sequence for WLAN ON and BT ON

For power-on sequence for WLAN ON and BT ON:

- VBAT should not rise 10-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

**Figure 6** shows the power-on sequence for WLAN ON and BT ON.

**Figure 6: Power-On Sequence - WLAN ON and BT ON**



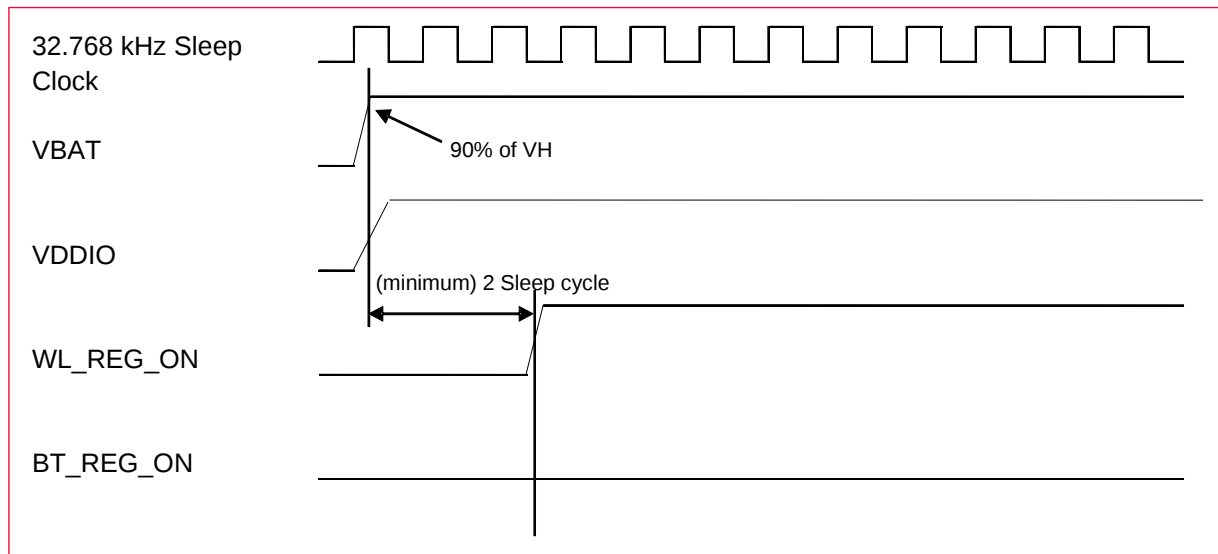
## 11.2 Power-On Sequence for WLAN ON and BT OFF

For power-on sequence for WLAN ON and BT OFF:

- VBAT should not rise 10-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

**Figure 7** shows the power-on sequence for WLAN ON and BT OFF.

**Figure 7: Power-On Sequence - WLAN ON and BT OFF**

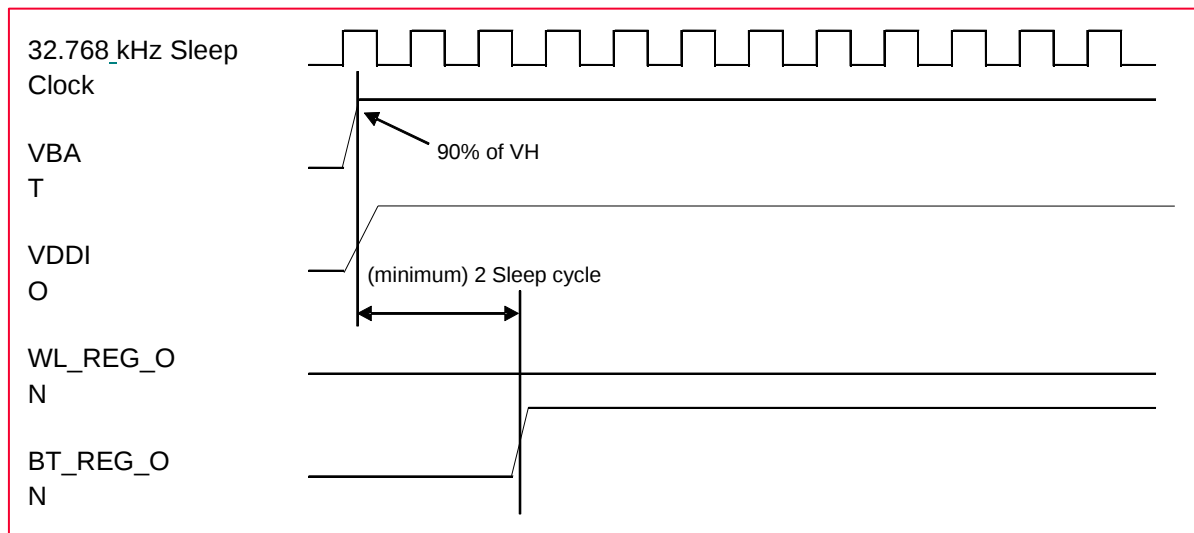


## 11.3 Power-On Sequence for WLAN OFF and BT ON

For power-on sequence for WLAN OFF and BT ON:

- VBAT should not rise 10-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

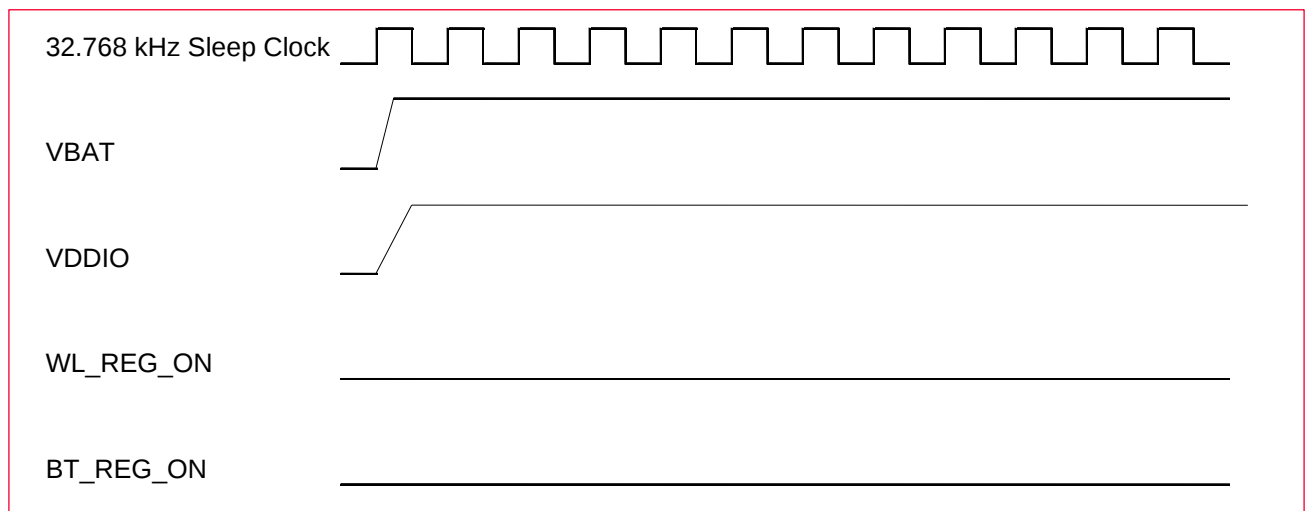
**Figure 8** shows the power-on sequence for WLAN OFF and BT ON.

**Figure 8: Power-On Sequence - WLAN OFF and BT ON**

## 11.4 Power-On Sequence for WLAN OFF and BT OFF

For power-on sequence for WLAN OFF and BT OFF:

- VBAT should not rise 10-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

**Figure 9: Power-On Sequence - WLAN OFF and BT OFF**

## 12 Digital I/O Requirements

This section describes the digital input/output pins and related parameters.

### 12.1 Digital I/O Pins

**Table 12** describes the digital input/output pins and related parameters.

**Table 12: Digital I/O Pins**

| Digital I/O Pins               | Symbol   | Minimum             | Typical | Maximum             | Unit |
|--------------------------------|----------|---------------------|---------|---------------------|------|
| For VDDIO = 1.8V               |          |                     |         |                     |      |
| • Input high voltage           | $V_{IH}$ | $0.65 \times VDDIO$ |         |                     | V    |
| • Input low voltage            | $V_{IL}$ |                     |         | $0.35 \times VDDIO$ | V    |
| • Output high voltage @ 2.0 mA | $V_{OH}$ | $VDDIO - 0.45$      |         |                     | V    |
| • Output low voltage @ 2.0 mA  | $V_{OL}$ |                     |         | 0.45                | V    |
| For VDDIO = 3.3 V              |          |                     |         |                     |      |
| • Input high voltage           | $V_{IH}$ | 2.00                |         |                     | V    |
| • Input low voltage            | $V_{IL}$ |                     |         | 0.80                | V    |
| • Output high voltage @ 2.0 mA | $V_{OH}$ | $VDDIO - 0.40$      |         |                     | V    |
| • Output low voltage @ 2.0 mA  | $V_{OL}$ |                     |         | 0.40                | V    |

### 12.2 RF Switch Control Output Pins

**Table 13** provides information about the RF switch control output pins.

**Table 13: RF Switch Control Output Pins**

| RF Switch Control Output Pins  | Symbol    | Minimum        | Typical | Maximum | Unit |
|--------------------------------|-----------|----------------|---------|---------|------|
| For VDDIO_RF = 3.3V:           |           |                |         |         |      |
| • Output high voltage @ 2.0 mA | $V_{OH}$  | $VDDIO - 0.40$ |         |         | V    |
| • Output low voltage @ 2.0 mA  | $V_{OL}$  |                |         | 0.40    | V    |
| Output capacitance             | $C_{out}$ |                |         | 5       | pF   |

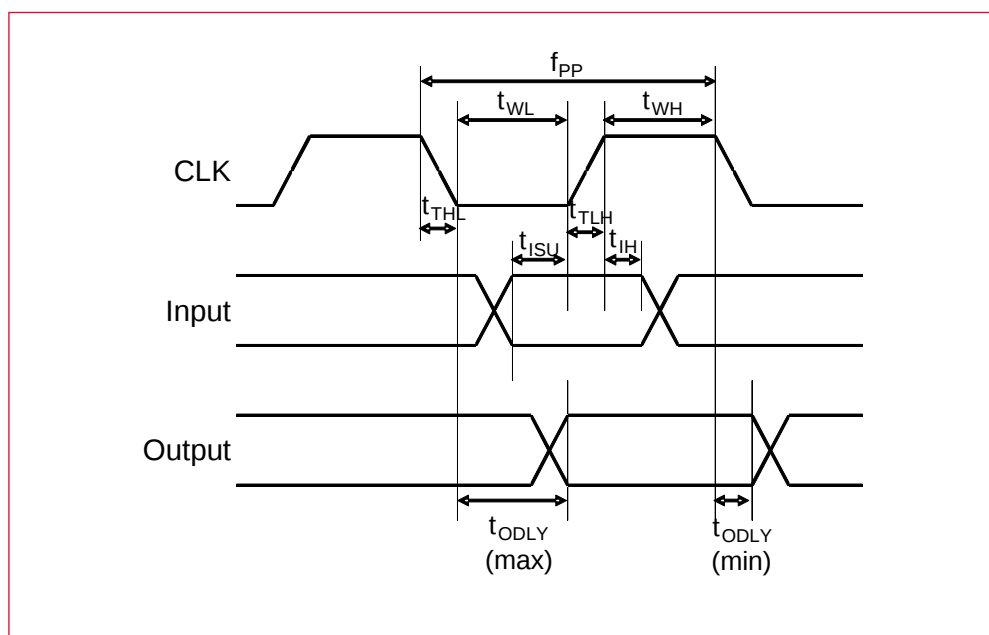
## 13 Interface Timing

This section describes the interface timing for SDIO, Bluetooth, and PCM, their speed modes, related parameters, and graphs.

### 13.1 SDIO Timing - Default Mode

The SDIO default timing diagram and data are shown in **Figure 10** and **Table 14**.

**Figure 10: SDIO Timing Diagram - Default Mode**



**Table 14: SDIO Timing Data - Default Mode**

| Parameter                                                                 | Symbol     | Minimum | Typical | Maximum | Unit |
|---------------------------------------------------------------------------|------------|---------|---------|---------|------|
| <b>Clock CLK (All values are referred to minimum VIH and maximum VIL)</b> |            |         |         |         |      |
| Frequency-Data Transfer Mode                                              | $f_{PP}$   | 0       |         | 25      | MHz  |
| Frequency-Identification Mode                                             | $f_{OD}$   | 0       |         | 400     | kHz  |
| Clock Low Time                                                            | $t_{WL}$   | 10      |         |         | ns   |
| Clock High Time                                                           | $t_{WH}$   | 10      |         |         | ns   |
| Clock Rise Time                                                           | $t_{TLH}$  |         |         | 10      | ns   |
| Clock Fall Time                                                           | $t_{THL}$  |         |         | 10      | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>                               |            |         |         |         |      |
| Input Setup Time                                                          | $t_{ISU}$  | 5       |         |         | ns   |
| Input Hold Time                                                           | $t_{IH}$   | 5       |         |         | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>                              |            |         |         |         |      |
| Output Delay Time-Data Transfer Mode                                      | $t_{ODLY}$ | 0       |         | 14      | ns   |
| Output Delay Time-Identification Mode                                     | $t_{ODLY}$ | 0       |         | 50      | ns   |

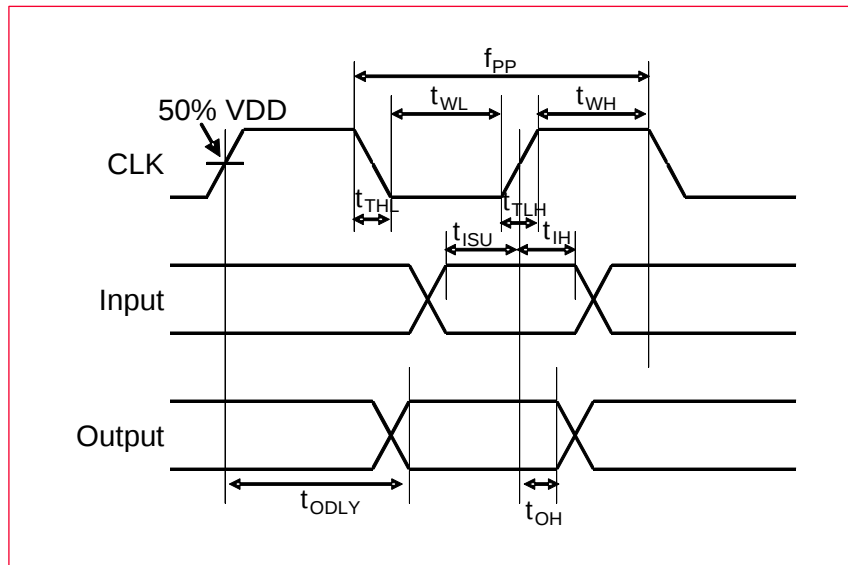


- Timing is based on  $CL < 40$  pF load on CMD and Data.
- Minimum ( $V_{ih}$ ) =  $0.7 \cdot V_{DDIO}$  and maximum ( $V_{il}$ ) =  $0.2 \cdot V_{DDIO}$ .

## 13.2 SDIO Timing - High Speed Mode

The SDIO high speed timing diagram and data are shown in **Figure 11** and **Table 15**.

**Figure 11: SDIO Timing Diagram – High Speed Mode**



**Table 15: SDIO Timing Data - High Speed Mode**

| Parameter                                                                                                 | Symbol     | Minimum | Typical | Maximum | Unit |
|-----------------------------------------------------------------------------------------------------------|------------|---------|---------|---------|------|
| <b>Clock CLK (All values are referred to minimum <math>V_{ih}</math> and maximum <math>V_{il}</math>)</b> |            |         |         |         |      |
| Frequency-Data Transfer Mode                                                                              | $f_{PP}$   | 0       |         | 50      | MHz  |
| Frequency-Identification Mode                                                                             | $f_{OD}$   | 0       |         | 400     | kHz  |
| Clock Low Time                                                                                            | $t_{WL}$   | 7       |         |         | ns   |
| Clock High Time                                                                                           | $t_{WH}$   | 7       |         |         | ns   |
| Clock Rise Time                                                                                           | $t_{TLH}$  |         |         | 3       | ns   |
| Clock Fall Time                                                                                           | $t_{THL}$  |         |         | 3       | ns   |
| <b>Inputs: CMD, DAT (referenced to CLK)</b>                                                               |            |         |         |         |      |
| Input Setup Time                                                                                          | $t_{ISU}$  | 6       |         |         | ns   |
| Input Hold Time                                                                                           | $t_{IH}$   | 2       |         |         | ns   |
| <b>Outputs: CMD, DAT (referenced to CLK)</b>                                                              |            |         |         |         |      |
| Output Delay Time-Data Transfer Mode                                                                      | $t_{ODLY}$ |         |         | 14      | ns   |
| Output Hold time                                                                                          | $t_{OH}$   | 2.5     |         |         | ns   |
| Total System Capacitance (each line)                                                                      | CL         |         |         | 40      | pF   |



- Timing is based on  $CL < 40$  pF load on CMD and Data.
- Minimum ( $V_{ih}$ ) =  $0.7 \cdot V_{DDIO}$  and maximum ( $V_{il}$ ) =  $0.2 \cdot V_{DDIO}$ .

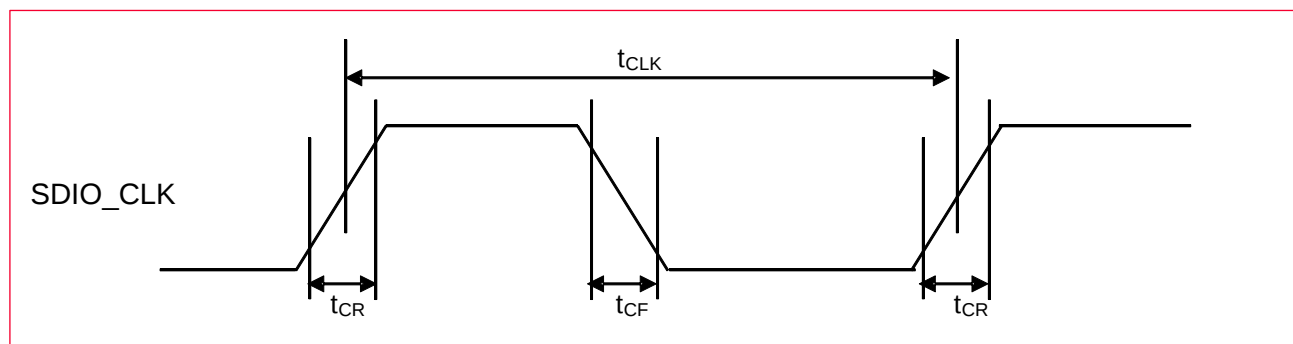
## 13.3 SDIO BUS Timing Specifications in SDR Mode

This section describes the SDIO BUS timing specifications in SDR Mode.

### 13.3.1 Clock Timing

The clock timing diagram and parameters are shown in **Figure 12** and **Table 16**.

**Figure 12: Clock Timing Diagram - SDR Mode**

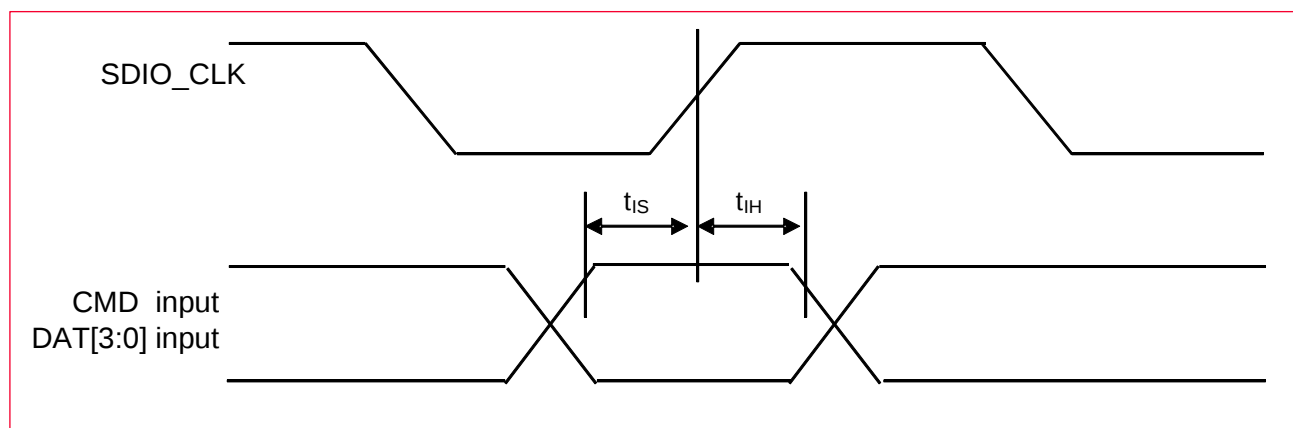


**Table 16: Clock Timing Parameters - SDR Mode**

| Parameter        | Symbol           | Minimum | Maximum              | Unit | Comments                                                                                                                       |
|------------------|------------------|---------|----------------------|------|--------------------------------------------------------------------------------------------------------------------------------|
|                  | $t_{CLK}$        | 40      |                      | ns   | SDR12 mode                                                                                                                     |
|                  |                  | 20      |                      | ns   | SDR25 mode                                                                                                                     |
|                  |                  | 10      |                      | ns   | SDR50 mode                                                                                                                     |
|                  |                  | 4.8     |                      | ns   | SDR104 mode                                                                                                                    |
|                  | $t_{CR}, t_{CF}$ |         | $0.2 \times t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 2.00$ ns (maximum) @ 100 MHz, cCARD = 10 pF<br>$t_{CR}, t_{CF} < 0.96$ ns (maximum) @ 208 MHz, cCARD = 10 pF |
| Clock duty Cycle |                  | 30      | 70                   | %    |                                                                                                                                |

### 13.3.2 Card Input Timing

The card input timing diagram and parameters are shown in **Figure 13** and **Table 17**.

**Figure 13: Card Input Timing Diagram - SDR Mode****Table 17: Card Input Timing Parameters - SDR Mode**

| Symbol             | Minimum | Maximum | Unit | Comments                    |
|--------------------|---------|---------|------|-----------------------------|
| <b>SDR104 Mode</b> |         |         |      |                             |
| $t_{IS}$           | 1.4     |         | ns   | cCARD = 10 pF, VCT = 0.975V |
| $t_{IH}$           | 0.8     |         | ns   | cCARD = 5 pF, VCT = 0.975V  |
| <b>SDR50 Mode</b>  |         |         |      |                             |
| $t_{IS}$           | 3.0     |         | ns   | cCARD = 10 pF, VCT = 0.975V |
| $t_{IH}$           | 0.8     |         | ns   | cCARD = 5 pF, VCT = 0.975V  |

### 13.3.3 Card Output Timing

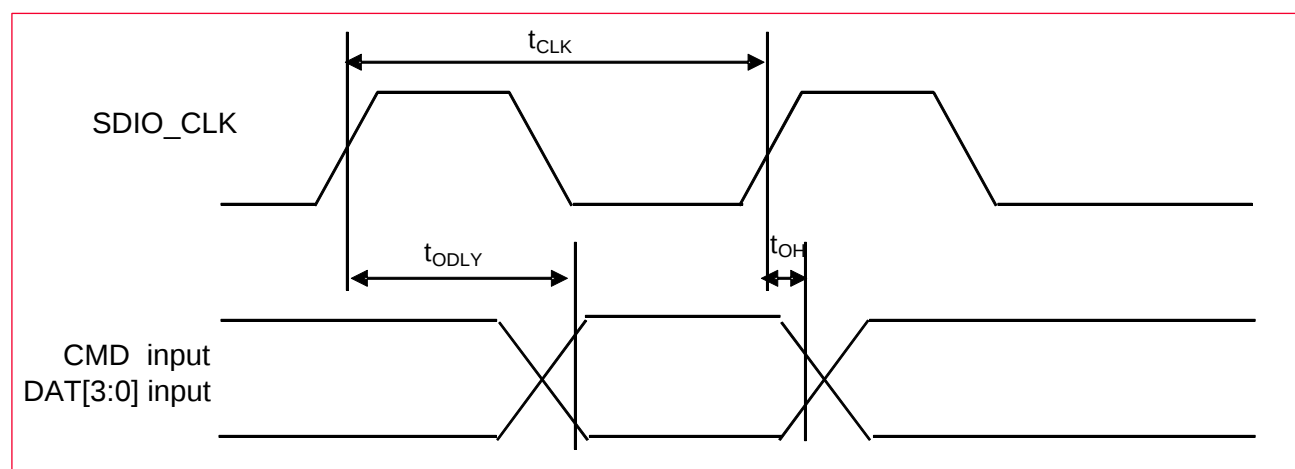
This section describes SDIO bus output timing.

#### 13.3.3.1 SDIO Bus Output Timing - SDR Modes up to 100 MHz

SDIO bus output timing diagram and parameters at SDR modes up to 100 MHz are shown in **Figure 14** and

Table 18 respectively.

Figure 14: SDIO Bus Output Timing Diagram - SDR Modes up to 100 MHz

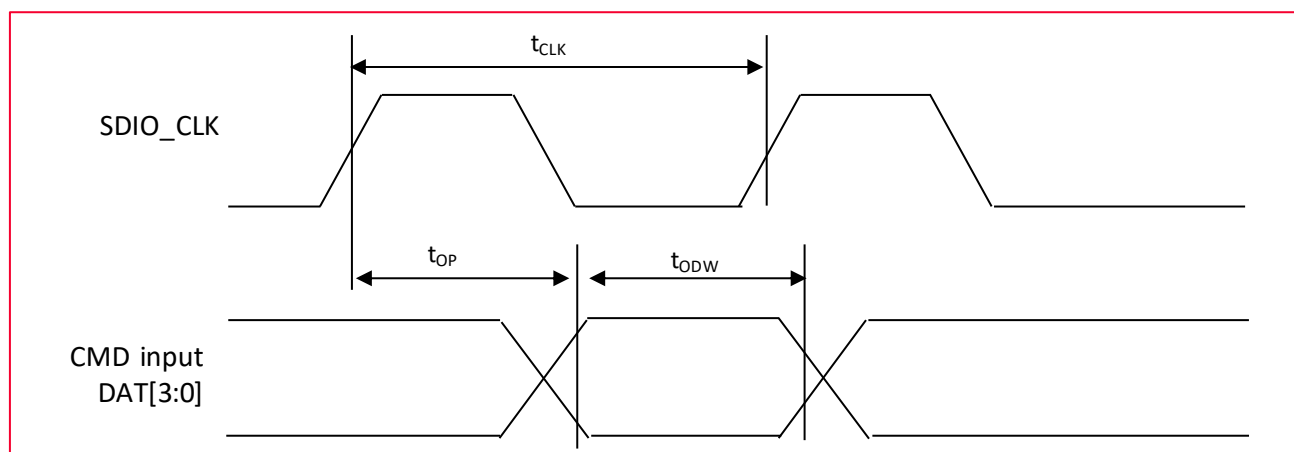


**Table 18: SDIO Bus Output Timing Parameters - SDR Modes up to 100 MHz**

| Symbol     | Minimum | Maximum | Unit | Comments                                                      |
|------------|---------|---------|------|---------------------------------------------------------------|
| $t_{ODLY}$ |         | 7.5     | ns   | $t_{CLK} \geq 10$ ns CL = 30 pF using driver type B for SDR50 |
| $t_{ODLY}$ |         | 14.0    | ns   | $t_{CLK} \geq 20$ ns CL = 40 pF using for SDR12, SDR25        |
| $t_{OH}$   | 1.5     |         | ns   | Hold time at the $t_{ODLY}(\min)$ CL = 15 pF                  |

### 13.3.3.2 SDIO Bus Output Timing - SDR Modes 100 MHz to 208 MHz

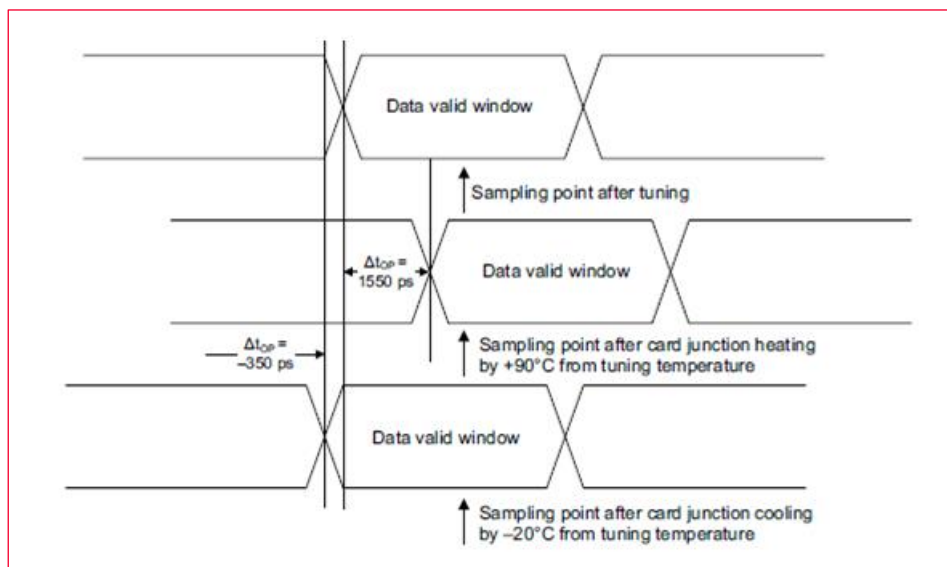
SDIO bus output timing diagram and parameters at SDR modes 100 MHz to 208 MHz are shown in **Figure 15** and **Table 19** respectively.

**Figure 15: SDIO Bus Output Timing Diagram - SDR Modes 100 MHz to 208 MHz****Table 19: SDIO Bus Output Timing Parameters - SDR Modes 100 MHz to 208 MHz**

| Symbol          | Minimum | Maximum | Unit | Comments                                        |
|-----------------|---------|---------|------|-------------------------------------------------|
| $t_{OP}$        | 0       | 2       | UI   | Card output phase                               |
| $\Delta t_{OP}$ | -350    | +1550   | ps   | Delay variation due to temp change after tuning |
| $t_{ODW}$       | 0.60    |         | UI   | $t_{ODW} = 2.88$ ns @ 208 MHz                   |

- $\Delta t_{OP} = +1550$  ps for junction temperature of  $\Delta t_{OP} = 90$  °C during operation.
- $\Delta t_{OP} = -350$  ps for junction temperature of  $\Delta t_{OP} = -20$  °C during operation.
- $\Delta t_{OP} = +2600$  ps for junction temperature of  $\Delta t_{OP} = -20$  °C to +125 °C during operation

**Figure 16** shows  $\Delta t_{OP}$  consideration for variable data window at SDR 104 mode.

Figure 16:  $\Delta t_{op}$  Consideration for Variable Data Window - SDR 104 Mode

## 13.4 SDIO Timing Specifications in DDR50 Mode

This section describes SDIO clock timing and SDIO data timing.

### 13.4.1 SDIO Clock Timing

This section provides information about SDIO clock timing at DDR50 mode. The diagram and parameters are shown in **Figure 17** and **Table 20** respectively.

Figure 17: SDIO Clock Timing Diagram - DDR50 Mode

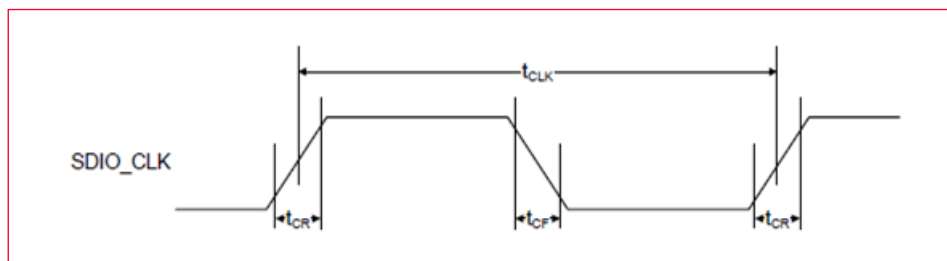


Table 20: SDIO Clock Timing Parameters - DDR50 Mode

| Parameter        | Symbol           | Minimum | Maximum              | Unit | Comments                                                           |
|------------------|------------------|---------|----------------------|------|--------------------------------------------------------------------|
|                  | $t_{CLK}$        | 20      |                      | ns   | DDR50 mode                                                         |
|                  | $t_{CR}, t_{CF}$ |         | $0.2 \times t_{CLK}$ | ns   | $t_{CR}, t_{CF} < 4.00 \text{ ns (max)}$ @ 50MHz,<br>cCard = 10 pF |
| Clock duty cycle |                  | 45      | 55                   | %    |                                                                    |

### 13.4.2 SDIO Data Timing

This section provides information about SDIO data timing at DDR50 mode. The diagram and parameters are shown in **Figure 18** and **Table 21** respectively.

Figure 18: SDIO Data Timing Diagram - DDR50 Mode

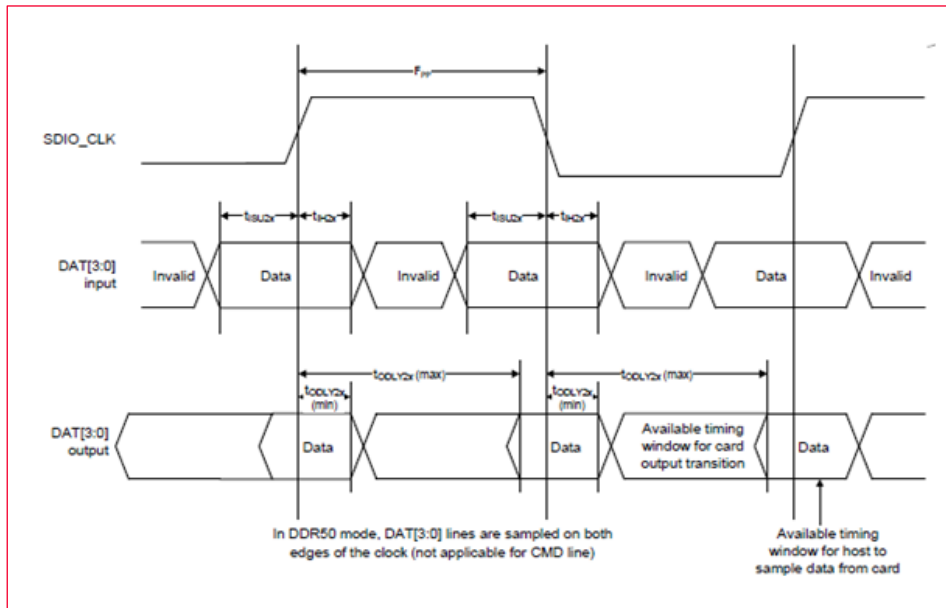


Table 21: SDIO Data Timing Parameters - DDR50 Mode

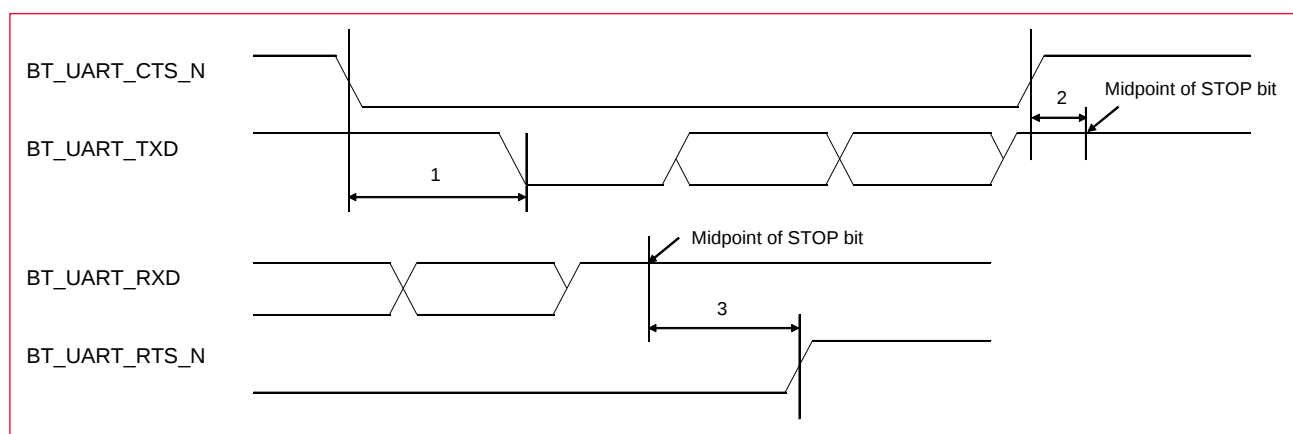
| Parameter         | Symbol              | Minimum | Maximum | Unit | Comments               |
|-------------------|---------------------|---------|---------|------|------------------------|
| <b>Input CMD</b>  |                     |         |         |      |                        |
| Input setup time  | t <sub>SU</sub>     | 6       |         | ns   | Ccard < 10 pF (1 card) |
| Input hold time   | t <sub>IH</sub>     | 0.8     |         | ns   | Ccard < 10 pF (1 card) |
| <b>Output CMD</b> |                     |         |         |      |                        |
| Output delay time | t <sub>ODLY</sub>   |         | 13.7    | ns   | Ccard < 30 pF (1 card) |
| Output hold time  | t <sub>OH</sub>     | 1.5     |         | ns   | Ccard < 15 pF (1 card) |
| <b>Input DAT</b>  |                     |         |         |      |                        |
| Input setup time  | t <sub>SU2x</sub>   | 3       |         | ns   | Ccard < 10 pF (1 card) |
| Input hold time   | t <sub>IH2x</sub>   | 0.8     |         | ns   | Ccard < 10 pF (1 card) |
| <b>Output DAT</b> |                     |         |         |      |                        |
| Output delay time | t <sub>ODLY2x</sub> |         | 7.5     | ns   | Ccard < 25 pF (1 card) |
| Output hold time  | t <sub>OH2x</sub>   | 1.5     |         | ns   | Ccard < 15 pF (1 card) |

## 13.5 UART Timing - Default Mode

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The UART supports the Bluetooth 4.2 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 K baud.

The UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 2\%$ .

UART timing (default mode) diagram and parameters are shown in **Figure 19** and **Table 22**.

**Figure 19: UART Timing Diagram - Default Mode****Table 22: UART Timing Parameters - Default Mode**

| Reference | Description                                             | Minimum | Typical | Maximum | Unit        |
|-----------|---------------------------------------------------------|---------|---------|---------|-------------|
| 1         | Delay time, UART_CTS_N low to UART_TXD valid            |         |         | 1.5     | Bit periods |
| 2         | Setup time, UART_CTS_N high before midpoint of stop bit |         |         | 0.5     | Bit periods |
| 3         | Delay time, midpoint of stop bit to UART_RTS_N high     |         |         | 0.5     | Bit periods |

Examples of some common baud rates are shown in **Table 23**.

**Table 23: Common Baud Rate Examples**

| Desired Rate | Actual Rate set in the module | Error (%) |
|--------------|-------------------------------|-----------|
| 4000000      | 4000000                       | 0.00      |
| 3000000      | 3000000                       | 0.00      |
| 921600       | 923077                        | 0.16      |
| 115200       | 115385                        | 0.16      |
| 57600        | 57692                         | 0.16      |
| 9600         | 9600                          | 0.00      |

## 13.6 Bluetooth PCM Timing

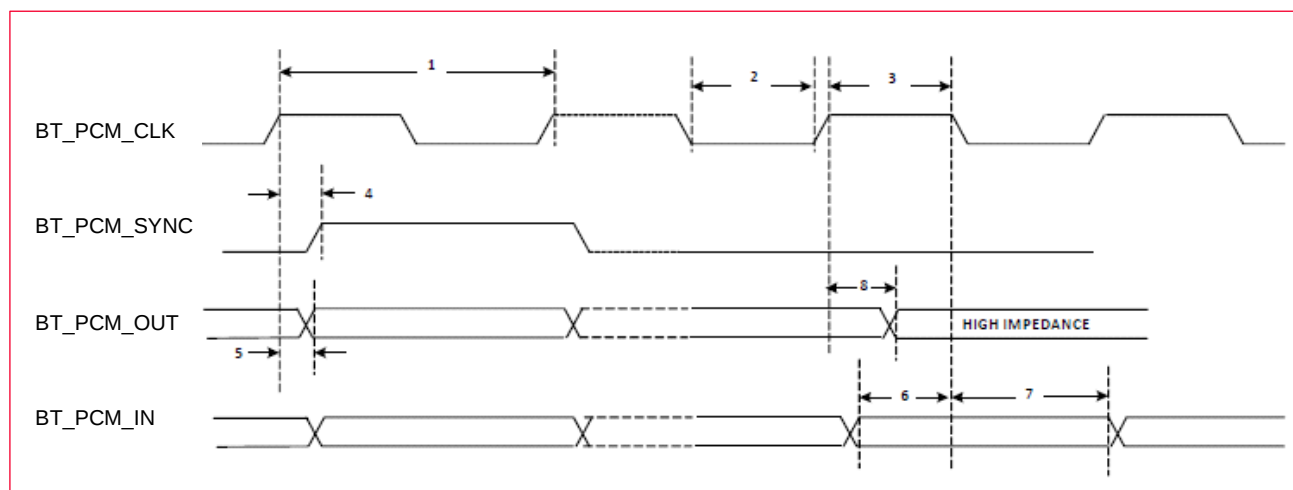
The PCM Interface can connect to linear PCM Codec devices. In master or slave mode. In master mode, the module generates the PCM\_CLK and PCM\_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the modules.

The PCM interface supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three-bit periods, and the pulse starts coincident with the first bit of the first slot.

### 13.6.1 Short Frame Sync - Master Mode

**Figure 20** and **Table 24** shows the Bluetooth PCM short frame sync data signal and parameters in master mode respectively.

**Figure 20: Short Frame Sync Signal - Master Mode**

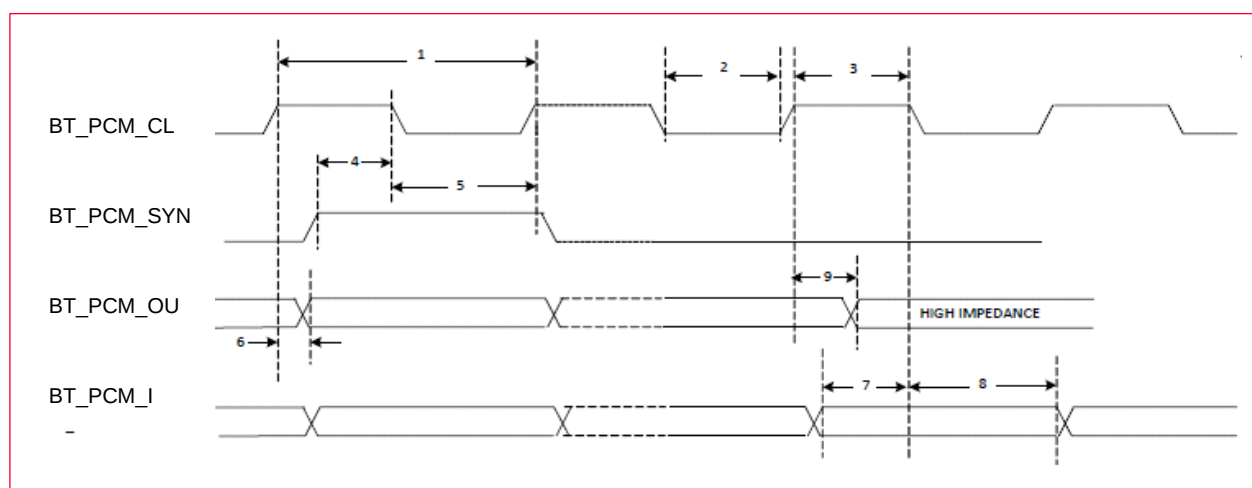


**Table 24: Short Frame Sync Signal Parameters - Master Mode**

| Reference | Description                                                                                   | Minimum | Typical | Maximum | Unit |
|-----------|-----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                       |         |         | 12      | MHz  |
| 2         | PCM bit clock High                                                                            | 41      |         |         | ns   |
| 3         | PCM bit clock Low                                                                             | 41      |         |         | ns   |
| 4         | PCM_SYNC delay                                                                                | 0       |         | 25      | ns   |
| 5         | PCM_OUT delay                                                                                 | 0       |         | 25      | ns   |
| 6         | PCM_IN setup                                                                                  | 8       |         |         | ns   |
| 7         | PCM_IN hold                                                                                   | 8       |         |         | ns   |
| 8         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance. | 0       |         | 25      | ns   |

### 13.6.2 Short Frame Sync - Slave Mode

**Figure 21** and **Table 25** shows PCM short frame sync data signal and its parameters in slave mode respectively.

**Figure 21: Short Frame Sync Signal - Slave Mode****Table 25: Short Frame Sync Signal Parameters - Slave Mode**

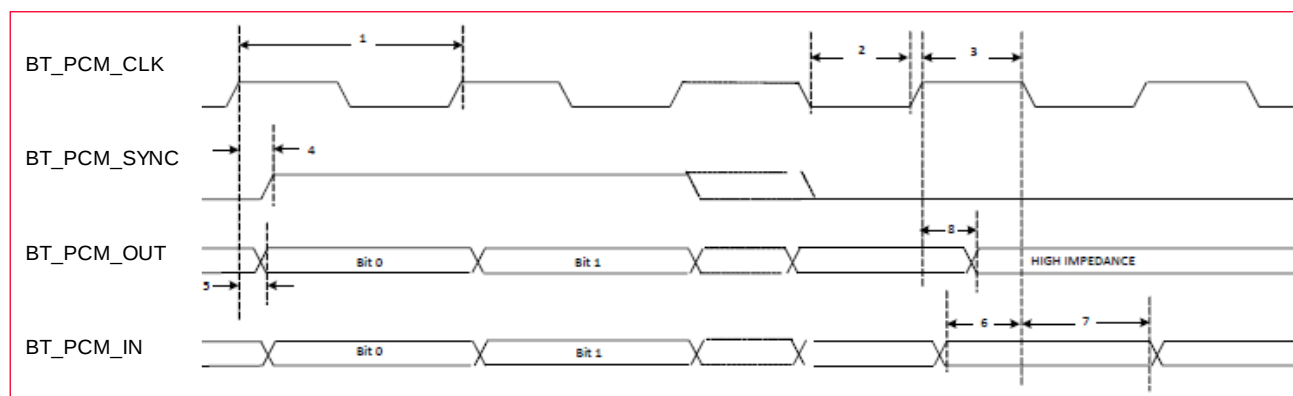
| Reference | Description                                                                                   | Minimum | Typical | Maximum | Unit |
|-----------|-----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                       |         |         | 12      | MHz  |
| 2         | PCM bit clock Low                                                                             | 41      |         |         | ns   |
| 3         | PCM bit clock High                                                                            | 41      |         |         | ns   |
| 4         | PCM_SYNC setup                                                                                | 8       |         |         | ns   |
| 5         | PCM_SYNC hold                                                                                 | 8       |         |         | ns   |
| 6         | PCM_OUT delay                                                                                 | 0       |         | 25      | ns   |
| 7         | PCM_IN setup                                                                                  | 8       |         |         | ns   |
| 8         | PCM_IN hold                                                                                   | 8       |         |         | ns   |
| 9         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance. | 0       |         | 25      | ns   |

### 13.6.3 Long Frame Sync - Master Mode

**Figure 22 and**

**Table 26** shows PCM long frame sync signal and its parameters in slave mode.

**Figure 22: Long Frame Sync Signal - Master Mode**

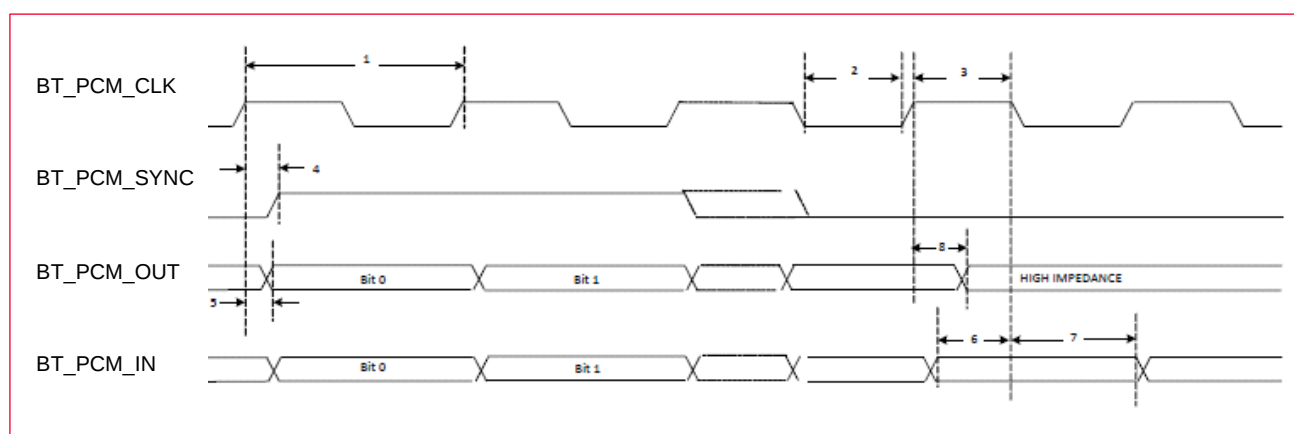


**Table 26: Long Frame Sync Signal Parameters - Master Mode**

| Reference | Description                                                                                  | Minimum | Typical | Maximum | Unit |
|-----------|----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                      |         |         | 12      | MHz  |
| 2         | PCM bit clock High                                                                           | 41      |         |         | ns   |
| 3         | PCM bit clock Low                                                                            | 41      |         |         | ns   |
| 4         | PCM_SYNC delay                                                                               | 0       |         | 25      | ns   |
| 5         | PCM_OUT delay                                                                                | 0       |         | 25      | ns   |
| 6         | PCM_IN setup                                                                                 | 8       |         |         | ns   |
| 7         | PCM_IN hold                                                                                  | 8       |         |         | ns   |
| 8         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance | 0       |         | 25      | ns   |

### 13.6.4 Long Frame Sync - Slave Mode

**Figure 23** and **Table 27** shows PCM long frame sync signal and parameters in slave mode.

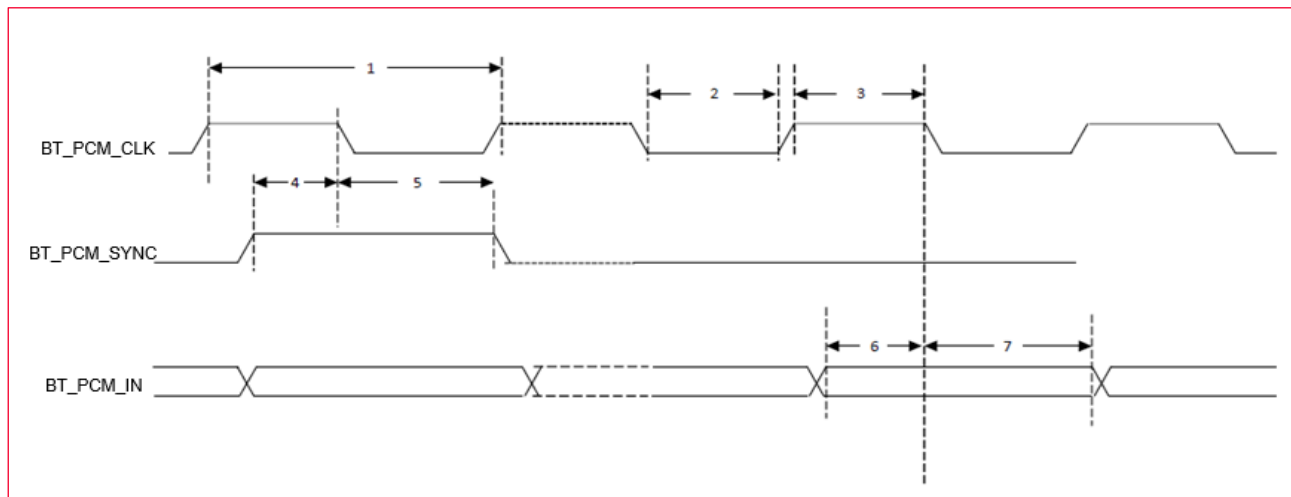
**Figure 23: Long Frame Sync Signal - Slave Mode****Table 27: Long Frame Sync Signal Parameters - Slave Mode**

| Reference | Description                                                                                   | Minimum | Typical | Maximum | Unit |
|-----------|-----------------------------------------------------------------------------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency                                                                       |         |         | 12      | MHz  |
| 2         | PCM bit clock High                                                                            | 41      |         |         | ns   |
| 3         | PCM bit clock Low                                                                             | 41      |         |         | ns   |
| 4         | PCM_SYNC setup                                                                                | 8       |         |         | ns   |
| 5         | PCM_SYNC hold                                                                                 | 8       |         |         | ns   |
| 6         | PCM_OUT delay                                                                                 | 0       |         | 25      | ns   |
| 7         | PCM_IN setup                                                                                  | 8       |         |         | ns   |
| 8         | PCM_IN hold                                                                                   | 8       |         |         | ns   |
| 9         | Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance. | 0       |         | 25      | ns   |

### 13.6.5 Short Frame Sync - Burst Mode

**Figure 24** and **Table 28** shows PCM short frame sync signal and its parameters in burst mode.

**Figure 24: Short Frame Sync Signal - Burst Mode**



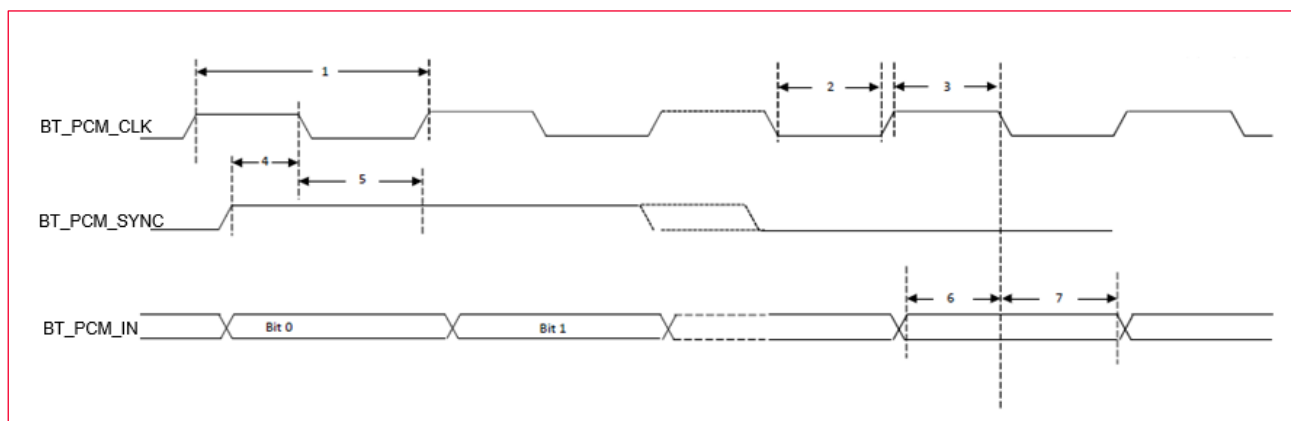
**Table 28: Short Frame Sync Signal Parameters - Burst Mode**

| Reference | Description             | Minimum | Typical | Maximum | Unit |
|-----------|-------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency |         |         | 24      | MHz  |
| 2         | PCM bit clock Low       | 20.8    |         |         | ns   |
| 3         | PCM bit clock High      | 20.8    |         |         | ns   |
| 4         | PCM_SYNC setup          | 8       |         |         | ns   |
| 5         | PCM_SYNC hold           | 8       |         |         | ns   |
| 6         | PCM_IN setup            | 8       |         |         | ns   |
| 7         | PCM_IN hold             | 8       |         |         | ns   |

### 13.6.6 Long Frame Sync - Burst Mode

**Figure 25** and **Table 29** shows PCM long frame sync signal and parameters in burst mode.

**Figure 25: Long Frame Sync Signal - Burst Mode**



**Table 29: Long Frame Sync Signal Parameters - Burst Mode**

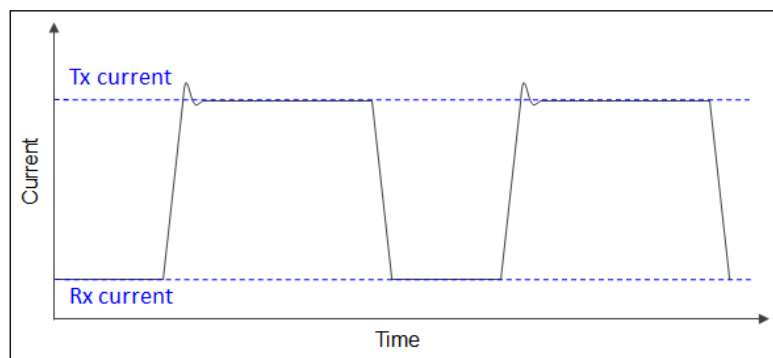
| Reference | Description             | Minimum | Typical | Maximum | Unit |
|-----------|-------------------------|---------|---------|---------|------|
| 1         | PCM bit clock frequency |         |         | 24      | MHz  |
| 2         | PCM bit clock Low       | 20.8    |         |         | ns   |
| 3         | PCM bit clock High      | 20.8    |         |         | ns   |
| 4         | PCM_SYNC setup          | 8       |         |         | ns   |
| 5         | PCM_SYNC hold           | 8       |         |         | ns   |
| 6         | PCM_IN setup            | 8       |         |         | ns   |
| 7         | PCM_IN hold             | 8       |         |         | ns   |

## 14 DC/RF Characteristics

This section describes the electrical characteristics of the Type 2AE module.

Burst current definition is shown in **Figure 26**.

**Figure 26: Burst Current Definition**



## 14.1 DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

**Table 30: Characteristics Values for IEEE 802.11b - 2.4 GHz**

| Items             | Contents           |
|-------------------|--------------------|
| Specification     | IEEE 802.11b       |
| Mode              | DSSS / CCK         |
| Channel Frequency | 2412 - 2472 MHz    |
| Data Rate         | 1, 2, 5.5, 11 Mbps |

### 14.1.1 High-Rate Condition for IEEE 802.11b - 2.4 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 17 dBm, 11 Mbps mode

**Table 31: High-Rate Condition for IEEE 802.11b - 2.4 GHz**

| Items                                      | Contents |         |         |         |
|--------------------------------------------|----------|---------|---------|---------|
| DC Characteristics                         | Minimum  | Typical | Maximum | Unit    |
| DC Current                                 |          |         |         |         |
| • Tx mode (1024 byte, 20 $\mu$ s interval) |          | 350     |         | mA      |
| • Rx mode                                  |          | 55      |         | mA      |
| TX Characteristics                         | Minimum  | Typical | Maximum | Unit    |
| Output Power                               | 14.5     | 17      | 19.5    | dBm     |
| Spectrum Mask Margin                       |          |         |         |         |
| • 1 <sup>st</sup> side lobes (-30 dBr)     | 0        |         |         | dB      |
| • 2 <sup>nd</sup> side lobes (-50 dBr)     | 0        |         |         | dB      |
| Power-on and Power-down ramp               |          |         | 2.0     | $\mu$ s |
| RF Carrier Suppression                     | 15       |         |         | dB      |
| Modulation Accuracy (EVM)                  |          |         | 35      | %       |
| Frequency Tolerance                        | -20      |         | 20      | ppm     |
| Out band Spurious Emissions                |          |         |         |         |
| • 30 - 47 MHz (BW = 100 kHz)               |          |         | -36     | dBm     |
| • 47 - 74 MHz (BW = 100 kHz)               |          |         | -54     | dBm     |
| • 74 - 87.5 MHz (BW = 100 kHz)             |          |         | -36     | dBm     |
| • 87.5 - 118 MHz (BW = 100 kHz)            |          |         | -54     | dBm     |
| • 118 - 174 MHz (BW = 100 kHz)             |          |         | -36     | dBm     |
| • 174 - 230 MHz (BW = 100 kHz)             |          |         | -54     | dBm     |
| • 230 - 470 MHz (BW = 100 kHz)             |          |         | -36     | dBm     |
| • 470 - 862 MHz (BW = 100 kHz)             |          |         | -54     | dBm     |
| • 862 - 1000 MHz (BW = 100 kHz)            |          |         | -36     | dBm     |
| • 1000 - 12750 MHz (BW = 1 MHz)            |          |         | -30     | dBm     |
| Rx Characteristics                         | Minimum  | Typical | Maximum | Unit    |
| Minimum Input Level Sensitivity            |          |         | -76     | dBm     |
| Maximum Input Level (FER $\leq$ 8%)        | -10      |         |         | dBm     |
| Adjacent Channel Rejection (FER $\leq$ 8%) | 35       |         |         | dB      |

## 14.1.2 Low-Rate Condition for IEEE 802.11b - 2.4 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 17 dBm, 1 Mbps mode

**Table 32: Low-Rate Condition for IEEE 802.11b - 2.4 GHz**

| Items                                  | Contents |         |         |      |
|----------------------------------------|----------|---------|---------|------|
| DC Characteristics                     | Minimum  | Typical | Maximum | Unit |
| DC Current                             |          |         |         |      |
| • Tx mode (1024 byte, 20μs interval)   |          | 340     |         | mA   |
| • Rx mode                              |          | 55      |         | mA   |
| TX Characteristics                     | Minimum  | Typical | Maximum | Unit |
| Output Power                           | 14.5     | 17      | 19.5    | dBm  |
| Spectrum Mask Margin                   |          |         |         |      |
| • 1 <sup>st</sup> side lobes (-30 dBr) | 0        |         |         | dB   |
| • 2 <sup>nd</sup> side lobes (-50 dBr) | 0        |         |         | dB   |
| Power-on and Power-down Ramp           |          |         | 2.0     | μs   |
| RF Carrier Suppression                 | 15       |         |         | dB   |
| Modulation Accuracy (EVM)              |          |         | 35      | %    |
| Frequency Tolerance                    | -20      |         | 20      | ppm  |
| Out band Spurious Emissions            |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)           |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)           |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)         |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)        |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)         |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)         |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)         |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)         |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)        |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)        |          |         | -30     | dBm  |
| Rx Characteristics                     | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity        |          |         | -76     | dBm  |
| Maximum Input Level (FER ≤ 8%)         | -10      |         |         | dBm  |
| Adjacent Channel Rejection (FER ≤ 8%)  | 35       |         |         | dB   |

## 14.2 DC/RF Characteristics for IEEE 802.11g - 2.4GHz

**Table 33: Characteristics Values for IEEE 802.11g - 2.4 GHz**

| Items             | Contents                          |
|-------------------|-----------------------------------|
| Specification     | IEEE 802.11g                      |
| Mode              | OFDM                              |
| Channel Frequency | 2412 - 2472 MHz                   |
| Data Rate         | 6, 9, 12, 18, 24, 36, 48, 54 Mbps |

### 14.2.1 High-Rate Condition for IEEE 802.11g - 2.4 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 16 dBm, 54 Mbps mode

**Table 34: High-Rate Condition for IEEE 802.11g - 2.4 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 290     |         | mA   |
| • Rx mode                                   |          | 55      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 13.5     | 16      | 18.5    | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -25     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Out Band Spurious Emissions                 |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -65     | dBm  |
| Maximum Input Level (PER $\leq$ 10%)        | -20      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -1       |         |         | dB   |

## 14.2.2 Low-Rate Condition for IEEE 802.11g – 2.4 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 18 dBm, 6 Mbps mode

**Table 35: Low-Rate Condition for IEEE 802.11g - 2.4 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 310     |         | mA   |
| • Rx mode                                   |          | 55      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 15.5     | 18      | 20.5    | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Out Band Spurious Emissions                 |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -82     | dBm  |
| Maximum Input Level (PER $\leq$ 10%)        | -20      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.3 DC/RF Characteristics for IEEE 802.11n - 2.4 GHz

**Table 36: Characteristics Values for IEEE 802.11n - 2.4 GHz**

| Items             | Contents        |
|-------------------|-----------------|
| Specification     | IEEE 802.11n    |
| Mode              | OFDM            |
| Channel Frequency | 2412 - 2472 MHz |
| Data Rate         | MCS0 - MCS7     |

### 14.3.1 High-Rate Condition for IEEE 802.11n - 2.4 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 14 dBm, MCS7

**Table 37: High-Rate Condition for IEEE 802.11n - 2.4 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 280     |         | mA   |
| • Rx mode                                   |          | 55      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 11.5     | 14      | 16.5    | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -27     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Out band Spurious Emissions                 |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -64     | dBm  |
| Maximum Input Level (PER $\leq$ 10%)        | -20      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -2       |         |         | dB   |

## 14.3.2 Low-Rate Condition for IEEE 802.11n – 2.4 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 16 dBm, MCS0

**Table 38: Low-Rate Condition for IEEE 802.11n - 2.4 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 300     |         | mA   |
| • Rx mode                                   |          | 55      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 13.5     | 16      | 18.5    | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Out band Spurious Emissions                 |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -82     | dBm  |
| Maximum Input Level (PER $\leq$ 10%)        | -20      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.4 DC/RF Characteristics for IEEE 802.11a - 5 GHz

**Table 39: Characteristics Values for IEEE 802.11a - 5 GHz**

| Items             | Contents                                                                        |
|-------------------|---------------------------------------------------------------------------------|
| Specification     | IEEE 802.11a                                                                    |
| Mode              | OFDM                                                                            |
| Channel Frequency | 5180 to 5240 MHz,<br>5260 to 5320 MHz,<br>5500 to 5720 MHz,<br>5745 to 5825 MHz |
| Data Rate         | 6, 9, 12, 18, 24, 36, 48, 54 Mbps                                               |

### 14.4.1 High-Rate Condition for IEEE 802.11a - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 14 dBm, 54 Mbps

**Table 40: High-Rate Condition for IEEE 802.11a - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 290     |         | mA   |
| • Rx mode                                   |          | 70      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 12       | 14      | 16      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -25     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -65     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -1       |         |         | dB   |

## 14.4.2 Low-Rate Condition for IEEE 802.11a - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 16 dBm, 6 Mbps

**Table 41: Low-Rate Condition for IEEE 802.11a - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 310     |         | mA   |
| • Rx mode                                   |          | 70      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 14       | 16      | 18      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -82     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.5 DC/RF Characteristics for IEEE 802.11n (HT20) - 5 GHz

**Table 42: Characteristics Values for IEEE 802.11n (HT20) - 5 GHz**

| Items             | Contents         |
|-------------------|------------------|
| Specification     | IEEE 802.11n     |
| Mode              | OFDM             |
| Channel Frequency | 5180 to 5825 MHz |
| Data Rate         | MCS0 - MCS7      |

### 14.5.1 High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 14 dBm, MCS7

**Table 43: High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 280     |         | mA   |
| • Rx mode                                   |          | 70      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 12       | 14      | 16      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -27     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -64     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -2       |         |         | dB   |

## 14.5.2 Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 16 dBm, MCS0

**Table 44: Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 300     |         | mA   |
| • Rx mode                                   |          | 70      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 14       | 16      | 18      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -82     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.6 DC/RF Characteristics for IEEE 802.11ac (VHT20) - 5 GHz

**Table 45: Characteristics Values for IEEE 802.11ac (VHT20) - 5 GHz**

| Items             | Contents         |
|-------------------|------------------|
| Specification     | IEEE 802.11ac    |
| Mode              | OFDM             |
| Channel Frequency | 5180 to 5825 MHz |
| Data Rate         | MCS0 - MCS8      |

### 14.6.1 High-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 13 dBm, MCS8

**Table 46: High-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 280     |         | mA   |
| • Rx mode                                   |          | 70      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 11       | 13      | 15      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -30     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -59     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -7       |         |         | dB   |

## 14.6.2 Low-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 16 dBm, MCS0

**Table 47: Low-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 300     |         | mA   |
| • Rx mode                                   |          | 70      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 14       | 16      | 18      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 9 MHz to 11 MHz (0 ~ -20 dBr)             | 0        |         |         | dB   |
| • 11 MHz to 20 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 20 MHz to 30 MHz (-28 ~ -40 dBr)          | 0        |         |         | dB   |
| • 30 MHz to 33 MHz (-40 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -82     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.7 DC/RF Characteristics for IEEE 802.11n (HT40) - 5 GHz

**Table 48: Characteristics Values for IEEE 802.11n (HT40) - 5 GHz**

| Items             | Contents         |
|-------------------|------------------|
| Specification     | IEEE 802.11n     |
| Mode              | OFDM             |
| Channel Frequency | 5190 to 5795 MHz |
| Data Rate         | MCS0 - MCS7      |

### 14.7.1 High-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 13 dBm, MCS7, HT 40 MHz

**Table 49: High-Rate Condition for IEEE 802.11n (HT40) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 320     |         | mA   |
| • Rx mode                                   |          | 80      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 11       | 13      | 15      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 19 MHz to 21 MHz (0 ~ -20 dBr)            | 0        |         |         | dB   |
| • 21 MHz to 40 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 40 MHz to 60 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 60 MHz to 80 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -27     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -61     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -2       |         |         | dB   |

## 14.7.2 Low-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 14 dBm, MCS0, HT 40 MHz

**Table 50: Low-Rate Condition for IEEE 802.11n (HT40) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 350     |         | mA   |
| • Rx mode                                   |          | 80      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 12       | 14      | 16      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 19 MHz to 21 MHz (0 ~ -20 dBr)            | 0        |         |         | dB   |
| • 21 MHz to 40 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 40 MHz to 60 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 60 MHz to 80 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -79     | dBm  |
| Maximum Input Level (PER <10%)              | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.8 DC/RF Characteristics for IEEE 802.11ac (VHT40) - 5 GHz

**Table 51: Characteristics Values for IEEE 802.11ac (VHT40) - 5 GHz**

| Items             | Contents          |
|-------------------|-------------------|
| Specification     | IEEE 802.11ac     |
| Mode              | OFDM              |
| Channel Frequency | 5190 to 5795 MHz, |
| Data Rate         | MCS0 - MCS9       |

### 14.8.1 High-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 11 dBm, MCS9, VHT 40 MHz

**Table 52: High-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 320     |         | mA   |
| • Rx mode                                   |          | 80      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 9        | 11      | 13      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 19 MHz to 21 MHz (0 ~ -20 dBr)            | 0        |         |         | dB   |
| • 21 MHz to 40 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 40 MHz to 60 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 60 MHz to 80 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -32     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -54     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -9       |         |         | dB   |

## 14.8.2 Low-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 14 dBm, MCS0, VHT 40 MHz

**Table 53: Low-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 350     |         | mA   |
| • Rx mode                                   |          | 80      |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 12       | 14      | 16      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 19 MHz to 21 MHz (0 ~ -20 dBr)            | 0        |         |         | dB   |
| • 21 MHz to 40 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 40 MHz to 60 MHz (-28 ~ -45 dBr)          | 0        |         |         | dB   |
| • 60 MHz to 80 MHz (-45 dBr)                | 0        |         |         | dB   |
| Constellation Error (EVM)                   |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -54     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.9 DC/RF Characteristics for IEEE 802.11ac (VHT80) - 5 GHz

**Table 54: Characteristics Values for IEEE 802.11ac (VHT80) - 5 GHz**

| Items             | Contents         |
|-------------------|------------------|
| Specification     | IEEE 802.11ac    |
| Mode              | OFDM             |
| Channel Frequency | 5210 to 5775 MHz |
| Data Rate         | MCS0 - MCS9      |

### 14.9.1 High-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 11 dBm, MCS9, VHT 80 MHz

**Table 55: High-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 340     |         | mA   |
| • Rx mode                                   |          | 105     |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 9        | 11      | 13      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 39 MHz to 41 MHz (0 ~ -20 dBr)            | 0        |         |         | dB   |
| • 41 MHz to 80 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 80 MHz to 120 MHz (-28 ~ -40 dBr)         | 0        |         |         | dB   |
| • 120 MHz to 140 MHz (-40 dBr)              | 0        |         |         | dB   |
| Constellation Error                         |          |         | -32     | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 1 00 kHz)            |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -51     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | -9       |         |         | dB   |

## 14.9.2 Low-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V, Output power setting = 13 dBm, MCS0, VHT 80 MHz

**Table 56: Low-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz**

| Items                                       | Contents |         |         |      |
|---------------------------------------------|----------|---------|---------|------|
| DC Characteristics                          | Minimum  | Typical | Maximum | Unit |
| DC Current                                  |          |         |         |      |
| • Tx mode (1024 byte, 20 $\mu$ s interval)  |          | 380     |         | mA   |
| • Rx mode                                   |          | 105     |         | mA   |
| TX Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Output Power                                | 11       | 13      | 15      | dBm  |
| Spectrum Mask Margin                        |          |         |         |      |
| • 39 MHz to 41 MHz (0 ~ -20 dBr)            | 0        |         |         | dB   |
| • 41 MHz to 80 MHz (-20 ~ -28 dBr)          | 0        |         |         | dB   |
| • 80 MHz to 120 MHz (-28 ~ -40 dBr)         | 0        |         |         | dB   |
| • 120 MHz to 140 MHz (-40 dBr)              | 0        |         |         | dB   |
| Constellation Error                         |          |         | -5      | dB   |
| Frequency Tolerance                         | -20      |         | 20      | ppm  |
| Spurious Emissions                          |          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                |          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                |          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)             |          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)              |          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)              |          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)             |          |         | -36     | dBm  |
| • 1000 - 5150 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5350 - 5470 MHz (BW = 1 MHz)              |          |         | -30     | dBm  |
| • 5725 - 26000 MHz (BW = 1 MHz)             |          |         | -30     | dBm  |
| Rx Characteristics                          | Minimum  | Typical | Maximum | Unit |
| Minimum Input Level Sensitivity             |          |         | -76     | dBm  |
| Maximum Input Level (PER < 10%)             | -30      |         |         | dBm  |
| Adjacent Channel Rejection (PER $\leq$ 10%) | 16       |         |         | dB   |

## 14.10 DC/RF Characteristics for Bluetooth

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V

**Table 57: DC/RF Characteristics for Bluetooth**

| Items                                                          | Contents                 |                |                |             |
|----------------------------------------------------------------|--------------------------|----------------|----------------|-------------|
| Bluetooth Specification (power class)                          | Version 5.2              |                |                |             |
| Channel Frequency (spacing)                                    | 2402 to 2480 MHz (1 MHz) |                |                |             |
| Current Consumption                                            | Minimum                  | Typical        | Maximum        | Unit        |
| • Tx = Rx = DH5 (fully occupied)                               |                          | 55             |                | mA          |
| • Tx = Rx = 2DH5 (fully occupied)                              |                          | 45             |                | mA          |
| • Tx = Rx = 3DH5 (fully occupied)                              |                          | 45             |                | mA          |
| <b>Transmitter</b>                                             | <b>Minimum</b>           | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| Output Power @ DH5                                             | 6                        | 10             | 14             | dBm         |
| Frequency range                                                | 2400                     |                | 2483.5         | MHz         |
| 20 dB bandwidth                                                |                          |                | 1              | MHz         |
| Adjacent Channel Power                                         |                          |                |                |             |
| • [M-N] = 2                                                    |                          |                | -20            | dBm         |
| • [M-N] ≥ 3                                                    |                          |                | -40            | dBm         |
| <b>Modulation Characteristics</b>                              | <b>Minimum</b>           | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| • Modulation $\Delta f_{1\text{avg}}$                          | 140                      |                | 175            | kHz         |
| • Modulation $\Delta f_{2\text{max}}$                          | 115                      |                |                | kHz         |
| • Modulation $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8                      | 1              |                |             |
| <b>Carrier Frequency Drift</b>                                 | <b>Minimum</b>           | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| • 1slot                                                        | -25                      |                | +25            | kHz         |
| • 3slot / 5slot                                                | -40                      |                | +40            | kHz         |
| • Maximum drift rate                                           |                          |                | 20             | kHz/50μs    |
| EDR Relative Power                                             | -4                       |                | 1              | dB          |
| EDR Carrier Frequency Stability and Modulation Accuracy        |                          |                |                |             |
| • $\omega_i$                                                   | -75                      |                | 75             | kHz         |
| • $\omega_i + \omega_o$                                        | -75                      |                | 75             | kHz         |
| • $\omega_o$                                                   | -10                      |                | 10             | kHz         |
| • RMS DEVM (DQPSK)                                             |                          |                | 20             | %           |
| • Peak DEVM (DQPSK)                                            |                          |                | 35             | %           |
| • 99% DEVM (DQPSK)                                             |                          |                | 30             | %           |
| • RMS DEVM (8DPSK)                                             |                          |                | 13             | %           |
| • Peak DEVM (8DPSK)                                            |                          |                | 25             | %           |
| • 99% DEVM (8DPSK)                                             |                          |                | 20             | %           |
| Spurious Emissions                                             |                          |                |                |             |
| • 30 - 47 MHz (BW = 100 kHz)                                   |                          |                | -36            | dBm         |
| • 47 - 74 MHz (BW = 100 kHz)                                   |                          |                | -54            | dBm         |
| • 74 - 87.5 MHz (BW = 100 kHz)                                 |                          |                | -36            | dBm         |
| • 87.5 - 118 MHz (BW = 100 kHz)                                |                          |                | -54            | dBm         |
| • 118 - 174 MHz (BW = 100 kHz)                                 |                          |                | -36            | dBm         |
| • 174 - 230 MHz (BW = 100 kHz)                                 |                          |                | -54            | dBm         |
| • 230 - 470 MHz (BW = 100 kHz)                                 |                          |                | -36            | dBm         |
| • 470 - 862 MHz (BW = 100 kHz)                                 |                          |                | -54            | dBm         |
| • 862 - 1000 MHz (BW = 100 kHz)                                |                          |                | -36            | dBm         |

| Items                                 | Contents       |                |                |             |
|---------------------------------------|----------------|----------------|----------------|-------------|
| • 1000 - 12750 MHz (BW = 1 MHz)       |                |                | -30            | dBm         |
| <b>Receiver</b>                       | <b>Minimum</b> | <b>Typical</b> | <b>Maximum</b> | <b>Unit</b> |
| BDR Sensitivity (BER ≤ 0.1%)          |                |                | -80            | dBm         |
| EDR Sensitivity (BER ≤ 0.007%) @8DPSK |                |                | -77            | dBm         |
| C/I Performance (BER ≤ 0.1%)          |                |                |                |             |
| • co-channel                          |                |                | 11             | dB          |
| • 1 MHz                               |                |                | 0              | dB          |
| • 2 MHz                               |                |                | -30            | dB          |
| • 3 MHz                               |                |                | -40            | dB          |
| • image (+4 MHz)                      |                |                | -9             | dB          |
| • image +/- 1 MHz                     |                |                | -20            | dB          |
| Maximum Input Level (BER ≤ 0.1%)      | -20            |                |                | dBm         |



**Adjacent Channel Power:** Up to three spurious responses within Bluetooth limits are allowed.

## 14.11 DC/RF Characteristics for Bluetooth Low Energy

**Conditions:** 25 °C, VBAT = 3.3V, VDDIO = 3.3V

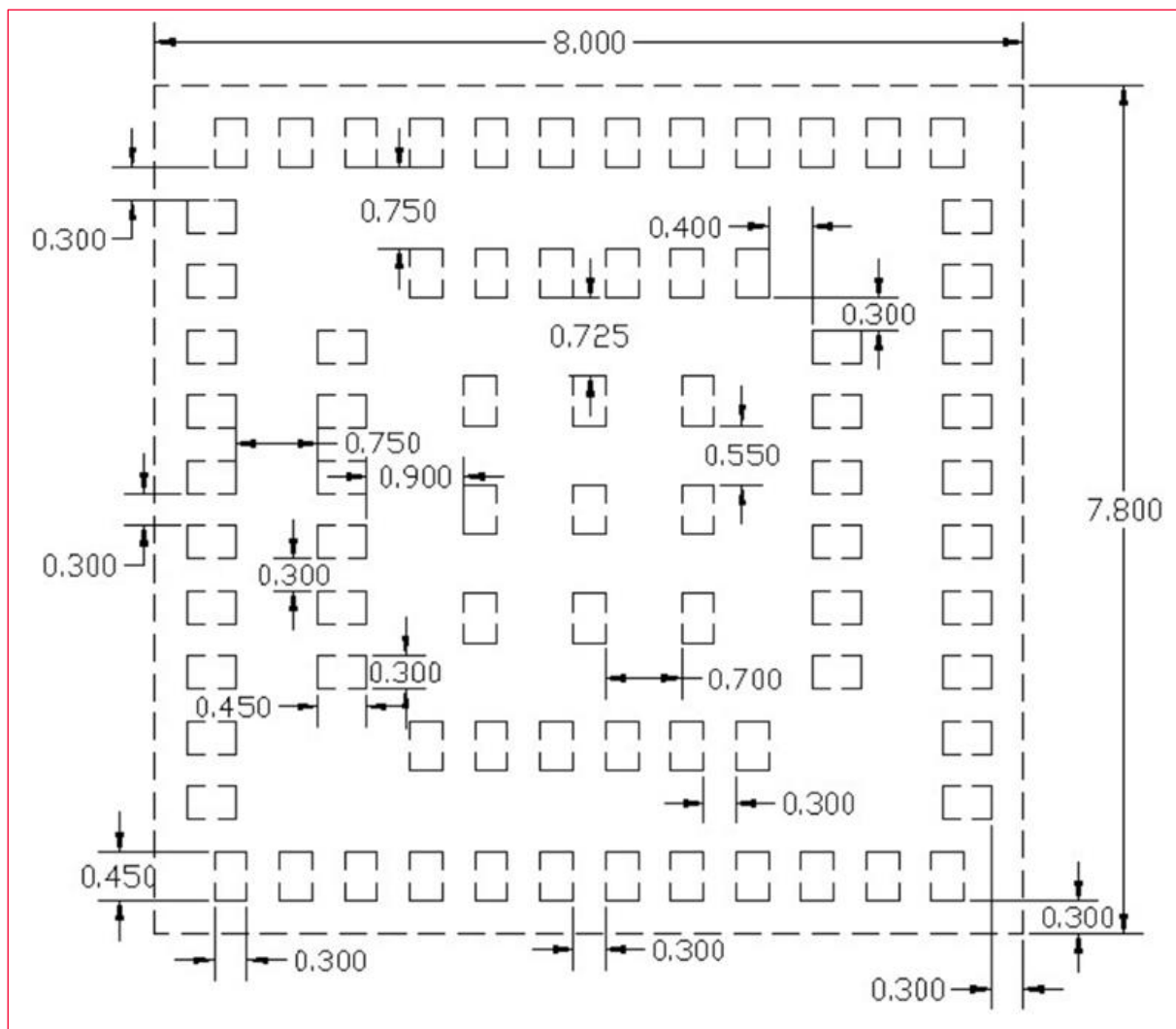
**Table 58: DC/RF Characteristics for BLE**

| Items                                               | Contents                 |         |         |      |
|-----------------------------------------------------|--------------------------|---------|---------|------|
| Bluetooth Specification (power class)               | Version 5.2(LE)          |         |         |      |
| Channel Frequency (spacing)                         | 2402 to 2480 MHz (2 MHz) |         |         |      |
| Number of RF Channel                                | 40                       |         |         |      |
| Item / Condition                                    | Minimum                  | Typical | Maximum | Unit |
| Center Frequency                                    | 2402                     |         | 2480    | MHz  |
| Channel Spacing                                     |                          | 2       |         | MHz  |
| Number of RF Channel                                |                          | 40      |         |      |
| Output Power                                        |                          | 8       |         | dBm  |
| Modulation Characteristics                          |                          |         |         |      |
| • $\Delta f_{1\text{avg}}$                          | 225                      |         | 275     | kHz  |
| • $\Delta f_{2\text{max}}$ (at 99.9%)               | 185                      |         |         | kHz  |
| • $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$ | 0.8                      |         |         |      |
| Spurious Emissions                                  |                          |         |         |      |
| • 30 - 47 MHz (BW = 100 kHz)                        |                          |         | -36     | dBm  |
| • 47 - 74 MHz (BW = 100 kHz)                        |                          |         | -54     | dBm  |
| • 74 - 87.5 MHz (BW = 100 kHz)                      |                          |         | -36     | dBm  |
| • 87.5 - 118 MHz (BW = 100 kHz)                     |                          |         | -54     | dBm  |
| • 118 - 174 MHz (BW = 100 kHz)                      |                          |         | -36     | dBm  |
| • 174 - 230 MHz (BW = 100 kHz)                      |                          |         | -54     | dBm  |
| • 230 - 470 MHz (BW = 100 kHz)                      |                          |         | -36     | dBm  |
| • 470 - 862 MHz (BW = 100 kHz)                      |                          |         | -54     | dBm  |
| • 862 - 1000 MHz (BW = 100 kHz)                     |                          |         | -36     | dBm  |
| • 1000 - 12750 MHz (BW = 1 MHz)                     |                          |         | -30     | dBm  |
| Receiver Sensitivity (PER < 30.8%)                  |                          |         | -70     | dBm  |
| Maximum Input Signal Level (PER < 30.8%)            | -10                      |         |         | dBm  |
| PER Report Integrity (-30 dBm input)                | 50                       |         | 65.4    | %    |

## 15 Land Pattern

The land pattern (in mm) is shown in **Figure 27**.

**Figure 27: Land Pattern (Unit: mm)**



This land pattern is for reference purpose only. Consult your manufacturing group to ensure your company's manufacturing guidelines are met.

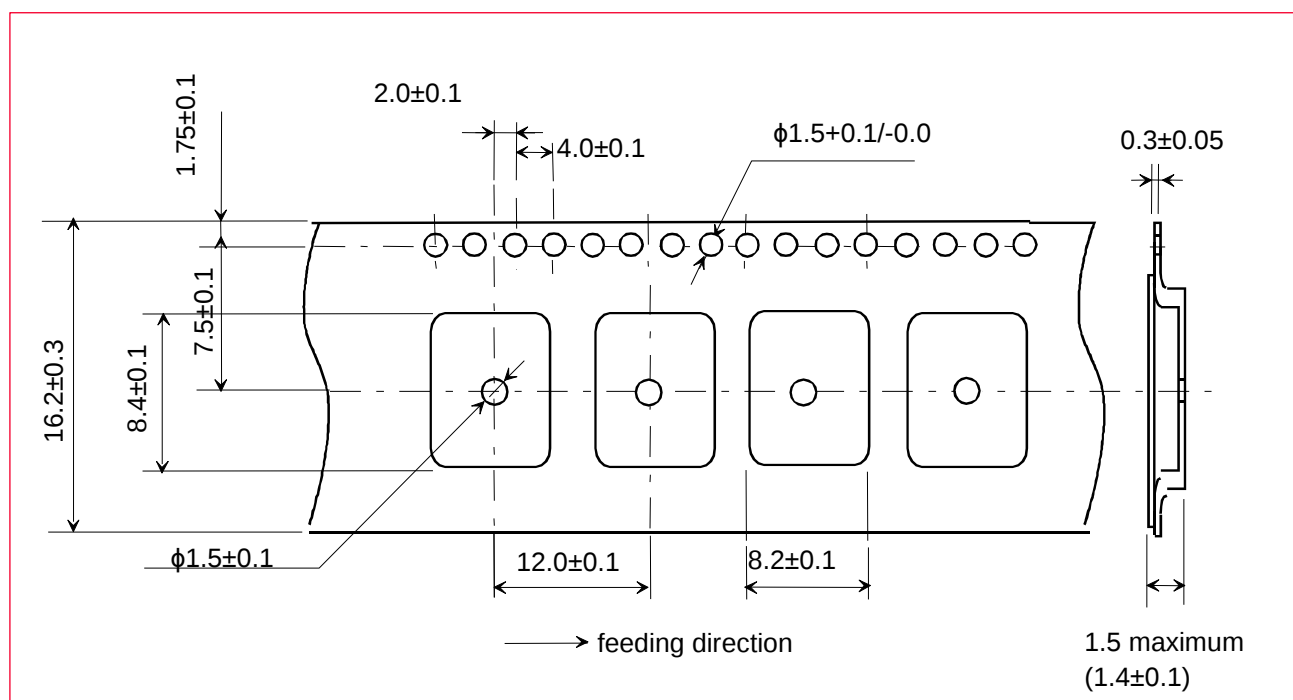
## 16 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

### 16.1 Dimensions of Tape (Plastic Tape)

**Figure 28** is a graphical representation of the tape dimension (plastic tape)<sup>5</sup>.

**Figure 28: Dimensions of Tape (Unit: mm)**

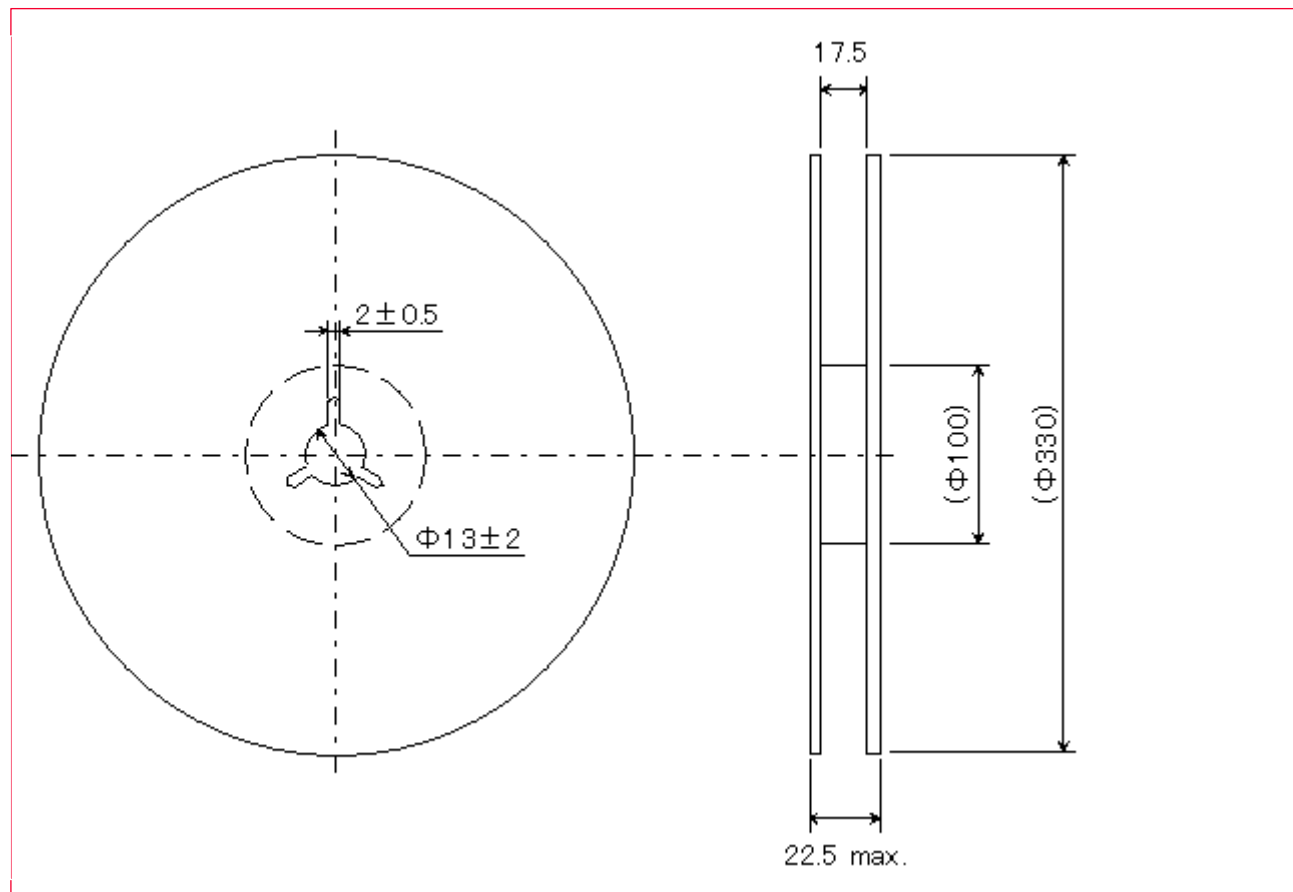


<sup>5</sup> Cumulative tolerance of maximum  $40.0 \pm 0.15$  mm every 10 pitches

## 16.2 Dimension of Reel

Figure 29 shows the reel dimensions.

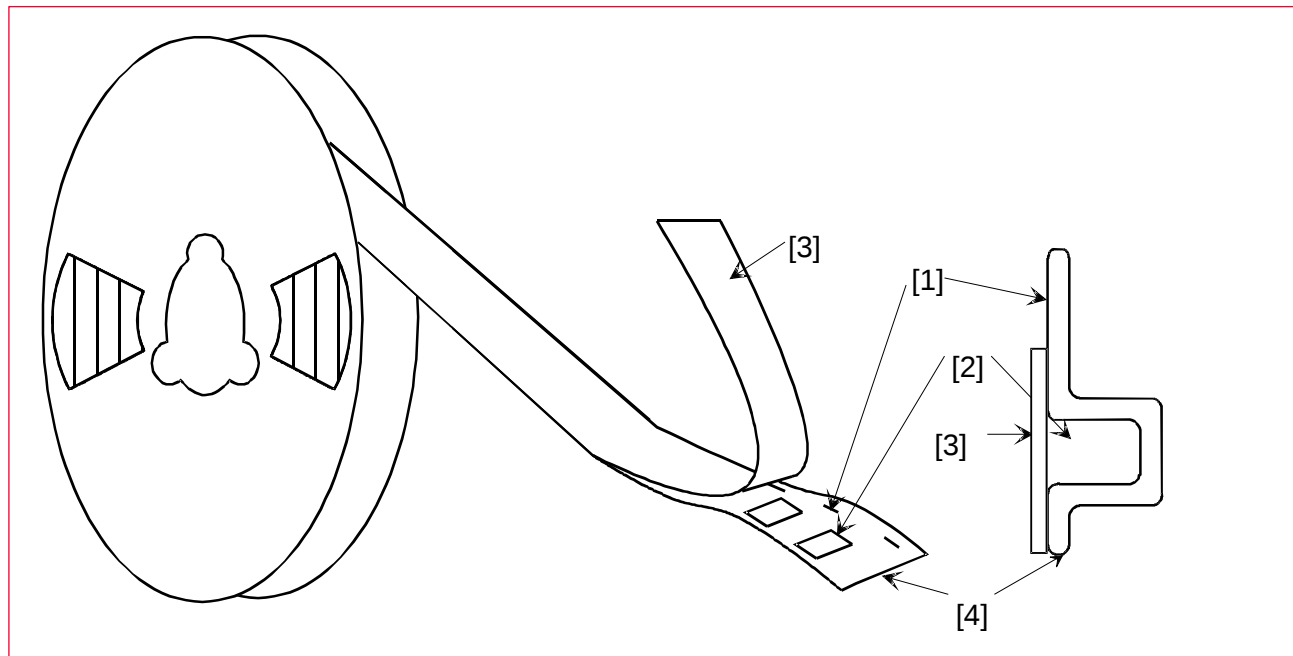
Figure 29: Dimensions of Reel (Unit: mm)



## 16.3 Taping Diagrams

**Figure 30** shows the tapings diagrams and **Figure 31** shows the close up.

**Figure 30: Taping Diagrams**

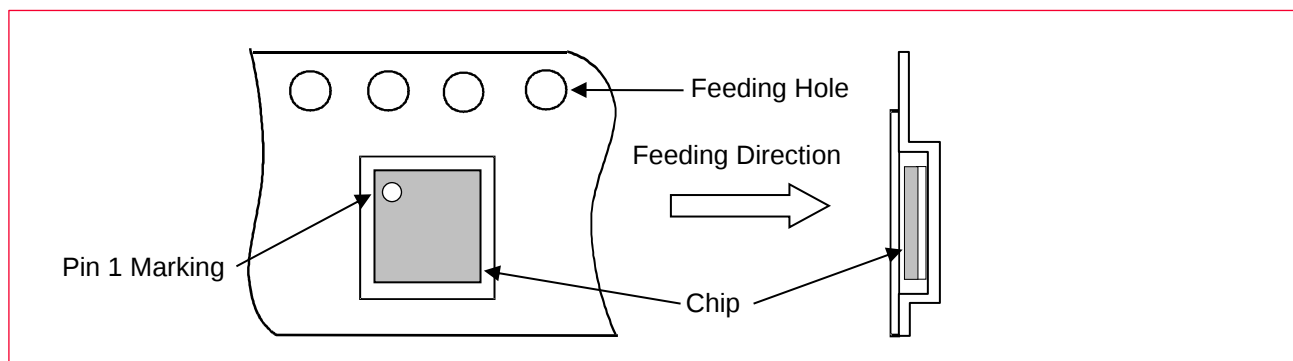


**Table 59** shows the taping specifications.

**Table 59: Taping Specifications**

| Mark | Description                                                                                                                                                            |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1    | Feeding hole: As specified in <a href="#">Dimensions of Tape (Plastic tape)</a>  .  |
| 2    | Hole for Chip: As specified in <a href="#">Dimensions of Tape (Plastic tape)</a>  . |
| 3    | Cover tape: 62 $\mu$ m in thickness.                                                                                                                                   |
| 4    | Base tape: As specified in <a href="#">Dimensions of Tape (Plastic tape)</a>  .     |

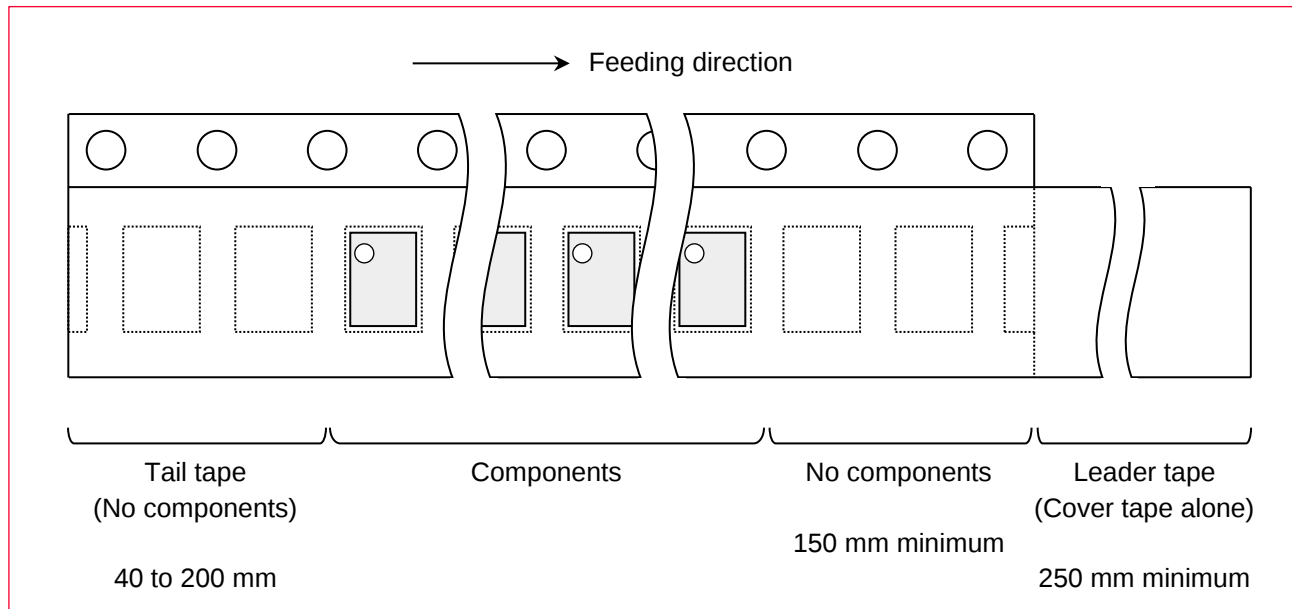
**Figure 31: Taping Diagrams (Close Up)**



## 16.4 Leader and Tail Tape

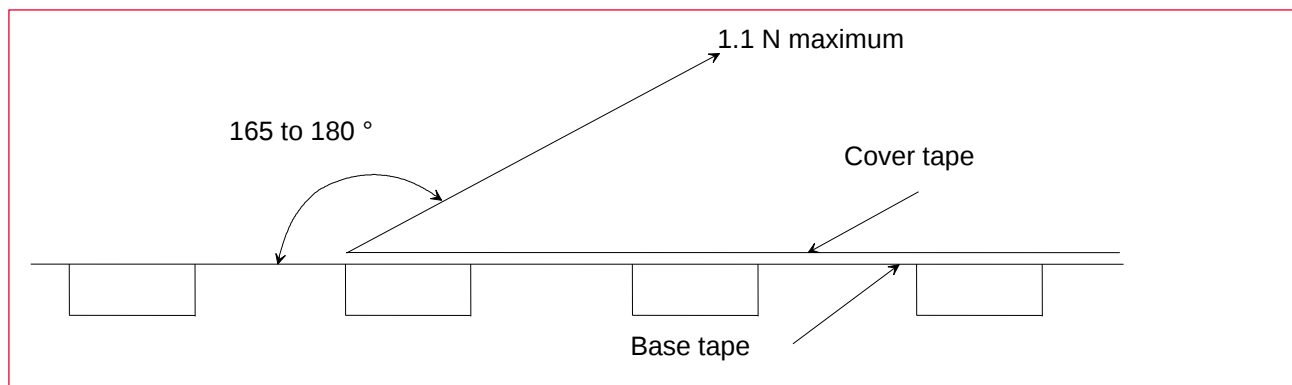
The leader and tail tape are shown in **Figure 32**.

**Figure 32: Leader and Tail Tape**



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Packaging unit: 1000 pcs. / Reel
- Tape material:
  - Base tape: Plastic
  - Reel: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling off force: 1.1 N maximum in the direction of peeling as shown in **Figure 33**.

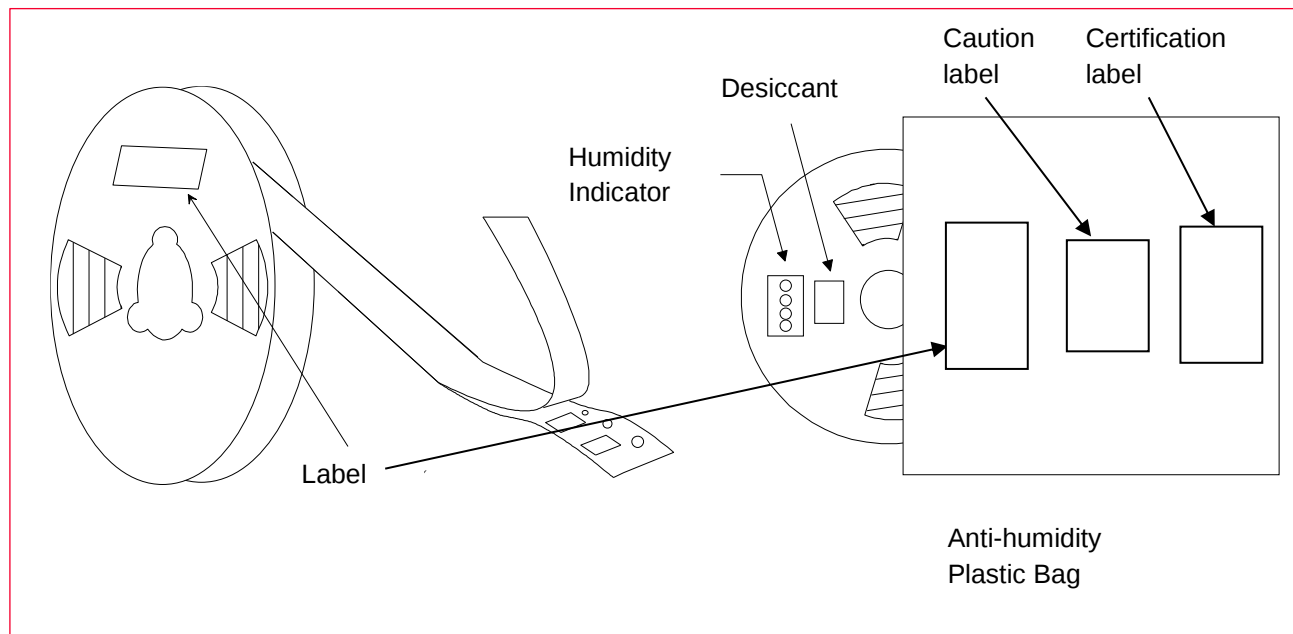
**Figure 33: Peeling Force**



## 16.5 Humidity Proof Packaging

**Figure 34** shows the humidity proof packaging.

**Figure 34: Humidity Proof Packaging**



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

## 17 Notice

### 17.1 Storage Conditions

Please use this product within 6 months after receipt.

- The product must be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH.



- Packing materials, in particular, may be deformed at the temperature over 40 °C

- The solderability of the product left idle for more than 6 months after receipt needs to be confirmed before it is used.
- The product must be stored in noncorrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>2</sub>, NO<sub>x</sub>, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object, and dropping the product, must not be applied as that will damage the packing materials.

This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)

- After the packing is opened, the product must be stored at <30 °C / <60 %RH and the product *should be* used within 168 hours after opening.
- When the color of the indicator in the packing is changed, the product *should be* baked before soldering.
- **Baking condition:** 125 +5/-0 °C, 24 hours, 1 time



- The products must be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

### 17.2 Handling Conditions

Be careful while handling or transporting products because excessive stress or mechanical shock may break the products.

Handle with care if you suspect that products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. *Do not touch* products with bare hands as that may cause poor solderability and cause damage by static electrical charge.

### 17.3 Standard PCB Design (Land Pattern and Dimensions)

All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.

The recommended land pattern and dimensions should be as per Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set.



- When using non-standard lands, contact Murata in advance.

## 17.4 Notice for Chip Placer

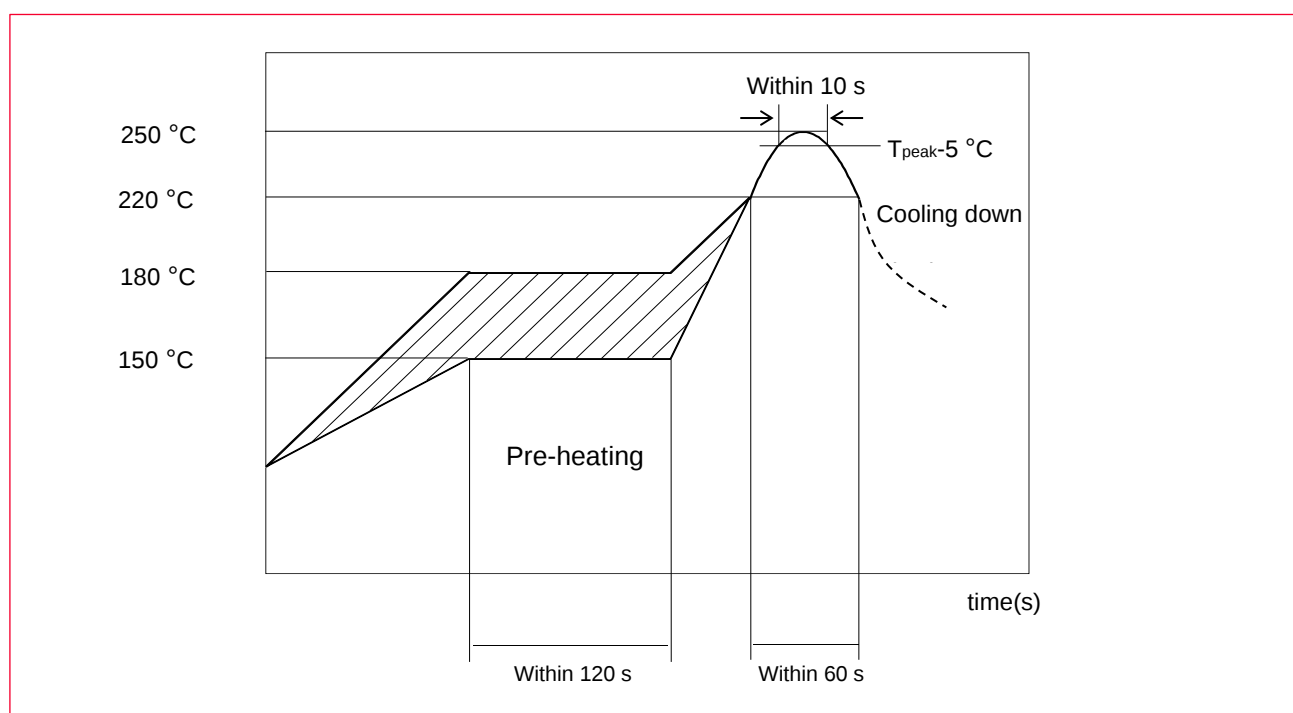
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

## 17.5 Soldering Conditions

The recommendation conditions of soldering are as in **Figure 35**.

Soldering must be carried out by the above-mentioned conditions to prevent products damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use concerning other soldering conditions.

**Figure 35: Reflow Soldering Standard Conditions (Example)**



- Please use the reflow within 2 times.
- Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt. % or less.

## 17.6 Cleaning

Since this Product is Moisture Sensitive, cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused such process.

## 17.7 Operational Environment Conditions

Murata products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, there is no problem in using the products under the above-mentioned conditions. However, using the products under the following circumstances may damage products and cause electricity leakage and abnormal temperature may occur:

- In atmosphere containing corrosive gas (Cl<sub>2</sub>, NH<sub>3</sub>, SO<sub>x</sub>, NO<sub>x</sub> etc.).
- In atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.



- If there is any chance of using the products under the conditions listed above, consult with Murata before actual use.



- Do not apply static electricity or excessive voltage while assembling and measuring the products, as it might be a cause of degradation or destruction to apply static electricity to products.

## 17.8 Input Power Capacity

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case the components are used beyond such input power capacity range.

## 18 Precondition to Use Our Products



- PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

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You shall indemnify and hold harmless us, our affiliates, and our licensor from and against any and all claims, costs, expenses and liabilities (including attorney's fees), which arise in connection with the using the Software.

The product shall not be used in any application listed below which requires especially high reliability for the prevention of such defect as may directly cause damage to the third party's life, body or property. You acknowledge and agree that, if you use our products in such applications, we will not be responsible for any failure to meet such requirements. Furthermore, YOU AGREE TO INDEMNIFY AND DEFEND US AND OUR AFFILIATES AGAINST ALL CLAIMS, DAMAGES, COSTS, AND EXPENSES THAT MAY BE INCURRED, INCLUDING WITHOUT LIMITATION, ATTORNEY FEES AND COSTS, DUE TO THE USE OF OUR PRODUCTS AND THE SOFTWARE IN SUCH APPLICATIONS.

- Aircraft equipment.
- Aerospace equipment.
- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.

- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.
- We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

Even in the unlikely event that an abnormality or malfunction occurs in this product under operating conditions that conform to the specifications, be sure to add an appropriate fail-safe function to the system to prevent secondary accidents.

We do not warrant or represent that any license, either express or implied, is granted under any our patent right, copyright, mask work right, or our other intellectual property right relating to any combination, machine, or process in which our products or services are used. Information provided by us regarding third-party products or services does not constitute a license from us to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from us under our patents or other intellectual property.

Please do not use our products, our technical information and other data provided by us for the purpose of developing of mass-destruction weapons and the purpose of military use.

Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

By signing on specification sheet or approval sheet, you acknowledge that you are the legal representative for your company and that you understand and accept the validity of the contents herein. When you are not able to return the signed version of specification sheet or approval sheet within 30 days from receiving date of specification sheet or approval sheet, it shall be deemed to be your consent on the content of specification sheet or approval sheet. Customer acknowledges that engineering samples may deviate from specifications and may contain defects due to their development status. We reject any liability or product warranty for engineering samples. In particular we disclaim liability for damages caused by

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- Deviation or lapse in function of engineering sample,
- Improper use of engineering samples.
- We disclaim any liability for consequential and incidental damages.

This Precondition to Use Our Products stipulated in this datasheet can only be modified, amended or altered by documents that explicitly reflect the mutual consent of both parties (including instances where one party explicitly indicates its acceptance of terms provided by the other party through click-through agreements).

If you can't agree with the above contents, please contact sales.

## Revision History

| Revision Code | Date         | Changed Item                                                                                                                                                                                                    | Comment                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------------|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1             | Jul 09, 2020 | First Issue                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2<br>(A)      | Dec 10, 2020 | 1. Scope<br>8. Absolute Maximum Ratings<br>9. Operating Conditions<br>13. DC / RF Characteristics<br>16. Tape and Reel Packing<br>17.6 Cleaning<br>15. Radio Regulatory Certification by Country for LBEE5PK2AE | <ul style="list-style-type: none"> <li>• Update</li> <li>• Update</li> <li>• Update</li> <li>• Update</li> <li>• Update</li> <li>• Update</li> <li>• Updated regulatory statement</li> </ul>                                                                                                                                                                                                                    |
| 3<br>(B)      | Dec 17, 2020 | 3. Ordering Information<br>6. Dimensions, Marking and Terminal Configurations<br>13. DC/RF Characteristics<br>13.7.2 Low-Rate Condition for IEEE 802.11n(HT40) – 5 GHz<br>16. Tape and Reel Packing             | <ul style="list-style-type: none"> <li>• Corrected part number</li> <li>• Correction</li> <li>• Correction</li> <li>• Correction</li> <li>• Correction</li> </ul>                                                                                                                                                                                                                                               |
| 4<br>(C)      | Apr 04, 2021 | 13. DC / RF Characteristics                                                                                                                                                                                     | <ul style="list-style-type: none"> <li>• Update</li> </ul>                                                                                                                                                                                                                                                                                                                                                      |
| 5<br>(D)      | Dec 17, 2021 | 6. Dimensions, Marking and Terminal Configurations                                                                                                                                                              | <ul style="list-style-type: none"> <li>• Updated module height</li> </ul>                                                                                                                                                                                                                                                                                                                                       |
| 6<br>(E)      | Dec 29, 2021 | 7.2 Pin Descriptions                                                                                                                                                                                            | <ul style="list-style-type: none"> <li>• Updated bandgap reference resistor to 4.75K ohm +/-1%.</li> </ul>                                                                                                                                                                                                                                                                                                      |
| 7<br>(F)      | Feb 02, 2022 | 1. Scope<br>5.2 Bluetooth Qualification                                                                                                                                                                         | <ul style="list-style-type: none"> <li>• Updated BT 5.2</li> <li>• Updated Bluetooth QDID</li> </ul>                                                                                                                                                                                                                                                                                                            |
| 8<br>(G)      | Apr 06, 2022 | 2. Key Features<br>4. Block Diagram<br>7.1 Module Pin Layout<br>7.4 Strapping Option<br>13. DC / RF Characteristics                                                                                             | <ul style="list-style-type: none"> <li>• Updated host interface.</li> <li>• Update</li> <li>• Updated terminal configuration.</li> <li>• Update</li> <li>• Update</li> </ul>                                                                                                                                                                                                                                    |
| 9<br>(H)      | Jun 14, 2022 | 1. Scope                                                                                                                                                                                                        | <ul style="list-style-type: none"> <li>• Updated IC P/N</li> </ul>                                                                                                                                                                                                                                                                                                                                              |
| 10<br>(I)     | Aug 18, 2022 | 13. DC/RF Characteristics                                                                                                                                                                                       | <ul style="list-style-type: none"> <li>• Update</li> </ul>                                                                                                                                                                                                                                                                                                                                                      |
| 11<br>(J)     | Nov 01, 2022 | 5. Certification information<br>7.2 Pin Descriptions<br><br>Reference schematic<br>15. Radio Regulatory Certification by Country for LBEE5PK2AE                                                                 | <ul style="list-style-type: none"> <li>• Update</li> <li>• Updated JTEG_SEL description.</li> <li>• Update</li> <li>• Updated Add APPENDIX of user/installation manual.</li> <li>• Removed Primary</li> </ul>                                                                                                                                                                                                   |
| 12<br>(K)     | Nov 30, 2022 | Reference schematic<br>13. DC/RF Characteristics                                                                                                                                                                | <ul style="list-style-type: none"> <li>• Corrected strap setting for USB.</li> <li>• Revised Wi-Fi RX current</li> </ul>                                                                                                                                                                                                                                                                                        |
| 13<br>(L)     | Sep 13, 2023 | 1. Scope<br><br>3. Ordering Information<br>6. Dimensions, Marking and Terminal Configurations<br>Reference Circuit<br>Appendix                                                                                  | <ul style="list-style-type: none"> <li>• Updated information. Created new section 'Key Features'.</li> <li>• Renamed part number section.</li> <li>• Created new section 'Module Pin Descriptions'</li> <li>• Moved section to HW app note.</li> <li>• Moved Appendix information into Sections 15 and 16.</li> <li>• Added transmit power tables.</li> <li>• Moved antenna sections to HW app note.</li> </ul> |

| Revision Code | Date          | Changed Item                                                                                            | Comment                                                                                                                                                           |
|---------------|---------------|---------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|               |               |                                                                                                         | Updated to new format                                                                                                                                             |
| 14 (M)        | Jul 04, 2024. | 7.3 SDIO Pin Descriptions                                                                               | <ul style="list-style-type: none"> <li>Revised the Pin No of the SDIO signal</li> </ul>                                                                           |
| 15 (N)        | Sep 10, 2024  | 2. Key Future<br>3 Ordering Information<br>15. Radio Regulatory Certification by Country for LBEE5PK2AE | <ul style="list-style-type: none"> <li>Add Fit Value</li> <li>Remove 2AE-EVB pats No</li> <li>Remove certification information</li> </ul>                         |
| 16            | Aug 8, 2025   | 15 DC/RF Characteristics<br>17 Notice<br>18 Precondition to Use Our Products                            | <ul style="list-style-type: none"> <li>Format changed</li> <li>Format changed</li> <li>Format changed</li> <li>Updated (Base IC datasheet revision: A)</li> </ul> |



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