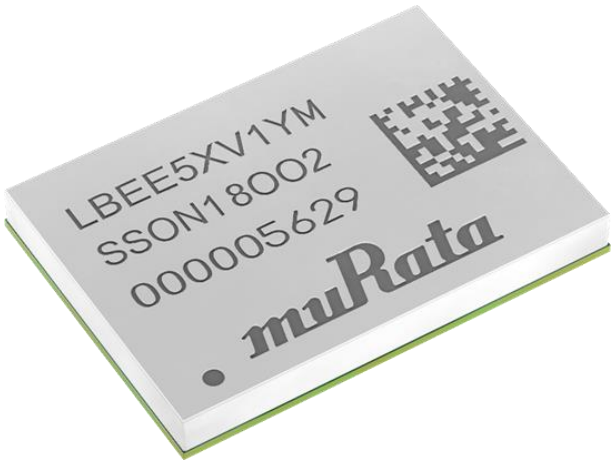
Datasheet

Type 1YM Wi-Fi™ + Bluetooth® Module

NXP 88W8997 Chipset for 802.11a/b/g/n/ac 2x2 MIMO + Bluetooth 5.2 Datasheet - Rev.21

- Design Name: Type 1YM
- P/N: LBEE5XV1YM-574



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About This Document

Murata's Type 1YM is a small and high-performance module based on NXP 88W8997 combo chipset, supporting IEEE 802.11a/b/g/n/ac 2x2 MIMO + Bluetooth 5.2 BR/EDR/LE. This datasheet describes Type 1YM module in detail.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product; specifically RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Embedded Artists AB Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This specification applies to the IEEE 802.11a/b/g/n/ac WLAN 2x2 MU-MIMO + Bluetooth 5.2 combo module.

2 Key Features

- NXP 88W8997 inside
- Supports IEEE 802.11a/b/g/n/ac specification: Dual band 2.4 GHz and 5 GHz
- MU-MIMO with 20 MHz, 40 MHz, and 80 MHz channels
- Up to MCS9 data rates (866 Mbps)
- Supports Bluetooth specification version 5.2
- For supported Bluetooth functions, refer to Bluetooth SIG site
- WLAN interface: PCIe 3.0, SDIO 3.0, USB 2.0 & 3.0
- Bluetooth interface: HCI UART, SDIO 3.0, USB 2.0 & 3.0, and PCM
- Temperature Range: - 30 °C to 85 °C
- Dimensions: 11.8 x 8.4 x 1.3 mm
- Weight: 352 mg
- MSL: 3
- Surface-mount type
- RoHS compliant
- Total FIT: 88

WLAN-USB, Bluetooth-SDIO, and Bluetooth-USB interfaces may not be supported.
Refer to Type 1YM webpage or check 1YM Community Forum page.

3 Ordering Information

Table 2 shows the ordering information for Type 1YM module.

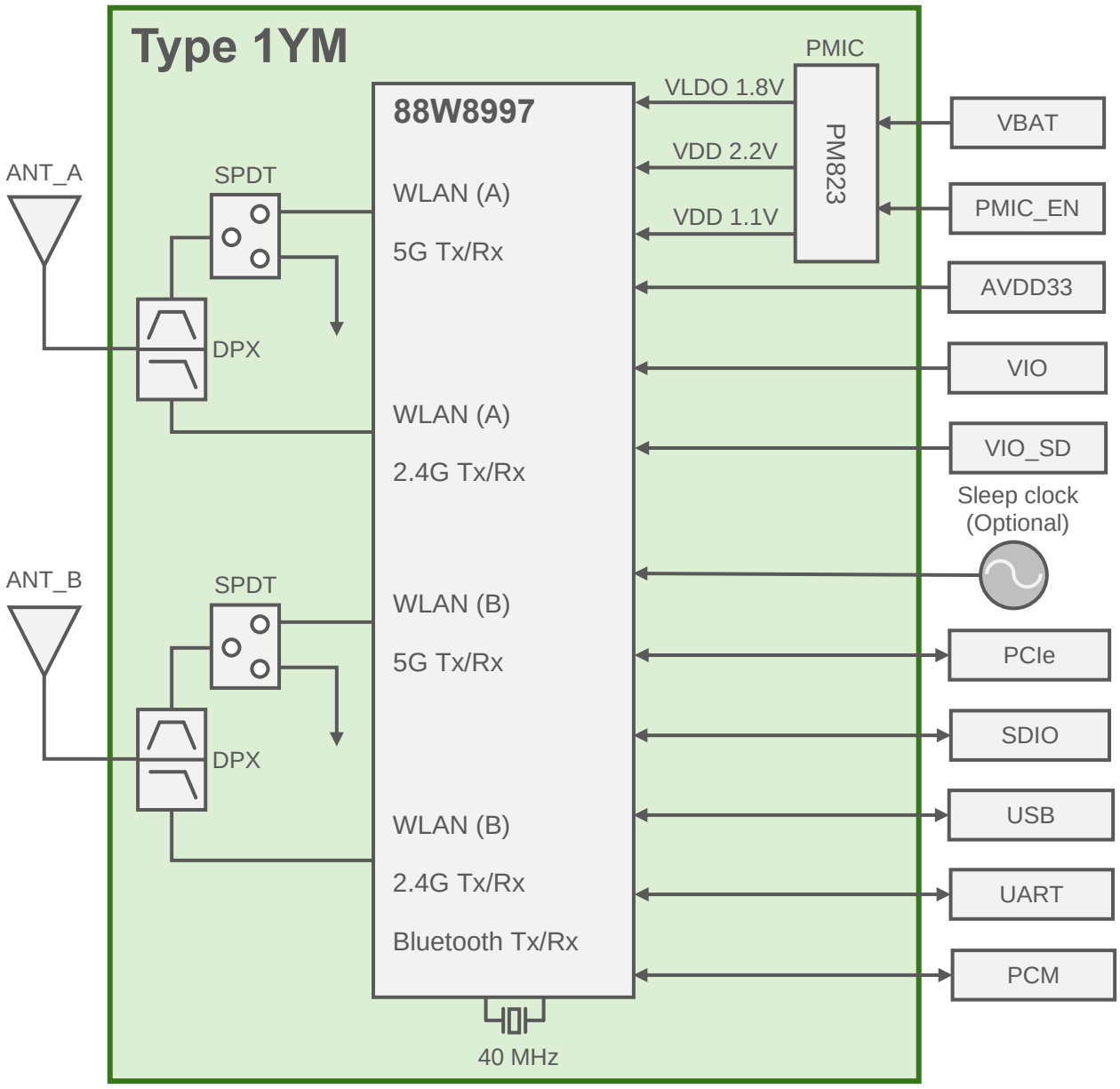
Table 2: Ordering Information

Ordering Part Number	Description
LBEE5XV1YM-574	Module order
LBEE5XV1YM-SMP	Sample module order (If module samples are not available through distribution, contact Murata referencing this part number)
EAR00370	Embedded Artists Type 1YM M.2 EVB (default EVB available through distribution)

4 Block Diagram

The Type 1YM block diagram is presented in **Figure 1**.

Figure 1: Block Diagram



WLAN-USB, Bluetooth-SDIO, and Bluetooth-USB interfaces may not be supported.
Refer to Type 1YM webpage or check 1YM Community Forum page.

5 Certification Information

This section has information about radio and Bluetooth certification.

5.1 Radio Certification

Transmit output power setting is defined by "txpower_XX.bin" (XX is country code). The transmit power files are hosted at Murata GitHub for Linux. **Table 3** shows the transmit power file required for each region.

Table 3: Transmit Power Limit Files

Country	ID	Country Code	Tx Power Limit File
USA (FCC)	VPYLB1YM	US	txpower_US.bin
Canada (IC)	772C-LB1YM	CA	txpower_CA.bin
Europe	EN300328/301893, EN300440 conducted test report is prepared.	DE	txpower_EU.bin
Japan	Japanese type certification is prepared. Ⓡ 001-P01563	JP	txpower_JP.bin

Each country code is defined by Murata's db.txt file. Please ask your contact person from Murata.

5.2 Bluetooth Qualification

- QDID: 157698
- Set Bluetooth Tx Power to Class 1 by using bt_power_config_1.sh.
- For PICS for supported Bluetooth functions refer to Bluetooth SIG site.

6 Dimensions, Markings and Terminal Configurations

This section has information on dimensions, marking, and terminal configurations for Type 1YM.

Figure 2: Dimensions, Markings, and Terminal Configurations

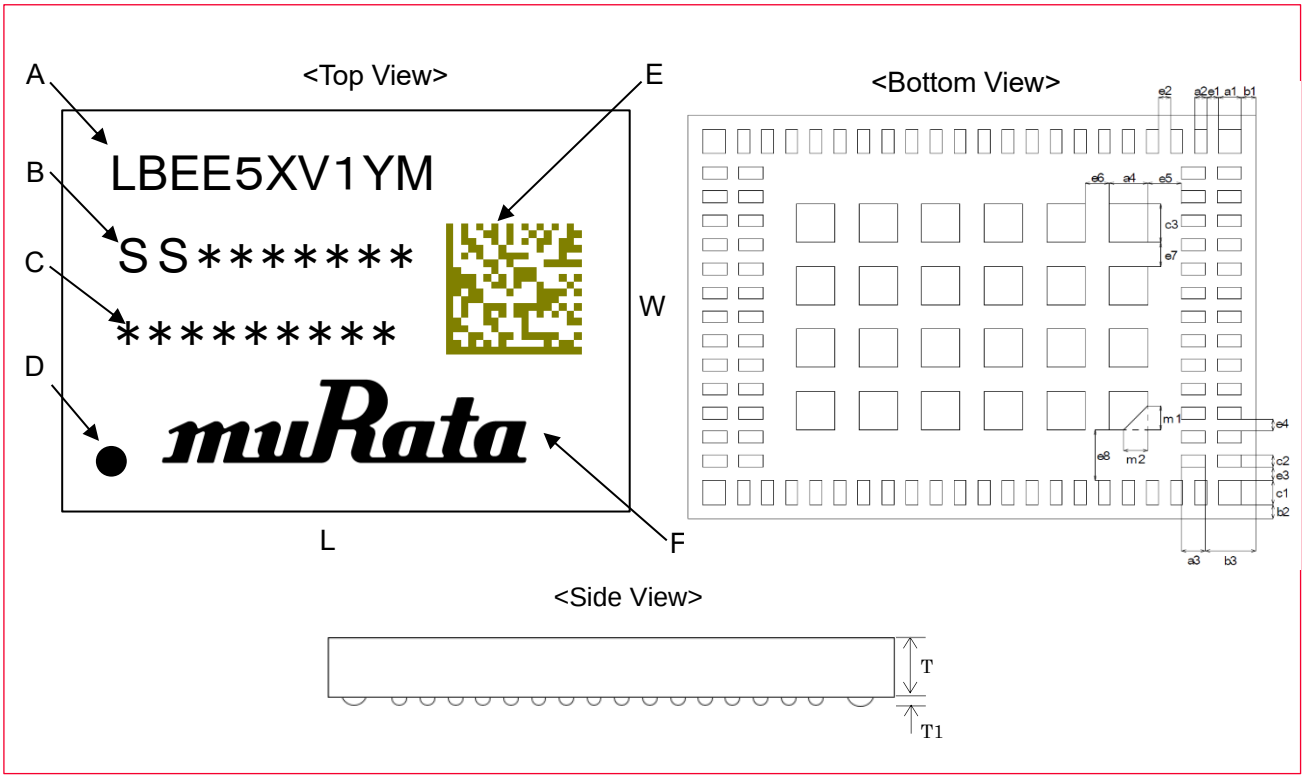
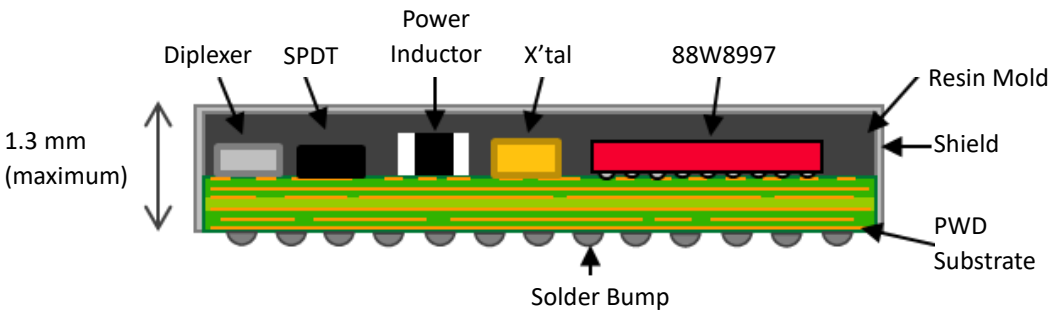


Table 4: Markings

Marking	Meaning
A	Module Type
B	Production Process Number
C	Serial Number
D	Pin 1 Marking
E	2D code
F	Murata Logo

Table 5: Dimensions

Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)
L	11.8 ± 0.2	W	8.4 ± 0.2	T	1.3 maximum	a1	0.475 ± 0.1
a2	0.25 ± 0.1	a3	0.5 ± 0.2	a4	0.8 ± 0.1	b1	0.3 ± 0.2
b2	0.3 ± 0.2	b3	1.05 ± 0.2	c1	0.5 ± 0.1	c2	0.25 ± 0.1
c3	0.8 ± 0.1	e1	0.25 ± 0.1	e2	0.25 ± 0.1	e3	0.25 ± 0.1
e4	0.25 ± 0.1	e5	0.7 ± 0.1	e6	0.5 ± 0.1	e7	0.5 ± 0.1
e8	1.05 ± 0.1	m1	0.5 ± 0.2	m2	0.5 ± 0.2	T1	0.045 typical



The sides of the module are GND shielded. In order to avoid contact between the GND shield and the electrodes on the mother board, please carefully evaluate the standoff before use the module.

7 Module Pin Descriptions

This section has the pin descriptions of Type 1YM and pin assignments layout descriptions.

7.1 Pin Assignments

The pin assignment layout (Top View) is shown in **Figure 3**.

Figure 3: Pin Assignments (Top View)

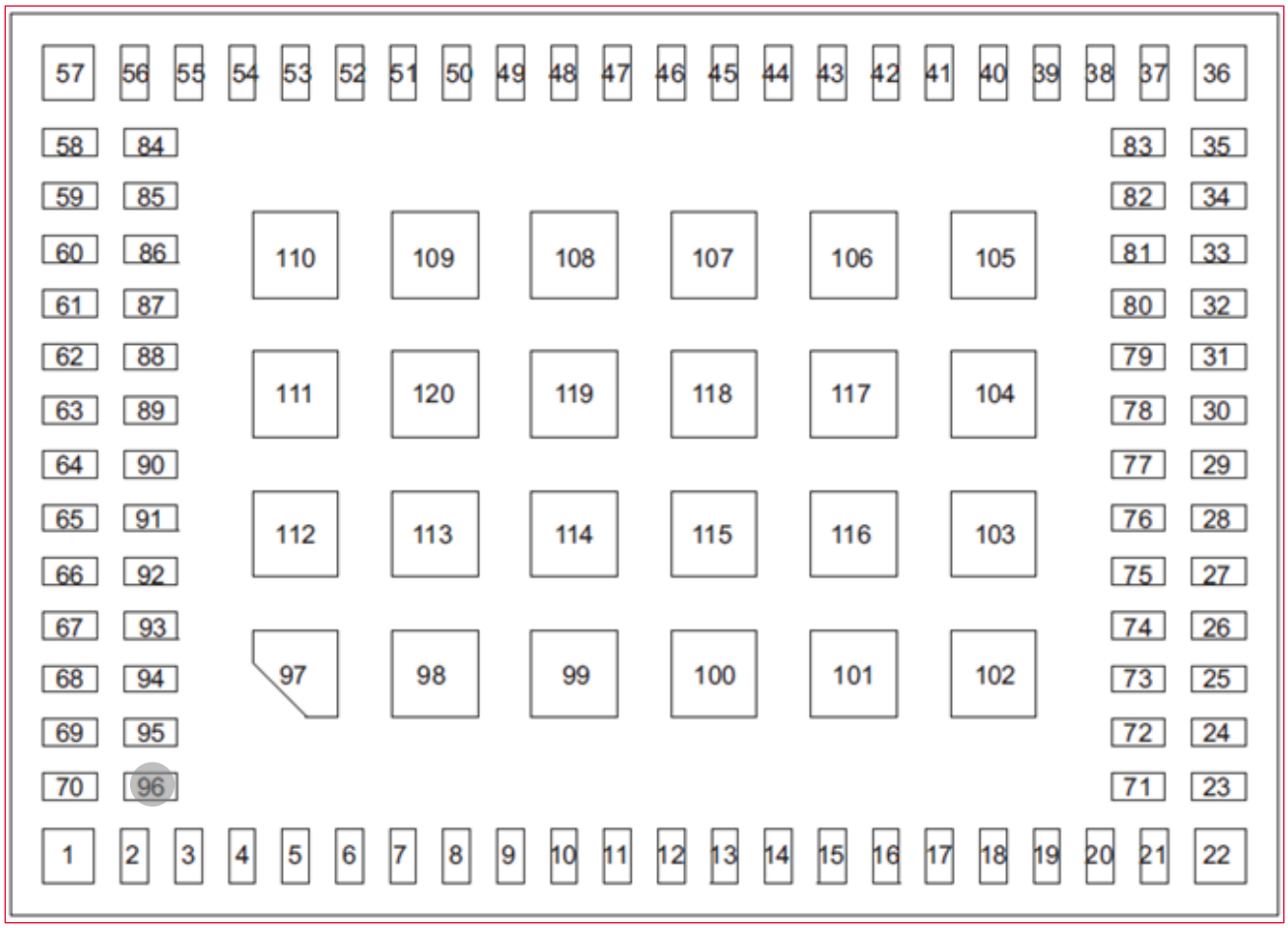


Table 6 illustrates the terminal configurations.

Table 6: Terminal Configurations

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	29	GND	57	GND
2	GPIO[24]	30	PMIC_EN	58	GND
3	GPIO[3]	31	GPIO[21]	59	WLAN_RF_A
4	GPIO[2]	32	PCIE_WAKE_N	60	GND
5	GPIO[17]	33	GPIO[5]	61	GPIO[6]
6	GPIO[16]	34	DNC	62	GPIO[9]
7	GPIO[15]	35	DNC	63	GPIO[8]
8	GPIO[14]	36	GND	64	GPIO[13]
9	VIO	37	GND	65	GPIO[10]
10	GPIO[20]	38	GND	66	GPIO[11]
11	GPIO[25]	39	PCIE_RXP	67	GPIO[12]
12	GND	40	PCIE_RXN	68	GND
13	NC	41	PCIE_TXP	69	WLAN_RF_B
14	NC	42	PCIE_TXN	70	GND
15	GND	43	PCIE_CLKP	71	GPIO[26]
16	VIO_SD	44	PCIE_CLKN	72	GPIO[27]
17	AVDD33	45	GND	73	GPIO[18]
18	SD_D1	46	GPIO[4]	74	GND
19	SD_D0	47	GPIO[0]	75	VBAT
20	SD_CLK	48	DNC	76	VBAT
21	SD_CMD	49	DNC	77	GND
22	GND	50	AVDD18	78	GPIO[1]
23	SD_D3	51	DNC	79	GPIO[23]
24	SD_D2	52	CONFIG_HOST_3	80	GPIO[22]
25	GPIO[19]	53	CONFIG_HOST_2	81	GPIO[7]
26	GND	54	CONFIG_HOST_1	82	PCIE_CLKREQ_N
27	VBAT	55	CONFIG_HOST_0	83	DNC
28	VBAT	56	SLP_CLK	84-120	GND

7.2 Pin Descriptions

Table 7 describes Type 1YM pins.

Table 7: Pin Descriptions

No.	Pin name	Type	Connection to IC Pin Name[1]	Description
1	GND	Ground		Ground
2	GPIO[24]	I/O	GPIO[24]	Programmable GPIO
3	GPIO[3]	I/O	GPIO[3]	Programmable GPIO
4	GPIO[2]	I/O	GPIO[2]	Programmable GPIO
5	GPIO[17]	I/O	GPIO[17]	Programmable GPIO
6	GPIO[16]	I/O	GPIO[16]	Programmable GPIO
7	GPIO[15] (HOST_WAKEUP_WLAN)[2]	I/O	GPIO[15]	Programmable GPIO

[1] ( ) of “pin name” is BSP configuration of NXP iMX8.
[2] NXP recommended GPIO. Check whether NXP software can support this function or not

No.	Pin name	Type	Connection to IC Pin Name[1]	Description
8	GPIO[14] (WLAN_WAKEUP_HOST[2]	I/O	GPIO[14]	Programmable GPIO
9	VIO	Power	VIO	Power Supply
10	GPIO[20]	I/O	GPIO[20]	Programmable GPIO
11	GPIO[25]	I/O	GPIO[25]	Programmable GPIO
12	GND	Ground		Ground
13	NC	I/O	USB_DMNS	USB Serial Differential Data-Negative
14	NC	I/O	USB_DPLS	USB Serial Differential Data-Positive
15	GND	Ground		Ground
16	VIO_SD	Power	VIO_SD	1.8V/3.3V Digital I/O SDIO Power Supply
17	AVDD33	Power	AVDD33	3.3V Analog Power Supply
18	SD_D1	I/O	SD_DAT[1]	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
19	SD_D0	I/O	SD_DAT[0]	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line
20	SD_CLK	I/O	SD_CLK	SDIO 4-bit mode: Clock SDIO 1-bit mode: Clock
21	SD_CMD	I/O	SD_CMD	SDIO 4-bit mode: Command line SDIO 1-bit mode: Command line
22	GND	Ground		Ground
23	SD_D3	I/O	SD_DAT[3]	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Not used
24	SD_D2	I/O	SD_DAT[2]	SDIO 4-bit mode: Data line Bit[2] or Read Wait (optional) SDIO 1-bit mode: Interrupt (optional)
25	NC (GPIO [19])	I/O	GPIO[19] DVS1(PMIC)	NC
26	GND	Ground		Ground
27	VBAT	Power	PVIN(PMIC)	Power Supply
28	VBAT	Power	PVIN(PMIC)	Power Supply
29	GND	Ground		Ground
30	PMIC_EN	I	EN(PMIC)	Enable build-in PMIC. Logic high enables internal regulators and internal hardware reset is de-asserted. Logic low disables regulators and internal hardware reset is asserted. **Do not float this pin**
31	GPIO[21]	I/O	GPIO[21]	Programmable GPIO
			PCIE_PERSTn	PCIe host indication to reset the device (input) (active low)
32	PCIE_WAKE_N	I/O	PCIE_WAKEn	PCIe wake signal (active low)
33	GPIO[5] (BT_PCM_DOUT)	I/O	GPIO[5]	Programmable GPIO
		O	PCM_DOUT	PCM Data
34	NC			No Connect
35	NC			No Connect
36	GND	Ground		Ground
37	GND	Ground		Ground
38	GND	Ground		Ground
39	PCIE_RXP	I	PCIE_RX_P	PCI Express Lane 0, Receive Pair, Positive Signal 2.5 GHz serial low-voltage interface
			USB3_RX_P	USB 3.0 receive data - positive

No.	Pin name	Type	Connection to IC Pin Name[1]	Description
40	PCIE_RXN	O	PCIE_RX_N	PCI Express Lane 0, Receive Pair, Negative Signal 2.5 GHz serial low-voltage interface
			USB3_RX_N	USB 3.0 receive data - negative
41	PCIE_TXP	O	PCIE_TX_P	PCI Express Lane 0, Transmit Pair, Positive Signal 2.5 GHz serial low-voltage interface
			USB3_TX_P	USB3.0 transmit data - positive
42	PCIE_TXN	O	PCIE_TX_N	PCI Express Lane 0, Transmit Pair, Negative Signal 2.5 GHz serial low-voltage interface
			USB3_TX_N	USB3.0 transmit data - negative
43	PCIE_CLKP	I	PCIE_RCLK_P	PCI Express Platform Reference Clock Positive signal of differential pair 100 MHz low-voltage interface
44	PCIE_CLKN	I	PCIE_RCLK_N	PCI Express Platform Reference Clock Negative signal of differential pair 100 MHz low-voltage interface
45	GND	Ground		Ground
46	GPIO[4] (BT_PCM_DIN)	I/O	GPIO[4]	Programmable GPIO
		I	PCM_DIN	PCM Data
47	GPIO[0]	I/O	GPIO[0]	Programmable GPIO Oscillator Mode: XOSC_EN/CLK_REQ(output)(active high) 0 = disable external oscillator 1 = enable external oscillator *Internal Pull-up
48	DNC		DNC	Do Not Connect
49	DNC		DNC	Do Not Connect
50	AVDD18	O	VLDO(PMIC)	LDO Output. Use for CONFIG_HOST pull-up.
51	DNC	DNC	DNC	Do Not Connect
52	CONFIG_HOST_3		CONFIG_HOST[3]	Configuration interface[3] See Section 4.2
53	CONFIG_HOST_2		CONFIG_HOST[2]	Configuration interface[2] See Section 4.2
54	CONFIG_HOST_1		CONFIG_HOST[1]	Configuration interface[1] See Section 4.2
55	CONFIG_HOST_0		CONFIG_HOST[0]	Configuration interface[0] See Section 4.2
56	SLP_CLK	I	SLP_CLK_IN	**Sleep Clock Input** Used for WLAN and Bluetooth low power modes. If no sleep clock input is provided, an internal sleep clock (derived from reference clock) will be used. if SLP_CLK is not connected, the internal circuit will detect no signal, and firmware will initialize the sleep clock based on the reference clock.

No.	Pin name	Type	Connection to IC Pin Name[1]	Description
57	GND	Ground		Ground
58	GND	Ground		Ground
59	WLAN_RF_A	I/O	RF_TR_2_A RF_TR_5_A	RF Transmit / Receive (2.4G/5 GHz) - PathA
60	GND	Ground		Ground
61	GPIO[6] (BT_PCM_CLK)	I/O	GPIO[6]	Programmable GPIO
		I/O	PCM_CLK	PCM Clock Signal Output if PCM master. Input if PCM slave.
		O	PCM_MCLK	PCM Clock Signal (optional) Optional clock used for some codecs. Derived from PCM_CLK.
62	GPIO[9] (BT_UART_RXD)	I/O	GPIO[9]	Programmable GPIO
		I	UART_SIN	Serial data Input from modem, data set, or peripheral device.
63	GPIO[8] (BT_UART_TXD)	I/O	GPIO[8]	Programmable GPIO
		O	UART_SOUT	Serial data Output to modem, data set, or peripheral device.
64	GPIO[13] (BT_WAKEUP_HOST)[2]	I/O	GPIO[13]	Programmable GPIO
		O	UART_DTRn	Data Terminal Ready Output to modem, data set, or peripheral device (active low).
65	GPIO[10] (BT_UART_CTSn)	I/O	GPIO[10]	Programmable GPIO
		I	UART_CTSn	Clear To Send Input from modem, data set, or peripheral device (active low).
66	GPIO[11] (BT_UART_RTSn)	I/O	GPIO[11]	Programmable GPIO
		O	UART_RTSn	Request To Send Output to modem, data set, or peripheral device (active low).
67	GPIO[12] (HOST_WAKEUP_BT)[2]	I/O	GPIO[12]	Programmable GPIO
		I	UART_DSRn	Data Set Ready Input from modem, data set, or peripheral device (active low).
68	GND	Ground		Ground
69	WLAN_RF_B	I/O	RF_TR_2_A RF_TR_5_A	RF Transmit / Receive (2.4G/5 GHz) - PathB
70	GND	Ground		Ground
71	GPIO[26]	I/O	GPIO[26]	Programmable GPIO
72	GPIO[27]	I/O	GPIO[27]	Programmable GPIO
73	NC (GPIO[18])	I/O	GPIO[18] DVS0(PMIC)	NC
74	GND	Ground		Ground
75	VBAT	Power	PVIN(PMIC)	Power Supply
76	VBAT	Power	PVIN(PMIC)	Power Supply
77	GND	Ground		Ground
78	GPIO[1] (USB_VBUS_ON)	I/O	GPIO[1]	Programmable GPIO

No.	Pin name	Type	Connection to IC Pin Name[1]	Description
79	GPIO[23]	I/O	GPIO[23]	Programmable GPIO
80	GPIO[22]	I/O	GPIO[22]	Programmable GPIO
			PCIE_W_DISABLEn	PCIe host indication to disable the WLAN function of the device (input) (active low)
81	GPIO[7] (BT_PCM_SYNC)	I/O	GPIO[7]	Programmable GPIO
		I/O	PCM_SYNC	PCM Sync Pulse Signal Output if PCM master. Input if PCM slave.
82	PCIE_CLKREQ_N	I/O	PCIE_CLKRQn	PCI Express Wake Signal
83	NC			No Connect
84-120	GND	Ground		Ground

7.3 Configuration Pins

Table 8 shows the configuration pins for Type 1YM.

Table 8: Configuration Pins

Configuration Bits	Pin Name	Configuration Function
CON[2]	CONFIG_HOST[2]	Firmware Boot Options No hardware impacts. Software reads and boots accordingly. See **Table 9**.
CON[1]	CONFIG_HOST[1]	
CON[0]	CONFIG_HOST[0]	

Table 9 shows the firmware download modes.

Table 9: Firmware Download Mode

Strap Value	WLAN	Bluetooth/BLE	ROM Notes	Firmware Download Mode	Number of SDIO Functions
000	SDIO	UART		Parallel	1 (WLAN)
001	SDIO	SDIO		Parallel	2 (WLAN, Bluetooth)
010	PCIe	USB 2.0	Initialize USB 2.0 PHY and COM PHY PCIe portion	Parallel	
011	PCIe	UART	Initialize only COM PHY PCIe portion	Parallel	
100	USB 3.0/2.0	UART	Initialize both COM PHY USB 3.0 and USB 2.0 PHY	Parallel	
101	USB 2.0	USB 2.0	Initialize only USB 2.0 PHY	Parallel	
110	USB 3.0/2.0	USB 3.0/2.0	Initialize both COM PHY USB 3.0 and USB 2.0 PHY	Parallel	
111	USB3.0	USB 3.0	Initialize only COM PHY USB 3.0 portion	Parallel	

WLAN-USB, BT-SDIO, and BT-USB interfaces may not be supported.
Refer to Type 1YM webpage or check 1YM Community Forum page.

AVDD18 output can be used to pull-up CONFIG_HOST pins.

7.4 Pin States

Pin states information for the tables below include:

- After firmware is downloaded, the pads (GPIO, Serial interface, RF control) are programmed in functional mode per the functionality of the pins.
- For SDIO, once the command is received from the host, the pads are configured accordingly.
- Pull-up and pull-down are only effective when the pad is in input mode.
- The power-down state shown is the default configuration. Many pads have programmable power-down values, which can be set by firmware.
- Do not need any termination to the open pins in input mode that have an Internal Pull-up/Pull-down resistor (PU/PD). Do not need any termination to the open pins in output mode. Do not need any termination to PCIE signals, Pin 13 and Pin 14 in SDIO mode.

Table 10: I/O State Table

Pin Name	Supply	No Pad Power State	Reset State	HW State[3]	PD State[4]	PD Prog[5]	Internal PU/PD	Int'l Pull Value[Ω]
GPIO[0]	VIO	tristate	output	output	drive low	yes	nominal PU	90K
GPIO[1]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[2]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[3]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[4]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[5]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[6]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[7]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[8]	VIO	tristate	input	input	drive low	yes	weak PU	800K
GPIO[9]	VIO	tristate	input	input	tristate	yes	weak PU	800K
GPIO[10]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[11]	VIO	tristate	input	input	drive high	yes	weak PU	800K
GPIO[12]	VIO	tristate	input	input	tristate	yes	nominal PD	90K
GPIO[13]	VIO	tristate	input	input	drive high	yes	nominal PU	90K
GPIO[14]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[15]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[16]	VIO	tristate	input	input	tristate	yes	nominal PD	90K
GPIO[17]	VIO	tristate	input	input	tristate	yes	nominal PD	90K
GPIO[18]	VIO	tristate	input	input	tristate	yes	nominal PD	90K

[3] Hardware default state after reset
[4] Power-down state
[5] Power-down state programmable

Pin Name	Supply	No Pad Power State	Reset State	HW State[3]	PD State[4]	PD Prog[5]	Internal PU/PD	Int'l Pull Value[Ω]
GPIO[19]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[20]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[21]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[22]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[23]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[24]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[25]	VIO	tristate	input	input	drive high	yes	nominal PU	90K
GPIO[26]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO[27]	VIO	tristate	input	input	tristate	yes	nominal PU	90K
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PU	90K
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PU	90K
SD_D0	VIO_SD	tristate	input	input	tristate	no	nominal PU	90K
SD_D1	VIO_SD	tristate	input	input	tristate	no	nominal PU	90K
SD_D2	VIO_SD	tristate	input	input	tristate	no	nominal PU	90K
SD_D3	VIO_SD	tristate	input	input	tristate	no	nominal PU	90K
PCIE_CLKP	AVDD18							
PCIE_CLKN	AVDD18							
PCIE_TXP	AVDD18							
PCIE_TXN	AVDD18							
PCIE_RXP	AVDD18							
PCIE_RXN	AVDD18							
PCIE_WAKE_N	VIO	tristate	input	output	N/A	N/A	N/A	
PCIE_CLKREQ_N	VIO	tristate	input	output	N/A	N/A	N/A	
CONFIG_HOST_0	AVDD18	tristate	input	input	tristate	no	weak PU	800K
CONFIG_HOST_1	AVDD18	tristate	input	input	tristate	no	weak PU	800K
CONFIG_HOST_2	AVDD18	tristate	input	input	tristate	no	weak PU	800K
CONFIG_HOST_3	AVDD18	tristate	input	input	tristate	no	weak PU	800K
SLP_CLK_IN	VIO	tristate	input[6]	input	tristate	no	nominal PU	90K

8 Absolute Maximum Ratings

The absolute maximum ratings are shown in **Table 11.**

Table 11: Absolute and Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-30	+85	°C
Supply Voltage	VBAT		6.0	V
	VIO		2.2	V
			3.0	V
			4.0	V

[6] Input mode after reset

Parameter		Minimum	Maximum	Unit
	VIO_SD		2.2	V
			4.0	V
	AVDD33		4.0	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

9 Operating Conditions

This section describes the operating conditions and external sleep clock requirements.

9.1 Operating Conditions

The operating conditions are shown in **Table 12**.

Table 12: Operating Conditions

Parameter		Minimum	Typical	Maximum	Unit
Operating Temperature	Ta	-30		+85	°C
	Tj			+125	°C
Operating Voltage	VBAT	2.7		5.5	V
	VIO	1.62	1.8	1.98	V
		2.25	2.5	2.75	V
		2.97	3.3	3.47	V
	VIO_SD	1.62	1.8	1.98	V
		2.97	3.3	3.47	V
	AVDD33[7]	2.97	3.3	3.63	V
IO Current	VIO & VIO_SD		0.2	0.6	mA
Peak Current[8]	VBAT		1.0	1.3	A

Operation beyond the recommended operating conditions is neither recommended nor guaranteed.

[7] AVDD33 is used for only when USB interface is used.
[8] Peak current of VBAT (RF portion) is happen during DPD calibration when the firmware is downloaded.

9.2 External Sleep Clock Requirements

Table 13 shows the external sleep clock requirements of Type 1YM.

Table 13: External Sleep Clock Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Unit
CLK	Clock frequency range/accuracy: • CMOS input clock signal type • ±250 ppm (initial, aging, temperature		32.768		kHz
V_{IH}	Input levels, where VIO = 1.8, 2.5, 3.3 V	0.7*VIO		VIO+0.4	V
V_{IL}		-0.4		0.3*VIO	V
PN	Phase noise requirement (@ 100 kHz)		-125		dBc/Hz
J_c	Cycle jitter		1.5		ns (RMS)
SR	Slew rate limit (10-90%)			100	ns
DC	Duty cycle tolerance	20		80	%

Voltage input levels = 1.8V or 3.3V

9.3 MIC_EN I/O Requirement

Table 14 shows the PMIC_EN I/O requirements of Type1YM.

Table 14: PMIC_EN I/O Requirements

Symbol	Parameter	Minimum	Maximum	Unit
$V_{PMIC\_EN\_IH}$	Input high voltage	1.2		V
$V_{PMIC\_EN\_IL}$	Input low voltage		0.4	V

9.4 Digital I/O Requirements

Table 15 shows the digital I/O requirements of Type 1YM.

Table 15: Digital I/O Requirements Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high voltage		0.7*VIO		VIO+0.4	V
V_{IL}	Input low voltage		-0.4		0.3*VIO	V
V_{HYS}	Input hysteresis		100			mV
V_{OH}	Output high voltage		VIO-0.4			V
V_{OL}	Output low voltage				0.4	V

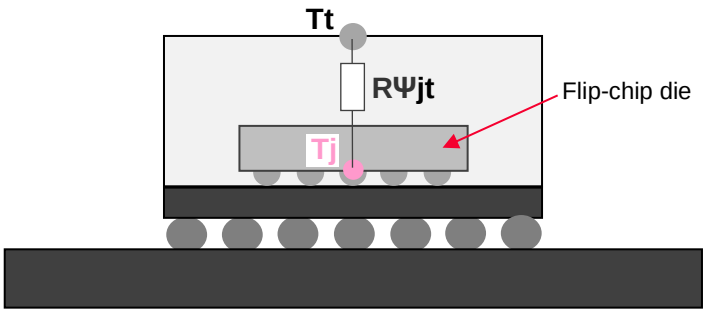
9.5 Package Thermal Conditions

The package thermal conditions are as below:

- **RΨjt :** 3.2℃/W
- **RΨjt** = (Tj - Tt)/P

> **Tj:** Junction temperature (°C), Tt: Top temperature (°C), P: Total Power Consumption (W)

Figure 4: Package Thermal Conditions



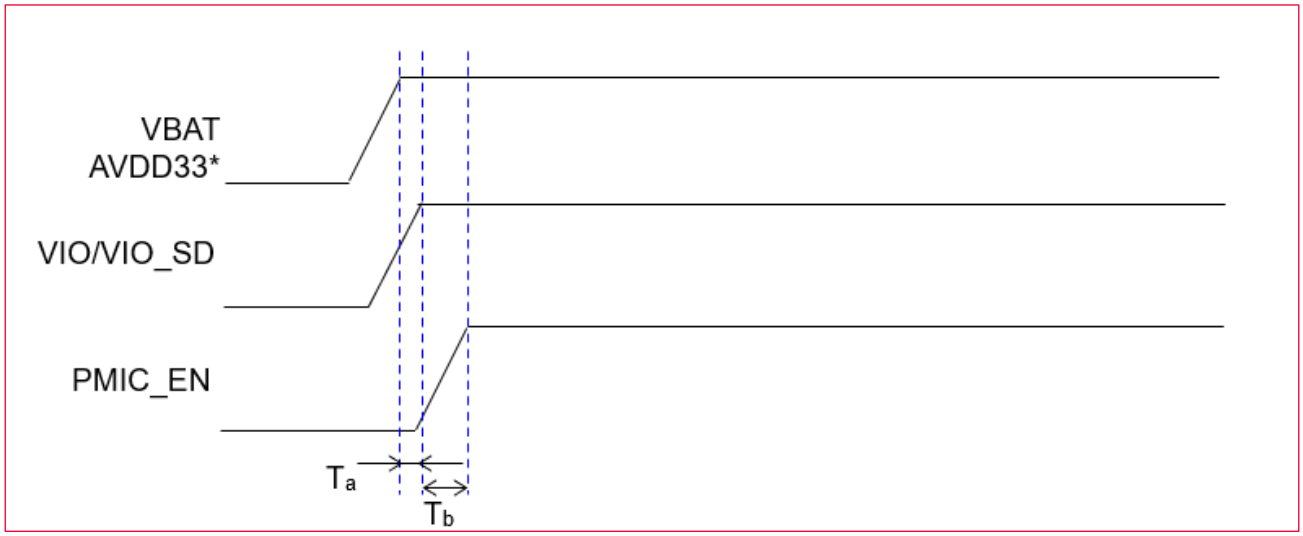
10 Power Sequence

This section describes the power-on and power-off sequences along with their parameters.

10.1 Power-On Sequence

- VBAT and VIO must be good (90%) at the same time or before assert PMIC_EN (= 0 to 1).
- Rump-up time of VIO must be < 100 ms.

Figure 5: Power-On Sequence Graph



AVDD33 is used for only when USB interface is used.

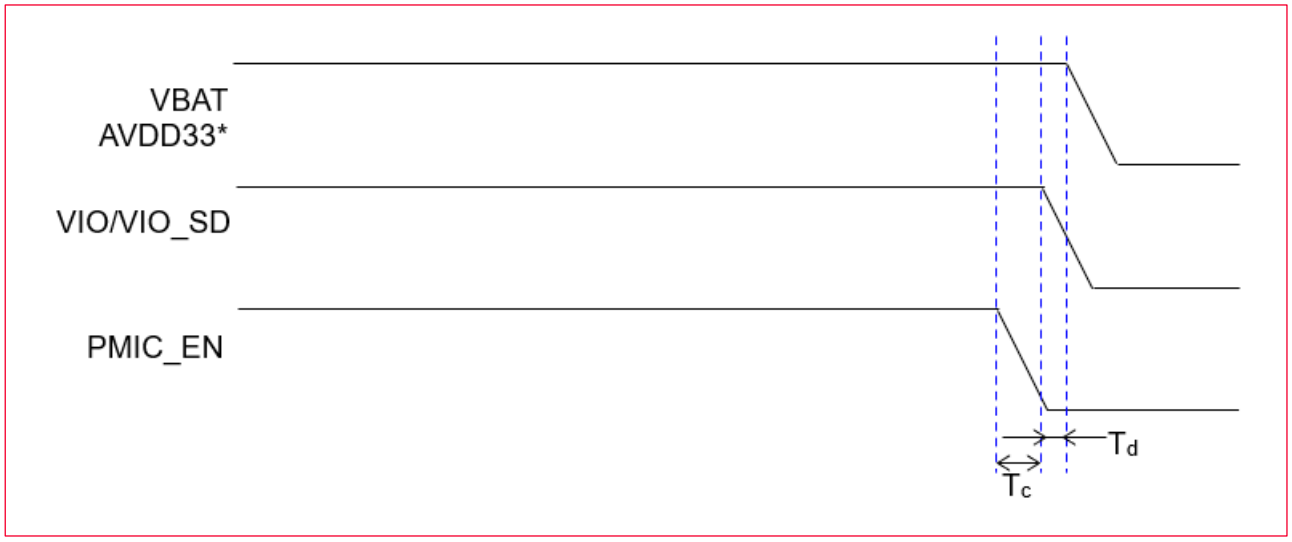
Table 16: Parameters for Power-On Sequence

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Ta	VBAT/AVDD33 to VIO time	0			ms
Tb	VIO to PMIC_EN time	0			ms

10.2 Power-Off Sequence

- VBAT and VIO must be down at the same time or before de-assert PMIC_EN (= 1 to 0).
- Rump-down time of VIO must be < 100 ms.

Figure 6: Power-Off Sequence Graph



AVDD33 is used for only when USB interface is used.

Table 17: Parameters for Power-Off Sequence

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_c	PMIC_EN to VIO time	0			ms
T_d	VIO to VBAT/AVDD33 time	0			ms

11 Host Interface Specification

This section describes the SDIO specification, its speed modes, related parameters, and graphs.

11.1 SDIO Specifications

- The SDIO host interface pins are powered from the VIO_SD voltage supply.
- The SDIO electrical specifications are identical for 4-bit SDIO and 1-bit SDIO transfer modes.

11.1.1 Default Speed, High Speed Modes

Figure 7 shows the default mode signals.

Figure 7: SDIO Protocol Timing Diagram - Default Speed Mode (3.3V)

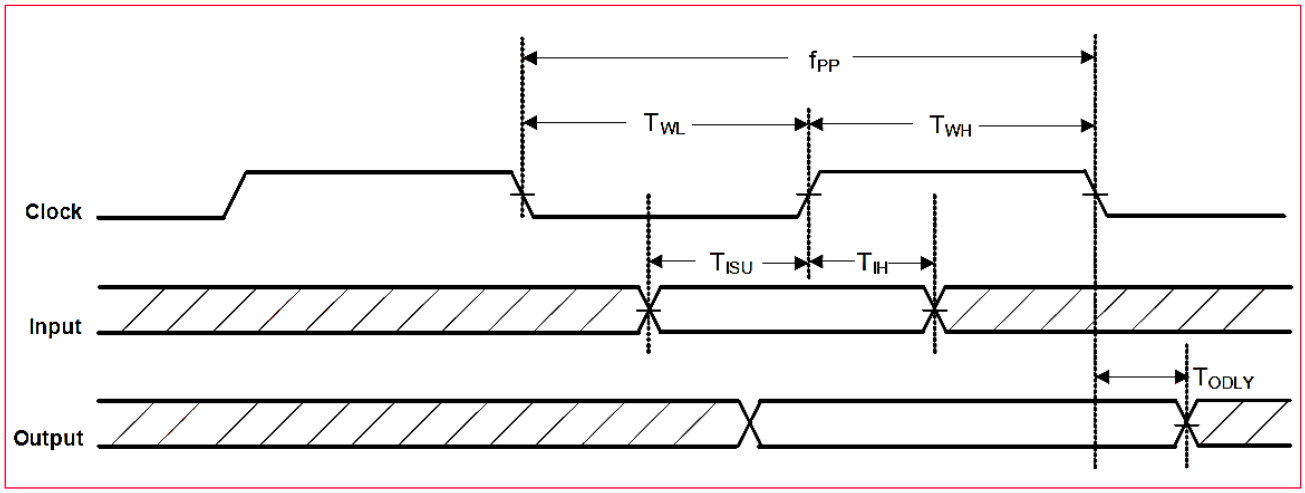


Figure 8 shows the high speed mode signals.

Figure 8: SDIO Protocol Timing Diagram - High Speed Mode (3.3V)

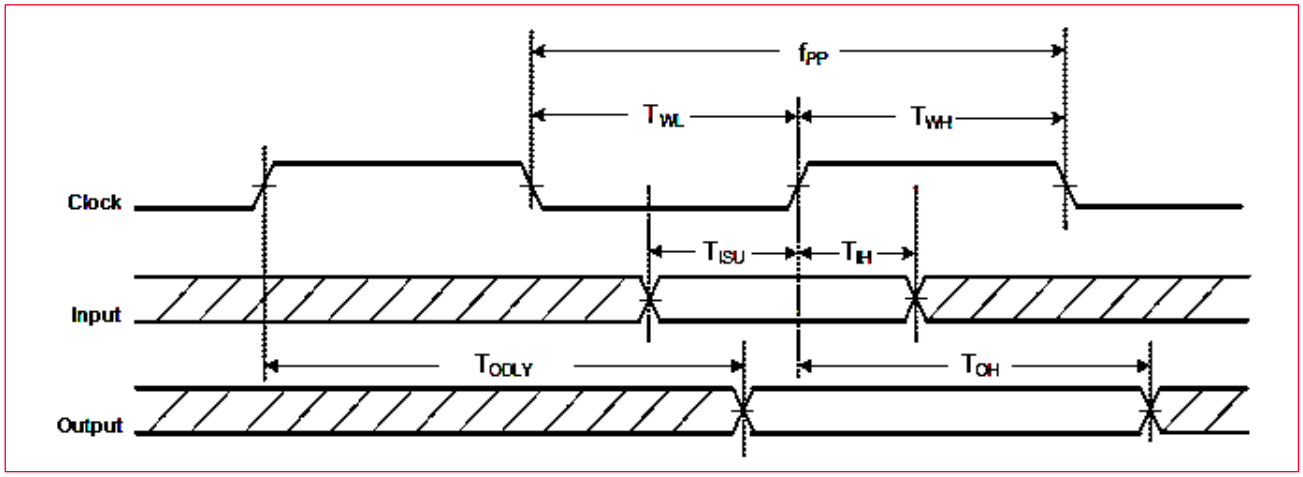


Table 18 lists the SDIO timing data for high speed mode.

Table 18: SDIO Timing Data - Default Speed, High Speed Modes (3.3V)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
f_{PP}	Clock frequency	Normal	0		25	MHz
		High speed	0		50	MHz
T_{WL}	Clock low time	Normal	10			ns
		High speed	7			ns
T_{WH}	Clock high time	Normal	10			ns
		High speed	7			ns
T_{ISU}	Input setup time	Normal	5			ns
		High speed	6			ns
T_{IH}	Input hold time	Normal	5			ns
		High speed	2	-	-	ns
T_{ODLY}	Output delay time	Normal	-	-	14	ns
	$C_L \leq 40$ pF (1 card)	High speed	-	-	14	ns
T_{OH}	Output hold time	High speed	2.5	-	-	ns

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

11.1.2 SDR12, SDR25, SDR50 Modes up to 100 MHz (1.8 V)

Figure 9 shows the SDIO protocol diagram for SDR12, SDR25, SDR50 Modes (up to 100 MHz & 1.8 V).

Figure 9: SDIO Protocol Timing Diagram - SDR12, SDR25, SDR50 Modes

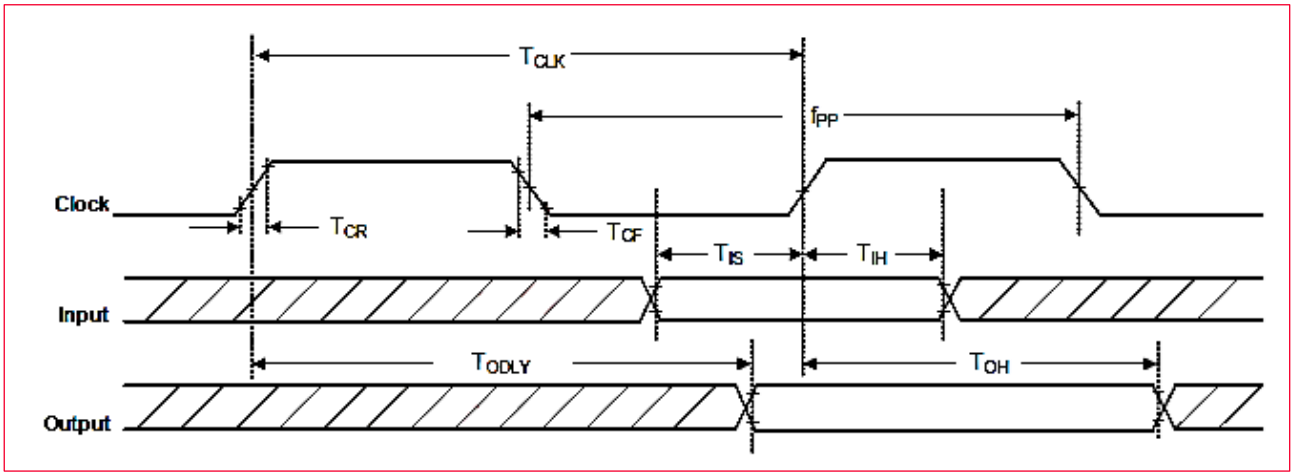


Table 19: SDIO Timing Data - SDR12, SDR25, SDR50 Modes

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	SDR12/25/50	25		100	MHz
T_{IS}	Input setup time	SDR12/25/50	3			ns
T_{IH}	Input hold time	SDR12/25/50	0.8			ns
T_{CLK}	Clock time	SDR12/25/50	10		40	ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF}< 2 ns(maximum) at 100 MHz C_{CARD} = 10 pF	SDR12/25/50			0.2*T_{CLK}	ns
T_{ODLY}	Output delay time C_L ≤ 30 pF	SDR12/25/50			7.5	ns
T_{OH}	Output hold time C_L = 15 pF	SDR12/25/50	1.5			ns

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

11.1.3 SDR104 Mode at 208 MHz (1.8 V)

Figure 10: SDIO Protocol Timing Diagram - SDR104 Mode shows the SDIO protocol timing diagram for SDR104 Mode (208 MHz &1.8V).

Figure 10: SDIO Protocol Timing Diagram - SDR104 Mode

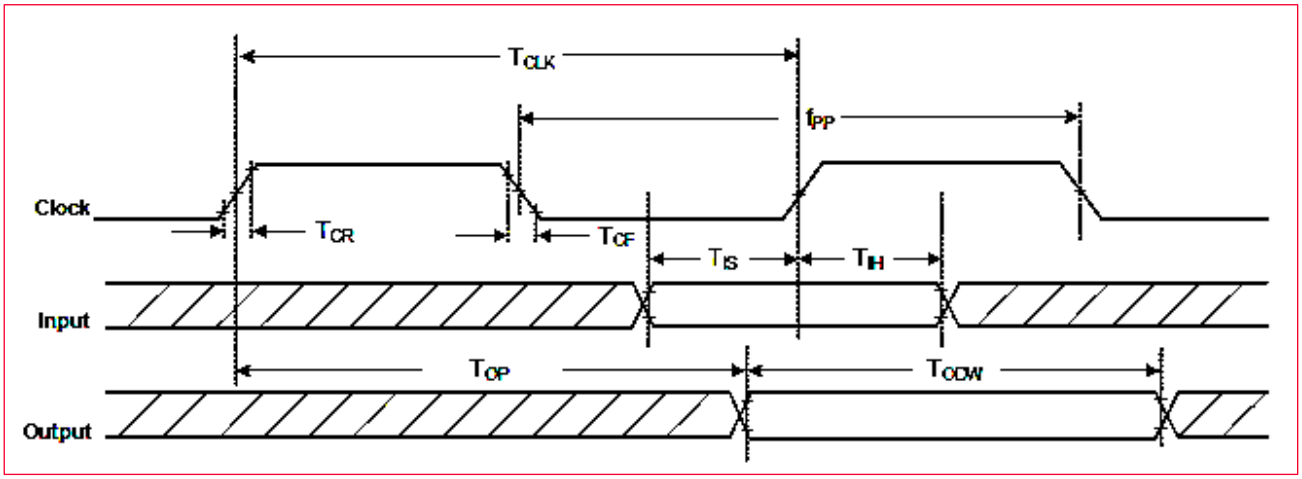


Table 20 shows the SDIO timing data parameters for SDR104 Mode (208 MHz).

Table 20: SDIO Timing Data - SDR104 Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	SDR104	0		208	MHz
T_{IS}	Input setup time	SDR104	1.4			ns
T_{IH}	Input hold time	SDR104	0.8			ns

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{CLK}	Clock time	SDR104	4.8			ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF}< 0.96 ns(maximum) at 208 MHz C_{CARD} = 10 pF	SDR104			0.2*T_{CLK}	ns
T_{OP}	Card output phase	SDR104	0		10	ns
T_{ODW}	Output timing of variable data window	SDR104	2.88			ns

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

11.1.4 DDR50 Mode at 50 MHz (1.8 V)

Figure 11 shows SDIO CMD timing diagram for DDR50 Mode (50 MHz & 1.8V).

Figure 11: SDIO CMD Timing Diagram - DDR50 Mode

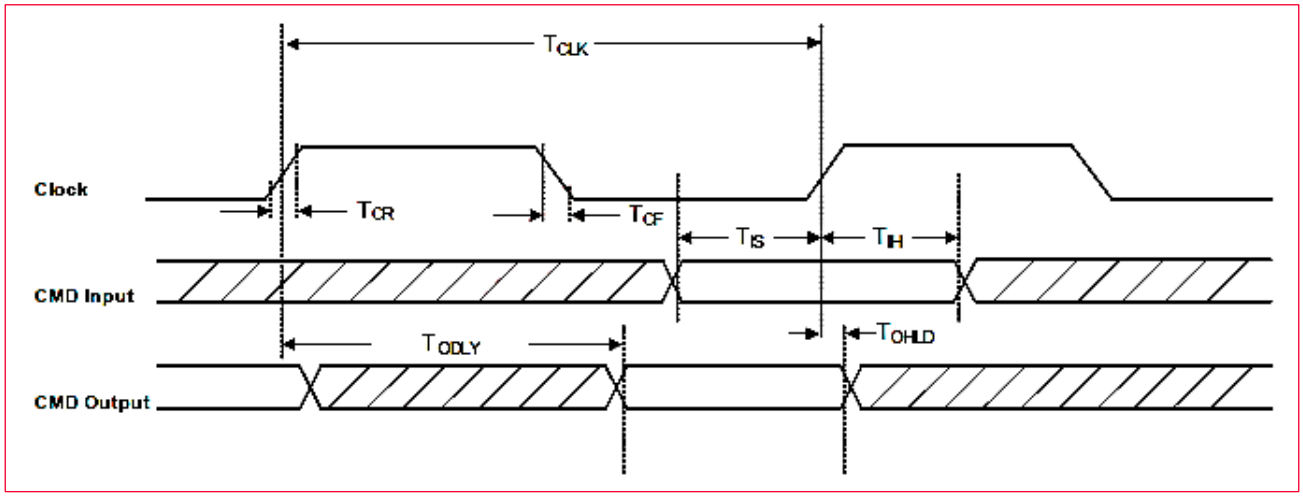


Figure 12 shows SDIO DAT[3:0] timing diagram for DDR50 Mode (50 MHz & 1.8V).

Figure 12: SDIO DAT[3:0] Timing Diagram - DDR50 Mode

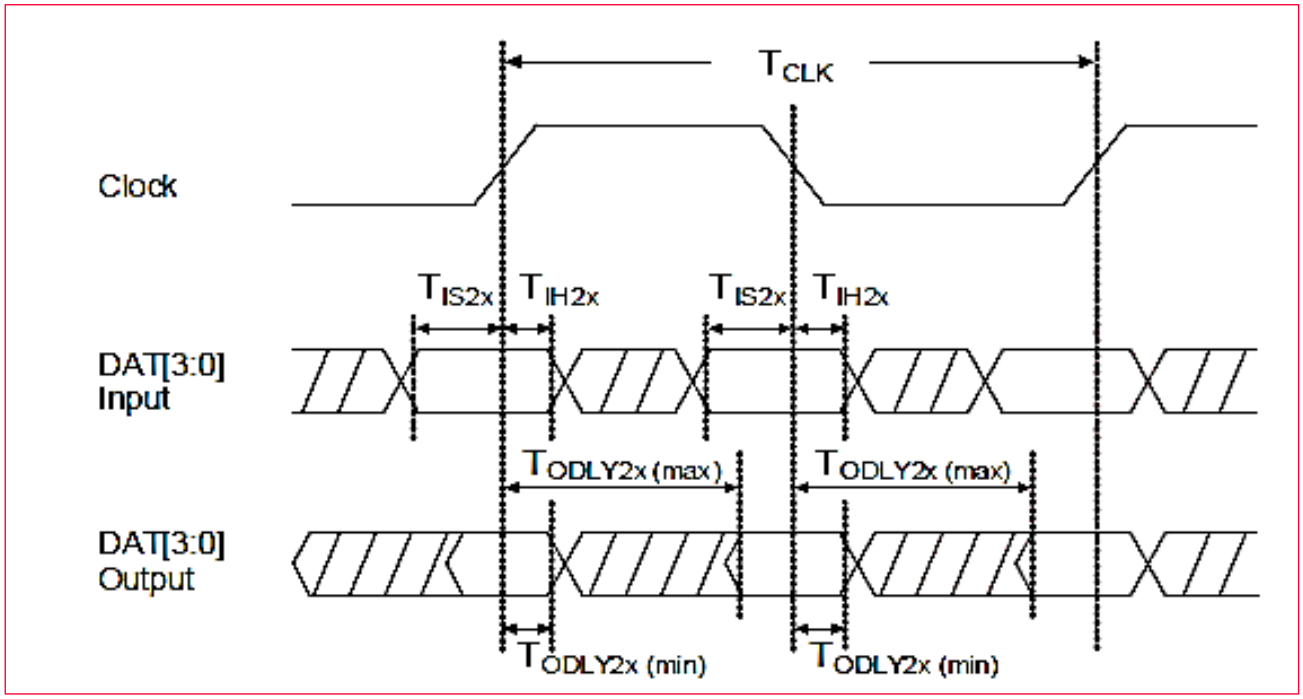


Table 21: SDIO Timing Data - DDR50 Mode (50 MHz)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Clock						
T_{CLK}	Clock time 50 MHz (maximum) between rising edges	DDR50	20			ns
T_{CR}, T_{CF}	Rise time, fall time T_{CR}, T_{CF} < 4.00 ns (maximum) at 50 MHz C_{CARD} = 10 pF	DDR50			0.2*T_{CLK}	ns
Clock Duty		DDR50	45		55	%
CMD Input (referenced to clock rising edge)						
T_{IS}	Input setup time C_{CARD} ≤ 10 pF (1 card)	DDR50	6			ns
T_{IH}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8			ns
CMD Output (referenced to clock rising edge)						
T_{ODLY}	Output delay time during data transfer mode C_L ≤ 30 pF (1 card)	DDR50			13.7	ns
T_{OHLD}	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5			ns
DAT [3:0] Input (referenced to clock rising and falling edges)						
T_{IS2x}	Input setup time	DDR50	3			ns

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
	C_{CARD} ≤ 10 pF (1 card)					
T_{IH2x}	Input hold time C_{CARD} ≤ 10 pF (1 card)	DDR50	0.8			ns
DAT [3:0] Output (referenced to clock rising and falling edges)						
$T_{ODLY2x\ (max)}$	Output delay time during data transfer mode C_L ≤ 25 pF (1 card)	DDR50			7.0	ns
$T_{ODLY2x\ (min)}$	Output hold time C_L ≥ 15 pF (1 card)	DDR50	1.5			ns

Over full range of values specified in the Recommended Operating Conditions unless otherwise specified.

11.2 PCI Express Specifications

The PCI Express host interface pins are powered from the AVDD18 voltage supply.

11.2.1 Differential Tx Output Electricals

This section describes the Tx output electricals.

11.2.1.1 PCI Express Tx Output Specifications Data - 2.5 GT/s

Specifications for Differential Tx Output Electricals is shown in **Table 22.**

This specification is in accordance with PCI Express Base Specification, Revision 2.1 March 4. 2009.

Table 22: PCI Express Tx Output Specifications Data - 2.5 GT/s

Symbol	Parameter	Minimum	Typical	Maximum	Unit
UI	Unit Interval (UI) The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	399.88		400.12	ps
$V_{TX-DIFF-PP}$	Differential peak-to-peak Tx voltage swing $V_{TX-DFFpp}$ = 2*|VT_{XD}+ -VT_{XD}-|	0.8		1.2	V
$V_{TX-DIFF-PP-LOW}$	Low power differential peak-to-peak tTx voltage swing VTX-DFFpp = 2*|VTXD+ - VTXD-	0.4		1.2	V
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0		4.0	dB
T_{TX-EYE}	Tx eye including all jitter sources	0.75		-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time between jitter median and maximum deviation from median.			0.125	UI
$T_{TX-RISE-FALL}$	Tx rise/fall time. Measured differentially from 20% to 80% of swing.	0.125			UI
$RL_{TX-DIFF}$	Tx package plus Si differential return loss	10			dB
RL_{TX-CM}	Tx package plus Si common mode return loss	6			dB
$V_{TX-CM-AC-P}$	Tx AC common mode voltage.		20		mV
$I_{TX-SHORT}$	Tx short circuit current limit			90	mA
$V_{TX-DC-CM}$	Tx DC common mode voltage	0		3.6	V
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle.	0		100	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage.	0		20	mV
$V_{TX-RCV-DETECT}$	Voltage change allowed during receiver detection.			600	mV
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	20			ns

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid diff signaling after leaving electrical idle			8	ns
$T_{CROSSLINK}$	Crosslink random timeout			1.0	ms
C_{TX}	AC coupling capacitor	75		200	nF

11.2.1.2 PCI Express Tx Output Specifications Data - 5 GT/s

PCI Express Tx Output Specifications Data for 5 GT/s is shown in **Table 23**.

This specification is in accordance with PCI Express Base Specification, Revision 2.1 March 4, 2009.

Table 23: PCI Express Tx Output Specifications Data - 5 GT/s

Symbol	Parameter	Minimum	Typical	Maximum	Unit
UI	Unit Interval (UI) The specified UI is equivalent to a tolerance of ±300 ppm for each Refclk source. Period does not account for SSC induced variations.	199.94		200.06	ps
$V_{TX-DIFF-PP}$	Differential peak-to-peak Tx voltage swing $V_{TX-DFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.8		1.2	V
$V_{TX-DIFF-PP-LOW}$	Low power differential peak-to-peak Tx voltage swing $V_{TX-DFFpp} = 2*\|V_{TXD+} - V_{TXD-}\|$	0.4		1.2	V
$V_{TX-DE-RATIO-3.5dB}$	Tx de-emphasis level ratio (3.5 dB)	3.0		4.0	dB
$V_{TX-DE-RATIO-6dB}$	Tx de-emphasis level ratio (6 dB)	5.5		6.5	dB
$T_{MIN-PULSE}$	Instantaneous lone pulse width. Measured relative to rising/falling pulse.	0.9			UI
T_{TX-EYE}	Tx eye including all jitter sources	0.75			UI
$T_{TX-HF-DJ-DD}$	Tx deterministic jitter > 1.5 MHz Deterministic jitter only.			0.15	UI
$T_{TX-LF-RMS}$	Tx RMS jitter < 1.5 MHz Total energy measured over a 10 kHz—1.5 MHz range		3.0		Ps RMS
$T_{TX-RISE-FALL}$	Tx rise/fall time Measured differentially from 20% to 80% of swing	0.15			UI
$R_{LTX-DIFF}$	Tx package plus Si differential return loss (1.25-2.5 GHz)	10			dB
	Tx package plus Si differential return loss (0.05-1.25 GHz)	8			
R_{LTX-CM}	Tx package plus Si common mode return loss	6			dB
$V_{TX-CM-AC-PP}$	Tx AC common mode voltage			100	mVPP
$I_{TX-SHORT}$	Tx short circuit current limit	0		90	mA
$V_{TX-DC-CM}$	Tx DC common mode voltage	0		3.6	V
$V_{TX-CM-DC-ACTIVE-IDLE-DELTA}$	Absolute delta of DC common mode voltage during L0 and electrical idle.	0		100	mV
$V_{TX-IDLE-DIFF-AC-p}$	Electrical idle differential peak output voltage $V_{TX-IDLE-DIFF-DC} = \|V_{TX-Idle-D+} - V_{TX-Idle-D-}\| \leq 20$ mV	0		20	mV
$V_{TX-IDLE-DIFF-DC}$	DC Electrical idle differential peak output voltage	0		5	mV

Symbol	Parameter	Minimum	Typical	Maximum	Unit
	$V_{TX-IDLE-DIFF-DC}$ = $\|V_{TX-Idle-D+} - V_{TX-Idle-D-}\|$ ≤5 mV				
$V_{TX-RCV-DETECT}$	Voltage change allowed during receiver detection.			600	mV
$T_{TX-IDLE-MIN}$	Minimum time spent in electrical idle	20			ns
$T_{TX-IDLE-SET-TO-IDLE}$	Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set.			8	ns
$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to transition to valid differential signaling after leaving electrical idle.			8	ns
$T_{CROSSLINK}$	Crosslink random timeout.			1.0	ms
C_{TX}	AC coupling capacitor	75		200	nF

11.2.2 Differential Rx Input Electricals

This section describes the Rx input electricals.

11.2.2.1 PCI Express Rx Input Specifications Data - 2.5 GT/s

PCI Express Rx Input Specifications Data for 2.5 GT/s is described in **Table 24**.

In accordance with PCI Express Base Specification, Revision 2.1 March 4, 2009.

Table 24: PCI Express Rx Input Specifications Data - 2.5 GT/s

Symbol	Parameter	Minimum	Typical	Maximum	Unit
UI	Unit Interval (UI) UI does not account for SSC induced variations.	399.88		400.12	ps
$V_{RX-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture.	0.175		1.2	V
$V_{RX-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture.	0.175		1.2	V
T_{RX-EYE}	Rx eye time opening Minimum eye time at Rx pins to yield a 10^{-12} BER.	0.40			UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum time delta between median and deviation from median.			0.3	UI
$V_{RX-CM-ACp}$	AC peak common mode input voltage.			150	mV
$RL_{RX-DIFF}$	Differential return loss	15			dB
RL_{RX-CM}	Common mode return loss	0		3.6	dB
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	W
Z_{RX-DC}	DC input impedance	40	50	60	W
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200			kΩ
$V_{RX-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65		175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms

Symbol	Parameter	Minimum	Typical	Maximum	Unit
$L_{RX-SKEW}$	Total skew			20	ns

11.2.2.2 PCI Express Rx Input Specifications Data - 5 GT/s

PCI Express Rx Input Specifications Data for 5 GT/s is described in **Table 25**.

In accordance with PCI Express Base Specification, Revision 2.1 March 4, 2009.

Table 25: PCI Express Rx Input Specifications Data - 5 GT/s

Symbol	Parameter	Minimum	Typical	Maximum	Unit
UI	Unit Interval (UI) UI does not account for SSC induced variations.	199.94		200.06	ps
$V_{RX-DIFF-PP-CC}$	Differential Rx peak-to-peak voltage for common Refclk Rx architecture	0.120		1.2	V
$V_{RX-DIFF-PP-DC}$	Differential Rx peak-to-peak voltage for data clocked Rx architecture	0.100		1.2	V
$T_{RX-TJ-CC}$	Maximum Rx inherent total timing error for common Refclk Rx architecture.			0.40	UI
$T_{RX-TJ-DC}$	Maximum Rx inherent total timing error for data clocked Rx architecture			0.34	UI
$T_{RX-DJ-DD-CC}$	Maximum Rx inherent deterministic timing error for common Refclk Rx architecture			0.30	UI
$T_{RX-DJ-DD-DC}$	Maximum Rx inherent deterministic timing error for data clocked Rx architecture			0.24	UI
$T_{RX-MIN-PLISE}$	Minimum width pulse at Rx Measured to account for worst Tj at 10-12 BER.	0.6			UI
$V_{RX-CM-ACp}$	AC peak common mode input voltage			150	mV
$R_{LRX-DIFF}$	Differential return loss	15			dB
R_{LRX-CM}	Common mode return loss	0		3.6	dB
$Z_{RX-DIFF-DC}$	DC differential input impedance	80	100	120	W
Z_{RX-DC}	DC input impedance	40	50	60	W
$Z_{RX-HIGH-IMP-DC}$	Powered down DC input impedance	200			kΩ
$V_{RX-IDLE-DET-DIFF-p-p}$	Electrical idle detect threshold	65		175	mV
$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	Unexpected electrical idle enter detect threshold integration time			10	ms
$L_{RX-SKEW}$	Total Skew			20	ns

11.3 USB Specifications

The USB 3.0 device interface pins are powered from the AVDD33 voltage supply.

Only if NXP supports USB SW.

11.3.1 USB LS Driver and Receiver Parameters

USB LS Driver and Receiver Parameters are described in **Table 26**.

- These parameters are in accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.
- The load is 100Ω differential for these parameters, unless other specified.

Table 26: USB LS Driver and Receiver Specifications Data

Symbol	Parameter	Minimum	Typical	Maximum	Unit
BR	Baud rate		1.5		Gbps
BRPPM	Baud rate tolerance	-15000.0		15000.0	ppm
Driver Specifications					
V_{OH}	Output signal ended high Defined with 1.425 kΩ pull-up resister to 3.6V.	2.8		3.6	V
V_{OL}	Output signal ended low Defined with 1.425 kΩ pull-down register to ground.	0.0		0.3	V
V_{CRS}	Output signal crossover voltage USB LS/FS Data Rise and Fall Time Diagram.	1.3		2.0	V
T_{LR}	Data fall time • USB LS/FS Data Rise and Fall Time Diagram. • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0		300.0	ns
T_{LF}	Data rise time. • USB LS/FS Data Rise and Fall Time Diagram. • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	75.0		300.0	ns
T_{LRFM}	Rise and fall time matching,	80.0		125.0	%
T_{UDJ1}	Source jitter total: to next transition • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-95.0		95.0	ns
T_{UDJ2}	Source jitter total: for paired transitions • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-150.0		150.0	ns
Receiver Specifications					
V_{IH}	Input signal ended high	2.0			V
V_{IL}	Input signal ended low			0.8	V
V_{DI}	Differential input sensitivity	0.2			V

11.3.2 USB FS Driver and Receiver Parameters

USB FS Driver and Receiver Specifications Data are illustrated in **Table 27**.

- This data is in accordance with Universal Serial Bus 2.0 Specification, Revision 2.0, April 2000.
- The load is 100 Ω differential for these parameters, unless other specified.

Table 27: USB FS Driver and Receiver Specifications Data

Symbol	Parameter	Minimum	Typical	Maximum	Unit
BR	Baud rate		12.0		Mbps
BRPPM	Baud rate tolerance	-2500.0		2500.0	ppm
Driver Specifications					
V_{OH}	Output signal ended high Defined with 1.425 kΩ pull-up resister to 3.6V.	2.8		3.6	V
V_{OL}	Output signal ended low Defined with 1.425 kΩ pull-down register to ground.	0.0		0.3	V
V_{CRS}	Output signal crossover voltage USB LS/FS Data Rise and Fall Time Diagram.	1.3		2.0	V
T_{FR}	Output rise time: • USB LS/FS Data Rise and Fall Time Diagram. • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0		20.0	ns
T_{FL}	Output fall time: • USB LS/FS Data Rise and Fall Time Diagram. • Defined from 10% to 90% for rise time and 90% to 10% for fall time.	-4.0		20.0	ns
T_{DJ1}	Source jitter total to next transition: • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-3.5		3.5	ns
T_{DJ2}	Source jitter total for paired transitions: • Including frequency tolerance. Timing difference between the differential data signals. • Defined at crossover point of differential data signals.	-4.0		4.0	ns
T_{FDEOP}	Source jitter for differential transition to SE0 transition • Defined at crossover point of differential data signals.	-2.0		5.0	ns
Receiver Specifications					
V_{IH}	Input signal ended high	2.0			V
V_{IL}	Input signal ended low			0.8	V
V_{DI}	Differential input sensitivity	0.2			V
T_{JR1}	Receiver jitter to next transition: • Defined at crossover point of differential data signals.	-18.5		18.5	ns

11.4 High Speed UART Specifications

The default baud rate is 115200 bps. Baud rate is configurable by the host stack. High speed UART specifications and parameters are shown in **Table 28** and **Figure 13**.

Figure 13: High Speed UART Specifications

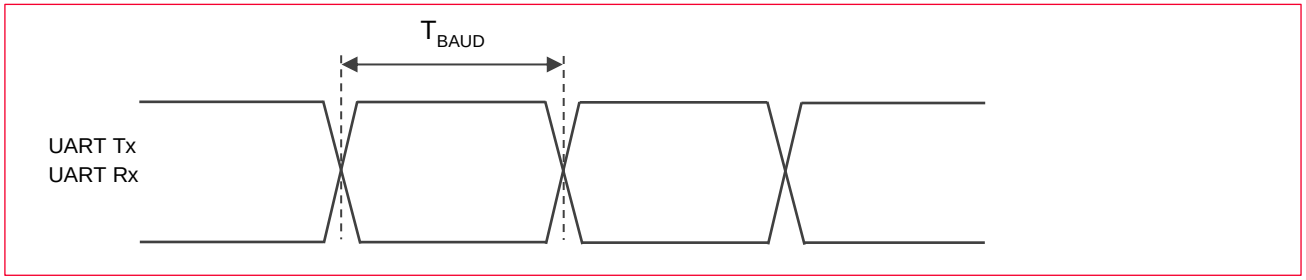


Table 28: High Speed UART Specifications Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_{BAUD}	Baud rate	40 MHz	250			ns

The acceptable deviation from the UART Rx target baud rate is ±3%.

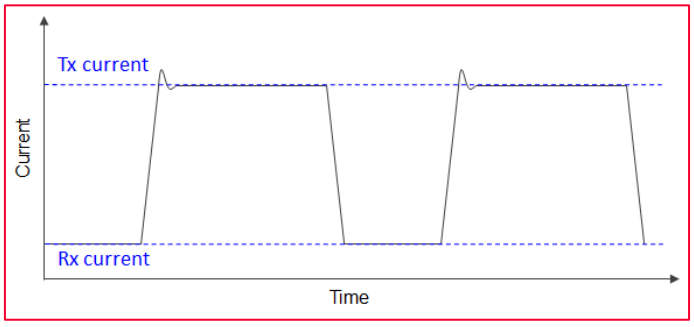
12 DC/RF Characteristics

ALL DC/RF characteristics are defined by following files as shown in **Table 29**. **Figure 14** shows the burst current definition for Type 1YM module.

Table 29: DC/RF Characteristics and Files

Characteristics	Filenames
WLAN Tx Power	txpower_US.bin, txpower_CA.bin, txpower_EU.bin, txpower_JP.bin
WLAN Regulatory Limit	db.txt
Energy Detect	ed_mac.bin
Bluetooth Power	bt_power_config_1.sh (Class 1), bt_power_config_2.sh (Class 2)

Figure 14: Burst Current Definition



12.1 DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Items	Contents
Specification	IEEE 802.11b - 2.4 GHz
Mode	DSSS / CCK
Channel frequency (spacing)	2412 to 2472 MHz (5 MHz)
Data rate	1, 2, 5.5,11 Mbps

12.1.1 High-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 17 dBm at module pad, 11 Mbps mode (1-Antenna)

Table 30: High-Rate Condition for IEEE 802.11b - 2.4 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		420	540	mA
• Rx mode		110	160	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	15	17	19	dBm
Spectrum Mask Margin				
• 1st side lobes			-30	dBr
• 2nd side lobes			-50	dBr
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW =100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-76	dBm
Maximum Input Level (FER ≤ 8%)	-10			dBm
Adjacent Channel Rejection (FER ≤ 8%)	35			dB

12.1.2 Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 17 dBm at module pad, 1 Mbps mode (1-Antenna)

Table 31: Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		420	540	mA
• Rx mode		110	160	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	15	17	19	dBm
Spectrum Mask Margin				
• 1st side lobes			-30	dBr
• 2nd side lobes			-50	dBr
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-80	dBm
Maximum Input Level (FER ≤ 8%)	-4			dBm
Adjacent Channel Rejection (FER ≤ 8%)	35			dB

12.2 DC/RF Characteristics for IEEE 802.11g - 2.4 GHz

Items	Contents
Specification	IEEE 802.11g - 2.4 GHz
Mode	OFDM
Channel frequency (spacing)	2412 to 2472 MHz (5 MHz)
Data rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.2.1 High-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 13 dBm at module pad, 54 Mbps mode (1-Antenna)

Table 32: High-Rate Condition for IEEE 802.11g - 2.4 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		310	380	mA
• Rx mode		110	160	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	11	13	15	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-65	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.2.2 Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 16 dBm at module pad, 6 Mbps mode (1-Antenna)

Table 33: Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		380	470	mA
• Rx mode		110	160	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	14	16	18	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.3 DC/RF Characteristics for IEEE 802.11n - 2.4 GHz

Items	Contents
Specification	IEEE 802.11n - 2.4 GHz
Mode	OFDM
Channel frequency (spacing)	2412 to 2472 MHz (5 MHz)
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps

12.3.1 High-Rate Condition for IEEE 802.11n - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 12 dBm at module pad, MCS7 mode (1-Antenna)

Table 34: High-Rate Condition for IEEE 802.11n - 2.4 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		300	360	mA
• Rx mode		110	160	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	10	12	14	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-45	dBr
Constellation Error (measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER < 10%)			-64	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.3.2 Low-Rate Condition for IEEE 802.11n - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 15 dBm at module pad, MCS0 mode (1-Antenna)

Table 35: Low-Rate Condition for IEEE 802.11n - 2.4 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		360	440	mA
• Rx mode		110	160	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	13	15	17	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-45	dBr
Constellation Error (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.4 DC/RF Characteristics for IEEE 802.11a - 5 GHz

Items	Contents
Specification	IEEE 802.11a - 5 GHz
Mode	OFDM
Channel frequency (spacing)	5180 - 5825 MHz
Data rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.4.1 High-Rate Condition for IEEE 802.11a - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 12 dBm at module pad, 54 Mbps mode (1-Antenna)

Table 36: High-Rate Condition for IEEE 802.11a - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		330	390	mA
• Rx mode		125	180	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	10	12	14	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-65	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

12.4.2 Low-Rate for IEEE 802.11a - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 14 dBm at module pad, 6 Mbps mode (1-Antenna)

Table 37: Low-Rate Condition for IEEE 802.11a - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		360	440	mA
• Rx mode		125	180	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	12	14	16	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

12.5 DC/RF Characteristics for IEEE 802.11n (HT20) - 5 GHz

Items	Contents
Specification	IEEE 802.11n - 5 GHz
Mode	OFDM
Channel frequency (spacing)	5180 to 5825 MHz
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps

12.5.1 High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 11 dBm at module pad, MCS7 mode (1-Antenna)

Table 38: High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		320	370	mA
• Rx mode		125	180	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	9	11	13	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	16			dB

12.5.2 Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 14 dBm at module pad, MCS0 mode (1-Antenna)

Table 39: Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		370	440	mA
• Rx mode		125	180	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	12	14	16	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	16			dB

12.6 DC/RF Characteristics for IEEE 802.11ac (VHT20) - 5 GHz

Items	Contents
Specification	IEEE 802.11ac - 5 GHz
Mode	OFDM
Channel frequency (spacing)	5180 to 5825 MHz
Data rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65, 78 Mbps

12.6.1 High-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 10 dBm at module pad, MCS8 mode (1-Antenna)

Table 40: High-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		300	355	mA
• Rx mode		125	180	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	8	10	12	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-30	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174-230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-59	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-16			dB

12.6.2 Low-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 14 dBm at module pad, MCS0 mode (1-Antenna)

Table 41: Low-Rate Condition for IEEE 802.11ac (VHT20) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		360	435	mA
• Rx mode		125	180	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	12	14	16	dBm
Spectrum Mask Margin				
• at fc +/- 11 MHz			-20	dBr
• at fc +/- 20 MHz			-28	dBr
• at fc ≥ +/-30 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	16			dB

12.7 DC/RF Characteristics for IEEE 802.11n (HT40) - 5 GHz

Items	Contents
Specification	IEEE 802.11n - 5 GHz
Mode	OFDM
Channel frequency (spacing)	5180 to 5825 MHz
Data rate	13.5,27,40.5,54,81,108,121.5,135 Mbps

12.7.1 High-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 11 dBm at module pad, MCS7 mode (1-Antenna)

Table 42: High-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		310	370	mA
• Rx mode		140	200	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	9	11	13	dBm
Spectrum Mask Margin				
• at fc +/- 21 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/-60 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-61	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-2			dB

12.7.2 Low-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 13 dBm at module pad, MCS0 mode (1-Antenna)

Table 43: Low-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		350	415	mA
• Rx mode		140	200	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	11	13	15	dBm
Spectrum Mask Margin				
• at fc +/- 21 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/-60 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-79	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-2			dB

12.8 DC/RF Characteristics for IEEE 802.11ac (VHT40) - 5 GHz

Items	Contents
Specification	IEEE 802.11ac - 5 GHz
Mode	OFDM
Channel frequency (spacing)	5190 to 5795 MHz
Data rate	13.5, 27, 40.5, 54, 81, 108, 121.5, 135, 162, 180 Mbps

12.8.1 High-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 10 dBm at module pad, MCS9 mode (1-Antenna)

Table 44: High-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		300	350	mA
• Rx mode		140	200	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	8	10	12	dBm
Spectrum Mask Margin				
• at fc +/- 21 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/-60 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-32	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-54	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm

12.8.2 Low-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 13 dBm at module pad, MCS0 mode (1-Antenna)

Table 45: Low-Rate Condition for IEEE 802.11ac (VHT40) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		350	410	mA
• Rx mode		140	200	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	11	13	15	dBm
Spectrum Mask Margin				
• at fc +/- 21 MHz			-20	dBr
• at fc +/- 40 MHz			-28	dBr
• at fc ≥ +/-60 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-79	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm

12.9 DC/RF Characteristics for IEEE 802.11ac (VHT80) - 5 GHz

Items	Contents
Specification	IEEE 802.11ac - 5 GHz
Mode	OFDM
Channel frequency (spacing)	5210 to 5775 MHz
Data rate	29.3, 58.5, 87.8, 117, 175.5, 234, 263.3, 292.5, 351, 390 Mbps

12.9.1 High-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 10 dBm at module pad, MCS9 mode (1-Antenna)

Table 46: High-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		310	365	mA
• Rx mode		160	220	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	8	10	12	dBm
Spectrum Mask Margin				
• at fc +/- 41 MHz			-20	dBr
• at fc +/- 80 MHz			-28	dBr
• at fc > +/-120 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-32	dB
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-51	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-9			dB

12.9.2 Low-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V, Output power setting = 12 dBm at module pad, MCS0 mode (1-Antenna)

Table 47: Low-Rate Condition for IEEE 802.11ac (VHT80) - 5 GHz

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode (99% Tx mode)		340	395	mA
• Rx mode		160	220	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power	10	12	14	dBm
Spectrum Mask Margin				
• at fc +/- 41 MHz			-20	dBr
• at fc +/- 80 MHz			-28	dBr
• at fc ≥ +/-120 MHz			-40	dBr
Constellation Error (measured at enhanced mode)			-5	dB
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-76	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-9			dB

12.10 DC/RF Characteristics for Bluetooth

Items	Contents
Bluetooth specification (power class)	Version 5.2 (Class 1)
Channel frequency (spacing)	2402 to 2480 MHz (1 MHz)
Number of RF Channel	79

12.10.1 Basic Data Rate Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V (Test method: Bluetooth Core Spec Vol.3 Part D)

Table 48: Basic Data Rate Condition

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode DH5		70	150	mA
• Rx mode DH5		70	125	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power@DH5	0	3	6	dBm
Frequency range	2400		2483.5	MHz
20 dB bandwidth			1	MHz
Adjacent Channel Power[9]				
• [M-N] = 2			-20	dBm
• [M-N] ≥ 3			-40	dBm
Modulation characteristics				
• Modulation $\Delta f1_{avg}$	140	151	175	kHz
• Modulation $\Delta f2_{max}$	115			kHz
• Modulation $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8	1		
Carrier Frequency Drift				
• 1 slot	-25		25	kHz
• 3 slot / 5 slot	-40		40	kHz
• Maximum drift rate			20	kHz/50 µs
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
BDR Sensitivity (BER ≤ 0.1%)		-96	-70	dBm
Maximum Input Level (BER ≤ 0.1%)	-20			dBm

[9] Up to three spurious responses within Bluetooth limits are allowed.

12.10.2 Enhanced Data Rate Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V (Test method: Bluetooth Core Spec Vol.3 Part D)

Table 49: Enhanced Data Rate Condition

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode 2DH5		70	150	mA
• Rx mode 2DH5		70	125	mA
• Tx mode 3DH5		70	150	mA
• Rx mode 3DH5		70	125	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power@2DH5/3DH5	-3	0	3	dBm
Frequency range	2400		2483.5	MHz
20 dB bandwidth			1	MHz
Adjacent Channel Power[10]				
• [M-N] = 2			-20	dBm
• [M-N] ≥ 3			-40	dBm
EDR Relative Power	-4		1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
• ωi	-75		75	kHz
• ωi+ωo	-75		75	kHz
• ωo	-10		10	kHz
• RMS DEVM (DQPSK)			20	%
• Peak DEVM (DQPSK)			35	%
• 99% DEVM (DQPSK)			30	%
• RMS DEVM (8DPSK)			13	%
• Peak DEVM (8DPSK)			25	%
• 99% DEVM (8DPSK)			20	%
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
EDR Sensitivity (BER ≤ 0.007%) @8DPSK		-88	-70	dBm
Maximum Input Level (BER ≤ 0.1%)	-20			dBm

[10] Up to three spurious responses within Bluetooth limits are allowed.

12.11 DC/RF Characteristics for Bluetooth Low Energy

Items	Contents
Bluetooth specification (power class)	Version 5.2 (Class 1.5)
Channel frequency (spacing)	2402 to 2480 MHz (2 MHz)
Number of RF Channel	40

12.11.1 1 Mbps PHY Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V (Test method: Bluetooth Core Spec Vol. 6 Part F)

Table 50: 1 Mbps PHY Condition

Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		70	150	mA
• Rx mode		70	125	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output power	0	3	6	dBm
In-band emission				
• f_{TX}+/-2 MHz			-20	dBm
• f_{TX}+/-[3+n] MHz; n = 0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	225		275	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier frequency offset and drift				
• Frequency offset (f_n); n = 0,1,2,3…k	-150		150	kHz
• Frequency drift ($\|f_0-f_n\|$); n = 2,3,4…k			50	kHz
• Drift rate				
• $\|f_1-f_0\|$			23	kHz
• $\|f_n-f_{n-5}\|$; n = 6,7, 8,…k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm

Items	Contents			
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-97	-70	dBm
Maximum input signal level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

12.11.2 2 Mbps PHY Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 3.3V (Test method: Bluetooth Core Spec Vol. 6 Part F)

Table 51: 2 Mbps PHY Condition

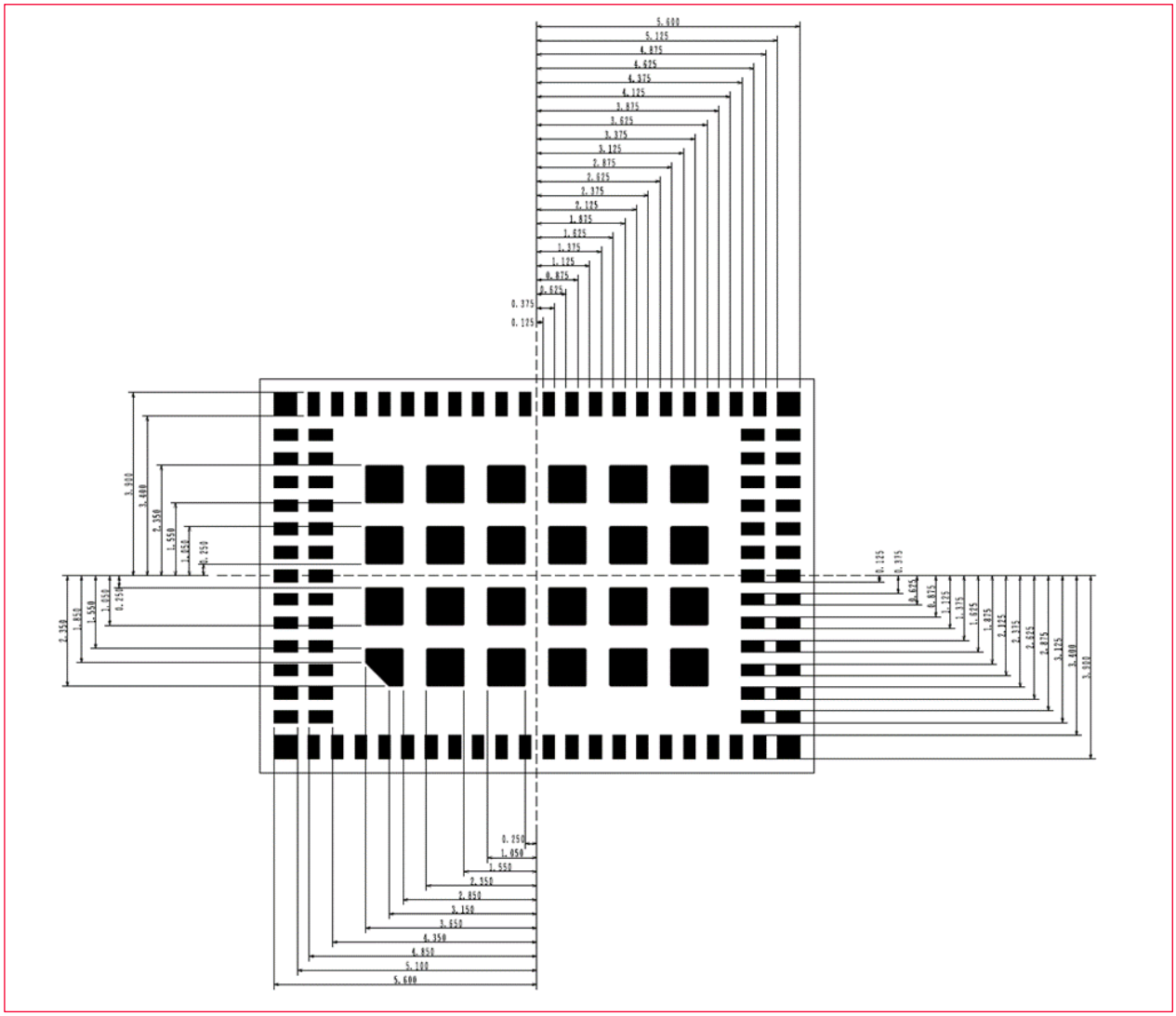
Items	Contents			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		70	150	mA
• Rx mode		70	125	mA
Tx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output power	0	3	6	dBm
In-band emission				
• f_{TX}+/-4 MHz			-20	dBm
• f_{TX}+/-5 MHz			-20	dBm
• f_{TX}+/-[6+n] MHz; n = 0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	450		550	kHz
• $\Delta f2_{max}$ (at 99.9%)	370			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			-
Carrier frequency offset and drift				
• Frequency offset (f_n); n = 0,1,2,3…k	-150		150	kHz
• Frequency drift ($\|f_0-f_n\|$); n = 2,3,4…k			50	kHz
• Drift rate				
• $\|f_1-f_0\|$			23	kHz
• $\|f_n-f_{n-5}\|$; n = 6,7, 8,…k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm

Items	Contents			
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver sensitivity (PER < 30.8%)		-95	-70	dBm
Maximum input signal level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

13 Land Pattern

The land pattern (top view, Unit: mm) is shown in **Figure 15**.

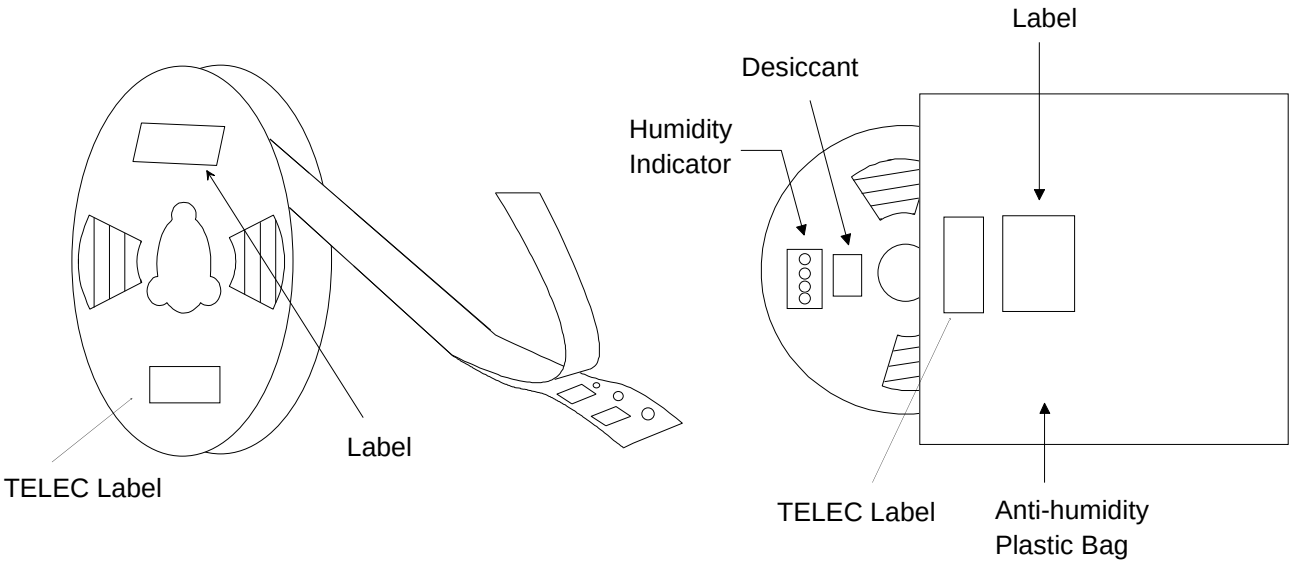
Figure 15: Land Pattern



13.1 Package Label

Figure 16 shows the package label information (Humidity Proof Packing).

Figure 16: Package Label (Humidity proof Packing)



The package label may be attached on one side only.

Package label display example is shown in **Figure 17**.

Figure 17: Package Label Display Example

13.2 Country of Origin

China

SHENZHEN MURATA TECHNOLOGY CO., LTD.

Some countries have applied for two countries, China and Japan, in preparation for future factory changes, but the production site in the delivery specifications is the above-mentioned factory in China.

14 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

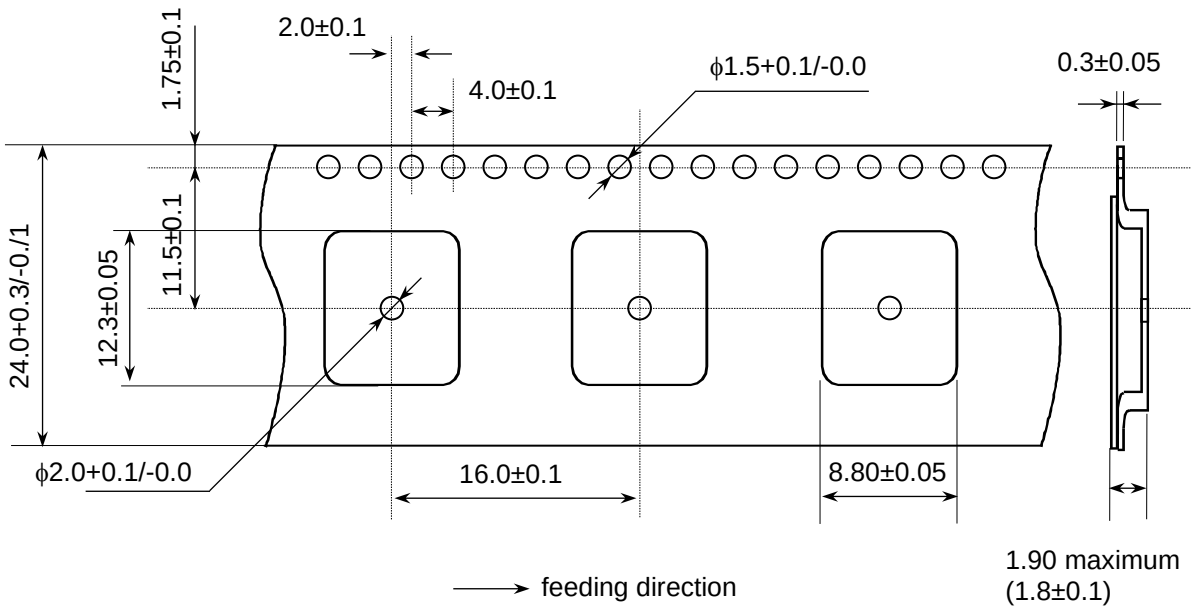
14.1 Dimensions of Tape (Plastic Tape)

The dimension of the tape is as follows:

- The corner and ridge radiuses (R) of the inside cavity are 0.3 mm maximum.
- Cumulative tolerance of 10 pitches of the sprocket hole is +/-0.15 mm.
- Measuring cavity positioning is based on cavity center in accordance with JIS/IES standard.

Figure 18 is a graphical representation of the tape dimension (plastic tape).

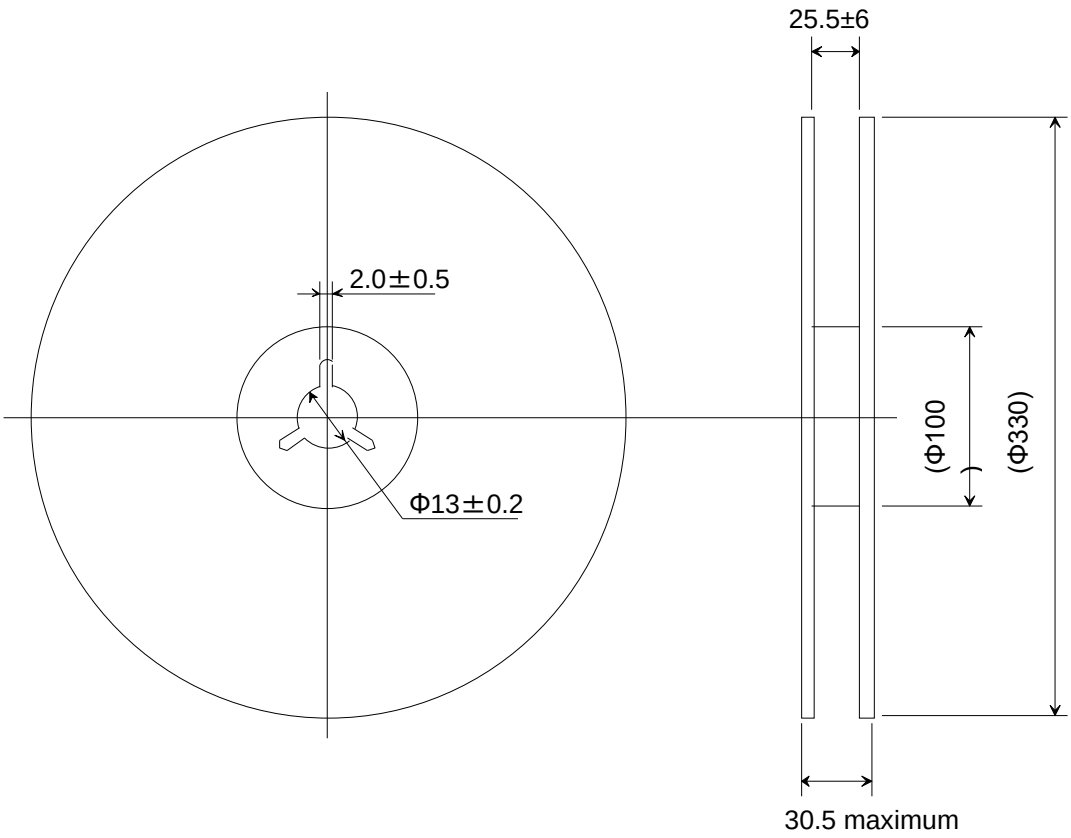
Figure 18: Dimensions of Tape (Plastic tape)



14.2 Dimensions of Reel

Figure 19 shows the reel dimensions.

Figure 19: Dimensions of Reel (Unit: mm)



14.3 Taping Diagrams

Figure 20 shows the tapings diagrams.

Figure 20: Taping Diagrams

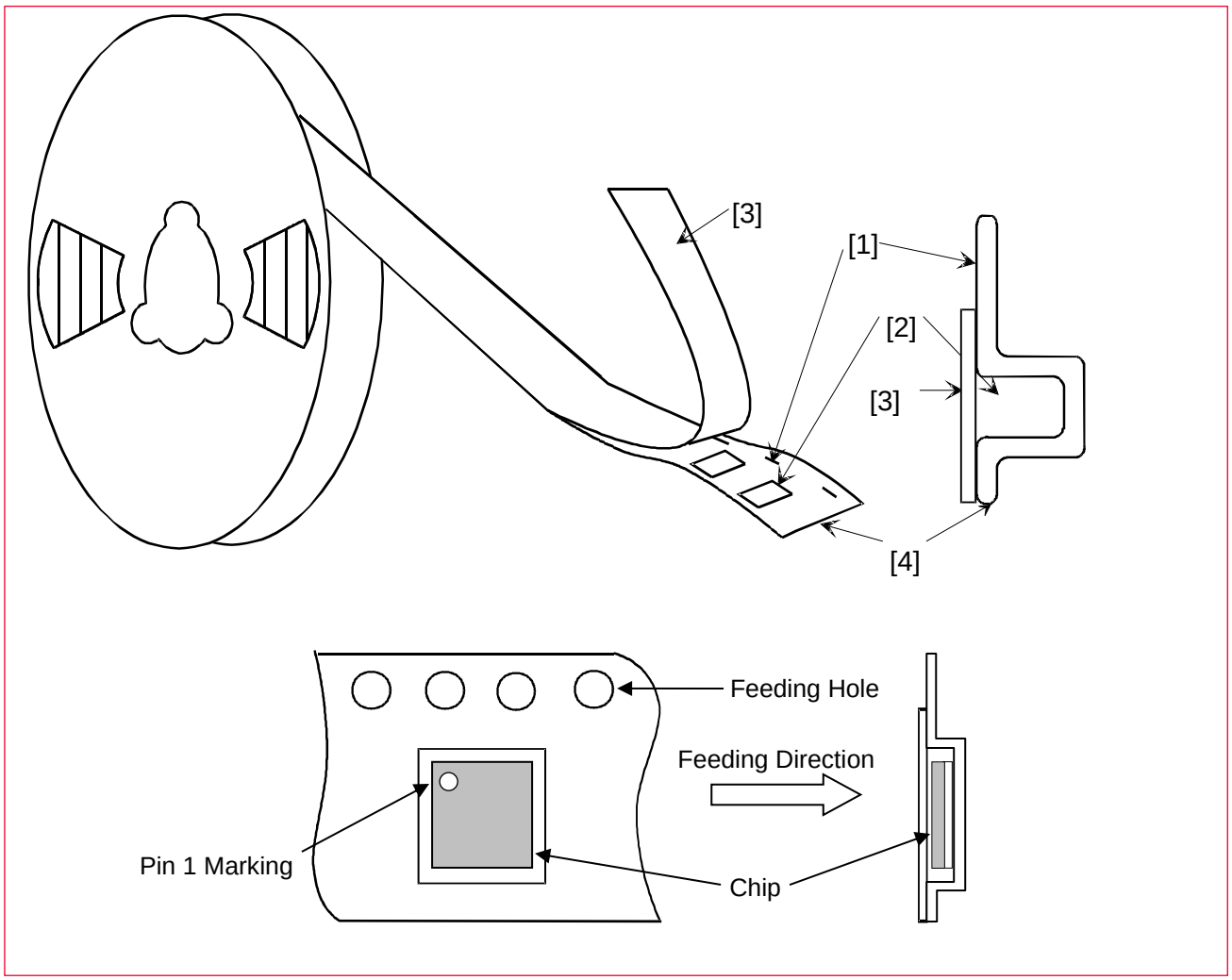


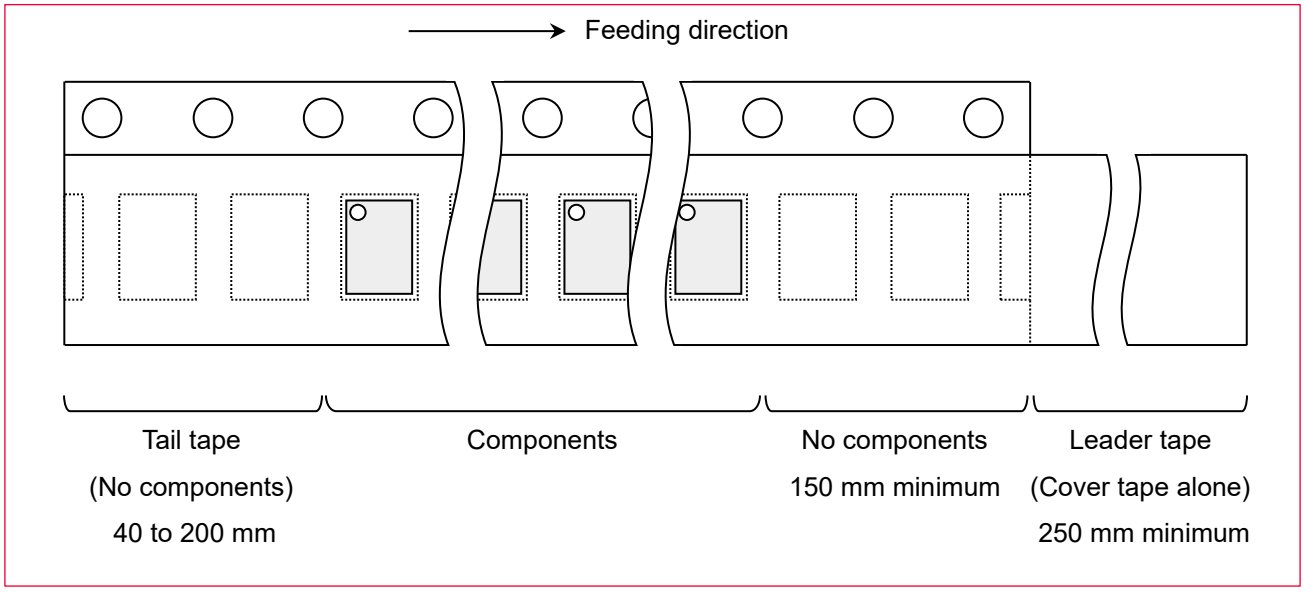
Table 52: Taping Specifications

Mark	Description
1	Feeding hole. As specified in Dimensions of Tape (Plastic tape).
2	Hole for Chip. As specified in Dimensions of Tape (Plastic tape).
3	Cover tape. 62 µm in thickness.
4	Base tape. As specified in Dimensions of Tape (Plastic tape).

14.4 Leader and Tail Tape

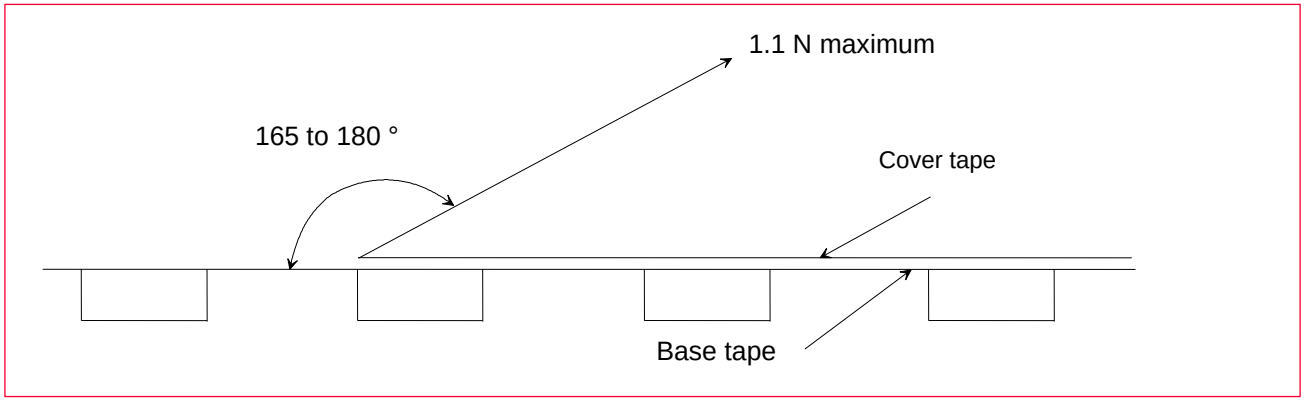
The leader and tail tape are shown in **Figure 21**.

Figure 21: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape: 5 N minimum.
- Packaging unit: 1000 pcs. / Reel
- Tape material:
  - Base tape: Plastic
  - Reel: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling off force: 1.1 N maximum in the direction of peeling as shown in **Figure 22**.

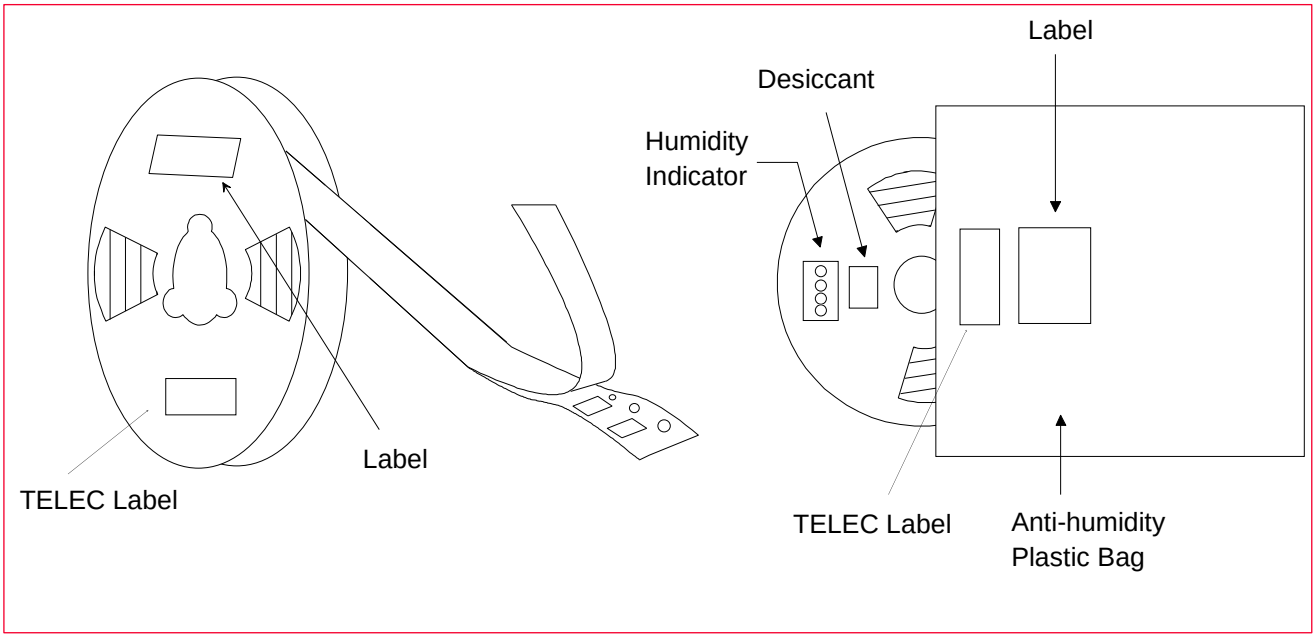
Figure 22: Peeling Force



14.5 Packaging (Humidity Proof Packing)

Figure 23 shows the humidity proof packaging.

Figure 23: Humidity Proof Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

15 Notice

15.1 Storage Conditions

- Please use this product within 6 months after receipt.
  - The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (Packing materials may be deformed at the temperature over 40 °C).
  - The product left more than 6 months after reception; it needs to be confirmed the solderability before used.
  - The product *must* be stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
  - Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, *must* not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
  - After the packing opened, the product *must* be stored at ≤30 °C / <60 %RH and the product *should* be used within 168 hours after opening.
  - When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products must be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

15.2 Handling Conditions

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals. If there is any such damage, the characteristics of products may change. *Do not touch* products with bare hands that may result in poor solder ability and destroy by static electrical charge.

15.3 Standard PCB Design (Land Pattern and Dimensions)

- All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.
- The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

15.4 Notice for Chip Placer

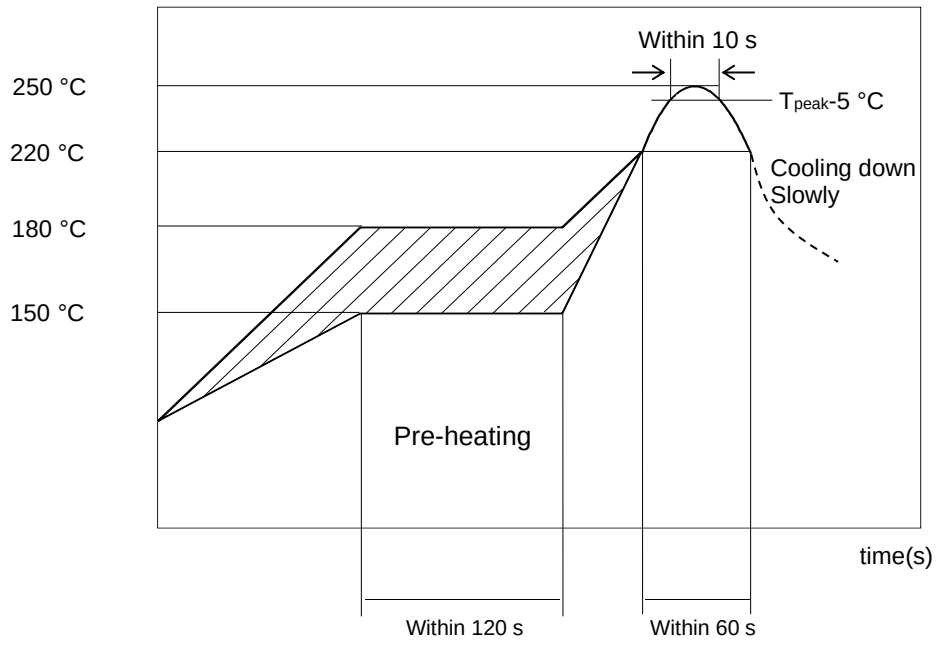
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

15.5 Soldering Conditions

The recommendation conditions of soldering are as in the following figure.

Soldering must be carried out by the above-mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Figure 24: Reflow soldering standard conditions (Example)



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less.

15.6 Cleaning

Since this Product is Moisture Sensitive, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

15.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl_2, NH_3, SO_X, NO_X etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.

Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

15.8 Input Power Capacity

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case the components are used beyond such input power capacity range.

16 Preconditions to Use Our Products

PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

Please note that the only warranty that we provide regarding the products is its conformance to the specifications provided herein. Accordingly, we shall not be responsible for any defects in products or equipment incorporating such products, which are caused under the conditions other than those specified in this specification.

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- Aircraft equipment.
- Aerospace equipment.
- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.

- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.
- We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

Even in the unlikely event that an abnormality or malfunction occurs in this product under operating conditions that conform to the specifications, be sure to add an appropriate fail-safe function to the system to prevent secondary accidents.

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Moreover, you must comply with "foreign exchange and foreign trade law", the "U.S. export administration regulations", etc.

Please note that we may discontinue the manufacture of our products, due to reasons such as end of supply of materials and/or components from our suppliers.

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If you can’t agree with the above contents, please contact sales.

Revision History

Revision Code	Date	Changed Item	Comment
1	2020.01.15	First version	
2 (A)	2020.02.17	8. DIMENSIONS, MARKING AND TERMINAL CONFIGURATIONS 10. REFERENCE PERIPHERAL CIRCUIT	• Added label design information. • Added Reference Circuit
3 (B)	2020.06.15	TOP page 7. Module Pin Descriptions 11. Pin States	• Changed part number to LBEE5XV1YM • Changed pin name RXP/RXN/TXP/TXN to -PCIE_RXP/PCIE_RXN/PCIE_TXP/PCIE_TXN. • Added pin state table
4 (C)	2020.06.20	4. Dimensions	• Added Solder bump and defined T1 dimension
5 (D)	2020.08.07	9.10 DC/RF Characteristics for Bluetooth 9.11 DC/RF Characteristics for Bluetooth (LE)	• Defined output power • Defined output power
6 (E)	2020.11.06	Updated to new format 1. Scope 2. Key Features 5. Certification Information 6. Dimensions, Marking and Terminal configurations 9. Operating Conditions 12. DC/RF Characteristics 15.Tape and Reel Packing APPENDIX	• Changed Bluetooth version 5.1 to 5.2 • Changed Bluetooth version 5.1 to 5.2 • Added certification information • Updated marking to final • Added peak current. • Fixed TBD specifications • Added packing information. • Added User manual and Antenna Installation Guide
7 (F)	2020.12.01	11.4 High speed UART specifications	• Added.
8 (G)	2021.01.07	7.1 Pin Descriptions 7.2. Pin Descriptions APPENDIX	• Corrected Typo (Pin64) • Added description for PCM and UART related pins. • Added configuration manual Base IC datasheet revision: D
9 (H)	2020.01.26	TOP page, 3. Ordering Information 9.1 Operating Conditions	• Changed tentative P/N • Updated VIO_SD
10 (I)	2021.3.04	11.4 High speed UART specifications 2. Features 7.3. Configuration pins - Added default baud rate information.	• Added default baud rate information • Added comment on USB IF • Added comment on USB IF
11 (J)	2021.4.01	2. Key feature & 5.2 Bluetooth Qualification 7.2 Pin Descriptions 9.1. Operating Conditions 14. Reference circuit	• Added a comment on supported Bluetooth functions • Updated the description of PMIC_EN • Added VIO_SD 1.8V mode • Added values of matching components
12 (K)	2021.04.26	7.2 Pin descriptions 7.3 Configuration pins 7.4 Pin States - Added comment to AVDD18 pin	• Added comment to AVDD18 pin • Added comment on pull-up • Changed DVDD18 to AVDD18 Added Internal pull values

Revision Code	Date	Changed Item	Comment
13 (L)	2021.12.14	7.4 Pin States 9.1 Operating Conditions 9.2 External Sleep Clock Requirements 10. Power Sequence 14. Reference Peripheral Circuit - Added SLP_CLK_IN	• Added SLP_CLK_IN • Defined IO current and Peak current • Added a comment • Defined timing parameters • Corrected locations of DC blocker for PCIE signal.
14 (M)	2022.04.08	9.1 Operating Conditions 9.4. Package Thermal Conditions 12.10. DC/RF Characteristics for Bluetooth 12.11. DC/RF Characteristics for Bluetooth	• Defined Ta and Tj. • Added. • Added test method • Added test method
15 (N)	2022.06.09	Appendix	• Translated Japanese to English
16 (O)	2022.07.15	Appendix	• Power table on Japanese regulatory
17 (P)	2022.09.27	2. Key Features	• Add Total Fit Value
18 (Q)	2022.10.25	Appendix	• Add EU certification Information
19 (R)	2022.10.31	2. Key Features 3. Ordering Information 7.4 Pin States 10. Power-Up / Power-Down Sequence 14. Reference Circuit Appendix	• Updated information • Added Embedded Artists' M.2 module information. • Added comments on termination of open pins. • Renamed section • Moved section to HW app note. • Moved Appendix information into Sections 14 and 15. • Moved antenna sections to HW app note. • Added power table for Europe region. Updated to new format
20 (S)	2023.03.24	4. Block Diagram 9.3 PMIC_EN I/O Requirement	• Modify layout • Add section 9.3: PMIC_EN I/O Requirement, and Table14: PMIC_EN I/O Requirement
21	2025.02.14	Revision History 2. Key features 6. Dimensions, Markings… 12. DC/RF Characteristics… (14. General for Radio…) (15. Radio Regulatory Cert…) 16. Preconditions to Use…	• Changed Revision rule • Added total FIT value • Added a structure figure and warning message • Corrected typo of spectrum mask • Removed stable modulation spec • Removed the section • Removed the section • Updated