

Type 1XK Wi-Fi™ + Bluetooth® Module

NXP IW416 Chipset for 802.11a/b/g/n + Bluetooth 5.2
Datasheet - Rev. 21

- Design Name: Type 1XK
- P/N: LBEE5CJ1XK-687

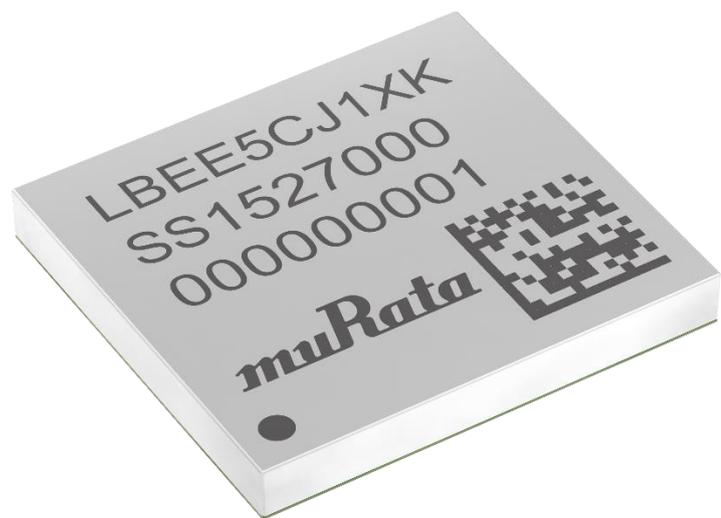


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About This Document

Murata's Type 1XK is a small and high-performance module based on NXP's IW416 combo chipset, supporting IEEE 802.11a/b/g/n + Bluetooth 5.2 BR/EDR/LE. This datasheet describes Type 1XK module in detail.



Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product. In particular, RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. Example: Insert → Tables → Quick Tables → Save Selection to Gallery 
	External Hyperlink This symbol indicates a hyperlink to an external document or website. Example: Murata Manufacturing Co., Ltd.  Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. Example: Scope  Click on the text to open the link.
<code>Console input/output or code snippet</code>	Console I/O or Code Snippet This text Style denotes console input/output or a code snippet.
<code># Console I/O comment // Code snippet comment</code>	Console I/O or Code Snippet Comment This text Style denotes a console input/output or code snippet comment. <ul style="list-style-type: none"> • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This specification characterizes the IEEE 802.11a/b/g/n + Bluetooth 5.2 BR/EDR/LE combo module.

2 Key Features

- ◆ NXP IW416 inside
- ◆ Supports IEEE 802.11a/b/g/n specification: Dual band 2.4 GHz and 5 GHz
- ◆ SISO with 20 MHz and 40 MHz channels
- ◆ Up to MCS7 data rates (150 Mbps)
- ◆ Supports Bluetooth specification version 5.2
- ◆ For supported Bluetooth functions, refer to [Bluetooth SIG site](#) 
- ◆ WLAN interface: SDIO 3.0
- ◆ Bluetooth interface: HCI UART, PCM, and I2S
- ◆ Temperature Range: - 40 °C to 85 °C
- ◆ Dimensions: 9.1 x 8.3 x 1.3 mm
- ◆ Weight: 268.8 mg
- ◆ MSL: 3
- ◆ Surface-mount type
- ◆ RoHS compliant
- ◆ Total Fit: 71

3 Ordering Information

Table 2 provides the ordering information for Type 1XK module.

Table 2: Ordering Information

Ordering Part Number	Description
LBEE5CJ1XK-687	Module order
LBEE5CJ1XK-SMP	Sample module order (If module samples are not available through distribution, contact Murata referencing this part number)
EAR00385	Embedded Artists Type 1XK M.2 EVB (default EVB available through distribution)
LBEE5CJ1XK-EVB	Murata Type 1XK M.2 EVB (contact Murata as this is special order item)

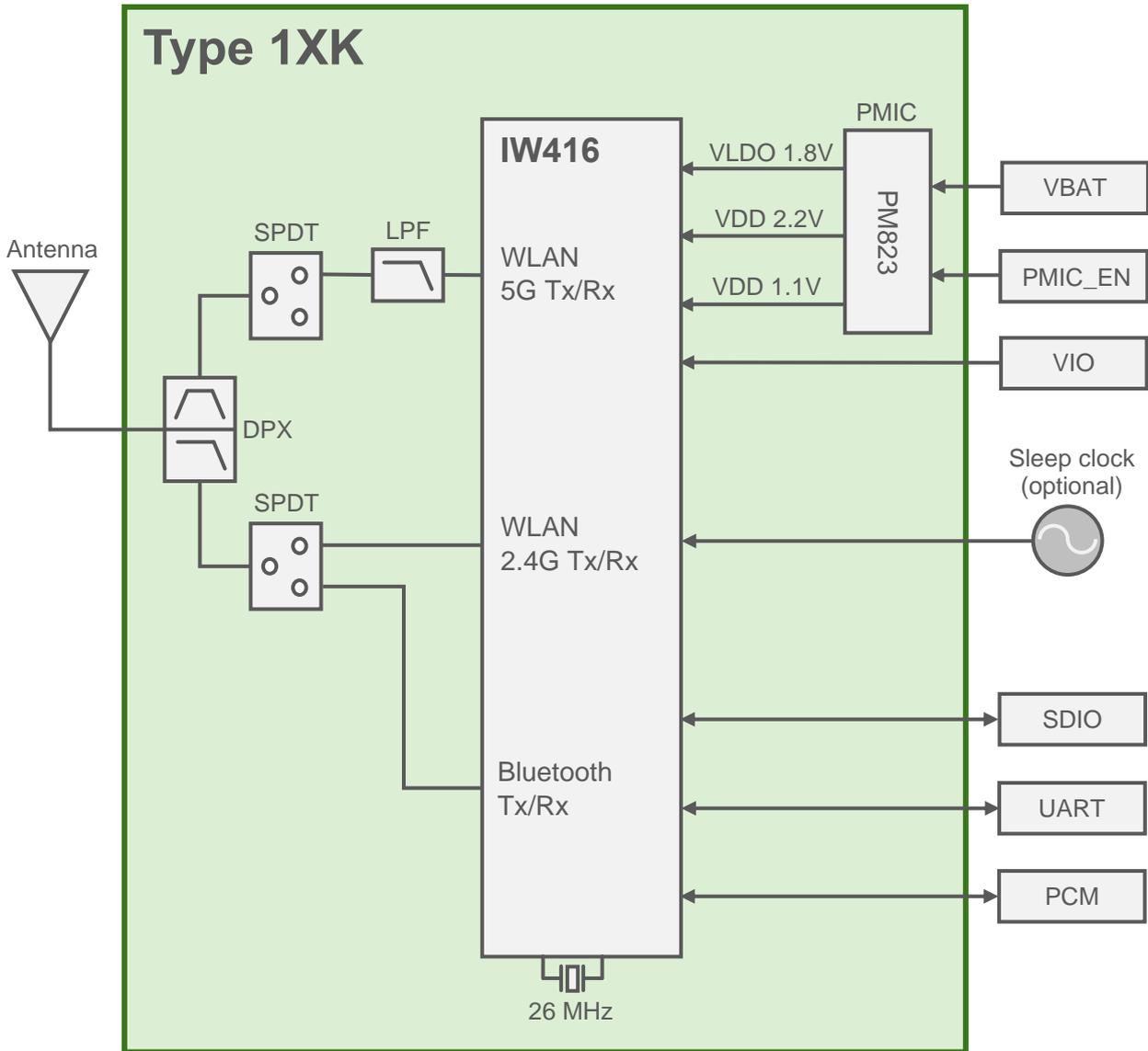


LBEE5CJ1XK is used in regulatory certification test report.

4 Block Diagram

Figure 1 shows the block diagram of Type 1XK module.

Figure 1: Block Diagram



5 Certification Information

This section has information about radio and Bluetooth certification.

5.1 Radio Certification

Transmit output power setting is defined by “txpower_XX.bin” (XX is country code). The transmit power files are hosted at Murata GitHub for [Linux](#) and [FreeRTOS](#). **Table 3** shows the transmit power file required for each region.

Table 3: Transmit Power Limit Files

Country	ID	Country Code	Tx Power Limit File	
			Linux	FreeRTOS
USA (FCC)	VPYLB1XK	US	txpower_US.bin	wlan_txpwrlimit_cfg_murata_1XK_US.h
Canada (IC)	772C-LB1XK	CA	txpower_CA.bin	wlan_txpwrlimit_cfg_murata_1XK_CA.h
Europe	EN300328/301893, EN300440 conducted test report is prepared.	DE	txpower_EU.bin	wlan_txpwrlimit_cfg_murata_1XK_EU.h
Japan	Japanese type certification is prepared.  001-P01624	JP	txpower_JP.bin	wlan_txpwrlimit_cfg_murata_1XK_JP.h



Each country code is defined by Murata's db.txt file. Please ask your contact person from Murata.

5.2 Bluetooth Qualification

- QDID: 169159
- Set Bluetooth Tx Power to Class 1 by using [bt_power_config_1.sh](#).
- For supported Bluetooth functions, refer to [Bluetooth SIG site](#).

6 Dimensions, Markings and Terminal Configurations

This section has information on dimensions, markings, and terminal configurations for Type 1XK.

Figure 2: Dimensions, Markings and Terminal Configurations

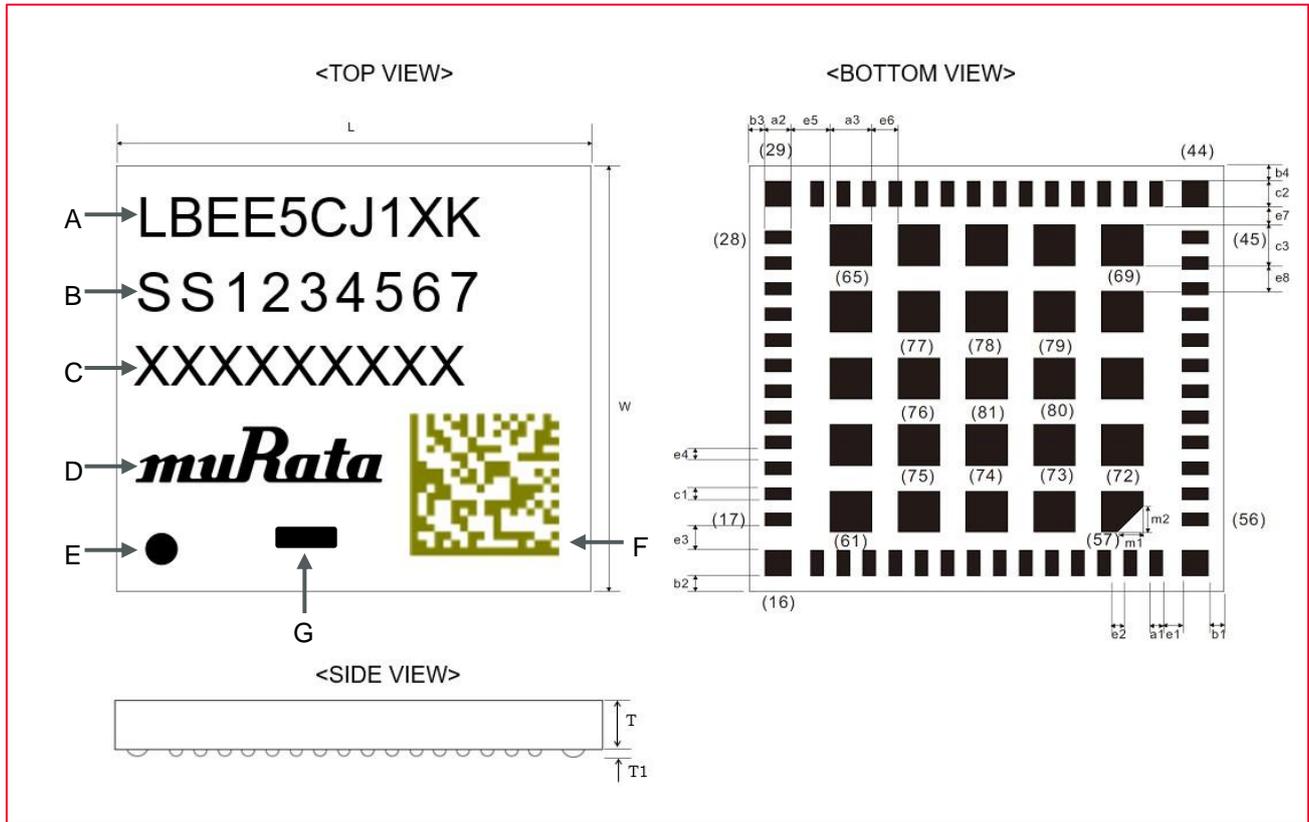


Table 4: Markings

Marking	Meaning
A	Module Type
B	Inspection Number
C	Serial Number
D	Murata Logo
E	Pin 1 Marking
F	2D code
G	Identification mark

Table 5: Dimensions

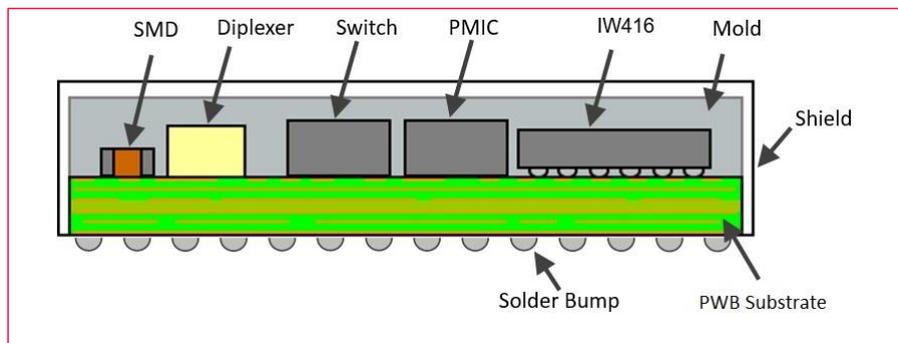
Marks	Dimensions	Marks	Dimensions	Marks	Dimensions	Marks	Dimensions
L	9.1 ± 0.2	W	8.3 ± 0.2	T	1.3 maximum	a1	0.25 ± 0.1
a2	0.5 ± 0.1	a3	0.8 ± 0.2	b1	0.3 ± 0.2	b2	0.3 ± 0.2
b3	0.3 ± 0.2	b4	0.3 ± 0.2	c1	0.25 ± 0.1	c2	0.5 ± 0.1
c3	0.8 ± 0.1	e1	0.375 ± 0.1	e2	0.25 ± 0.1	e3	0.475 ± 0.1
e4	0.25 ± 0.1	e5	0.75 ± 0.1	e6	0.5 ± 0.1	e7	0.35 ± 0.1
e8	0.5 ± 0.1	m1	0.5 ± 0.2	m2	0.5 ± 0.2	T1	0.045 typical



T dimension does not include height of solder bumps.
Unit of Dimensions are in mm.

Figure 3 shows the structure of Type 1XK.

Figure 3: Structure



The sides of the module are GND shielded. In order to avoid contact between the GND shield and the electrodes on the mother board, please carefully evaluate the standoff before use the module.

7 Module Pin Descriptions

This section has the pin descriptions of Type 1XK and pin assignments layout descriptions.

7.1 Pin Assignments

The pin assignment (Top View) layout is shown in **Figure 4**.

Figure 4: Pin Assignments Top View

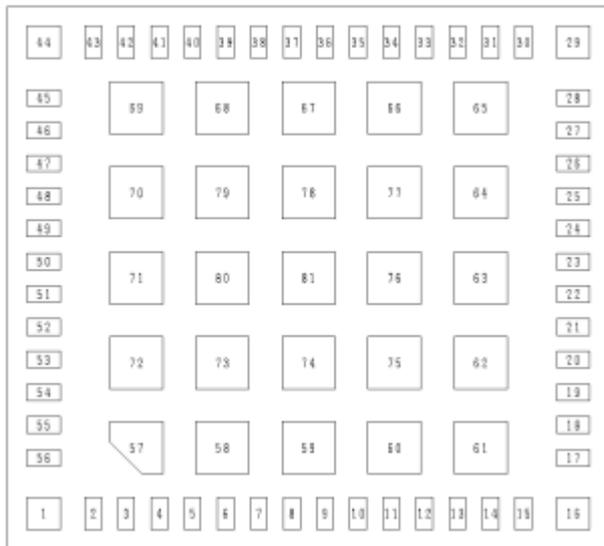


Table 6 illustrates the terminal configurations.

Table 6: Terminal Configurations

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	20	GPIO(3) TDO	39	GND
2	VIO	21	GND	40	GND
3	SD_D2	22	VBAT	41	GND
4	SD_CLK	23	VBAT	42	RF_CNTL2_N
5	SD_D0	24	GND	43	RF_CNTL3_P
6	SD_CMD	25	GND	44	GND
7	GPIO(9) UART_RXD	26	GND	45	BT_ANT SHARED
8	GPIO(6)	27	GND	46	GND
9	GPIO(7)	28	GND	47	BT_ANT DEDICATED
10	NC	29	GND	48	GND
11	GPIO(4)	30	GND	49	GND
12	GPIO(1)	31	PMIC_EN	50	GND
13	GPIO(15) TMS	32	WCI_SOUT	51	GPIO(11) UART_RTS
14	GPIO(5)	33	WCI_SIN	52	GPIO(0)
15	GPIO(8) UART_CTS	34	GPIO(12)	53	GPIO(13)

16	GND	35	RF_CNTL1_P	54	GPIO(10) UART_TXD
17	GPIO(14) TCK	36	RF_CNTL0_N	55	SD_D3
18	GPIO(2) TDI	37	GND	56	SD_D1
19	SLP_CLK_IN	38	RF_ANT	57-81	GND

7.2 Pin Descriptions

Table 7 describes Type 1XK Pins.

Table 7: Pin Descriptions

No.	Pin Name	Type	Connection to IC Pin Name	Description
1	GND			Ground
2	VIO	P	VIO VIO_RF VIO_SD	Power supply
3	SD_D2	I	SD_DAT[2]	SDIO 4-bit mode: Data line Bit[2] or read wait (optional) SDIO 1-bit mode: Read wait (optional)
4	SD_CLK	I	SD_CLK	SDIO Clock input
5	SD_D0	I	SD_DAT[0]	SDIO 4-bit mode: Data line Bit[0] SDIO 1-bit mode: Data line
6	SD_CMD	I/O	SD_CMD	SDIO 4-bit mode: Command/response (input/output) SDIO 1-bit mode: Command line
7	GPIO(9) UART_RXD	I/O	GPIO[9]	GPIO mode: GPIO[9] (input/output) UART mode: UART_SIN (input)
8	GPIO(6)	I/O	GPIO[6]	GPIO mode: GPIO[6] (input/output) PCM mode: PCM_CLK - PCM data clock (input if slave, output if master). I2S mode: I2S_BCLK - I2S bit clock (input if slave, output if master). PTA mode: EXT_PRI - External radio priority signal (input).
9	GPIO(7)	I/O	GPIO[7]	GPIO mode: GPIO[7] (input/output) PCM mode: PCM_SYNC - PCM frame sync (input if slave, output if master). I2S mode: I2S_LRCLK - I2S left-right clock (input if slave, output if master). PTA mode: EXT_REQ - Request from the external radio (input).
10	NC			NC *Floating terminal pad. Recommended grounding for mechanical strength.

No.	Pin Name	Type	Connection to IC Pin Name	Description
11	GPIO(4)	I/O	GPIO[4]	GPIO mode: GPIO[4] (input/output) PCM mode: PCM_DOUT ¹ - PCM transmit signal (output). I2S mode: I2S_DOUT/I2S_DIN (depending on the configuration. If GPIO[5] is configured as I2S_DIN, then GPIO[4] is set as I2S_DOUT, and vice-versa). PTA mode: EXT_FREQ - External radio frequency signal (input). Out-of-band wake-up mode: IW416 Alternate Bluetooth to host wake-up signal (output) ²
12	GPIO(1)	I/O	GPIO[1]	GPIO mode: GPIO[1] (input/output) This pin is used as a configuration pin: CON[9] (input). PTA mode: EXT_STATE - External radio state signal (input). Out-of-band wake-up mode: IW416 Wi-Fi to host wake-up signal (output) Do not drive this signal during boot-up
13	GPIO(15) TMS	I/O	GPIO[15]	GPIO mode: GPIO[15] (input/output) Reset recovery mode: Independent software reset for Bluetooth subsystem (input).
14	GPIO(5)	I/O	GPIO[5]	GPIO mode: GPIO[5] (input/output) PCM mode: PCM_DIN ³ - PCM receive signal (input). I2S mode: I2S_DOUT/I2S_DIN - I2S transmit/receive signal (output/input) (depending on the configuration). PTA mode: EXT_GNT - External radio grant signal (output).
15	GPIO(8) UART_CTS	I/O	GPIO[8]	GPIO mode: GPIO[8] (input/output) This pin is used as a configuration pin: CON[7] (input) UART mode: UART_CTSn - UART clear-to-send input signal (input, active low). Do not drive this signal during boot-up
16	GND			Ground
17	GPIO(14) TCK	I/O	GPIO[14]	GPIO mode: GPIO[14] (input/output) Reset recovery mode: Independent software reset for Wi-Fi subsystem (input)
18	GPIO(2) TDI	I/O	GPIO[2]	GPIO mode: GPIO[2] (input/output) Power management mode: DVSC[0], Digital voltage scaling control (output)
19	SLP_CLK_IN	I	SLP_CLK_IN	Sleep Clock Input (optional) Used for lower power operation in sleep mode. An external sleep clock of 32.768 kHz can be used for lowest current consumption in sleep mode. An external sleep clock is required if automatic reference clock frequency detection is used. If no external sleep clock is used, leave this pin floating (DNC).
20	GPIO(3) TDO	I/O	GPIO[3]	GPIO mode: GPIO[3] (input/output) Power management mode: DVSC[1], Digital voltage scaling control (output) PCM mode: PCM_MCLK (output) - PCM clock signal (output, optional). I2S mode: I2S_CCLK - I2S clock (output, optional).
21	GND			Ground
22	VBAT	P	PVIN(PMIC)	Power supply

¹ The function can be swapped with GPIO(5) using a software command without affecting the hardware connection.

² If PCM not used in application, GPIO(4) can be used as Bluetooth to host wake-up signal.

³ The function can be swapped with GPIO(4) using a software command without affecting the hardware connection.

No.	Pin Name	Type	Connection to IC Pin Name	Description
23	VBAT	P	PVIN(PMIC)	Power supply
24	GND			Ground
25	GND			Ground
26	GND			Ground
27	GND			Ground
28	GND			Ground
29	GND			Ground
30	GND			Ground
31	PMIC_EN	I	EN(PMIC)	Enable build-in PMIC. Logic high enables internal regulators and internal hardware reset is de-asserted. Logic low disables regulators and internal hardware reset is asserted. Do not float this pin
32	WCI_SOUT			WCI-2_SOUT (output)
33	WCI_SIN			WCI-2_SIN (input)
34	GPIO(12)	I/O	GPIO[12]	GPIO mode: GPIO[12] (input/output) UART mode: UART_DSRn - UART data-set-ready (input) (active low). Host wake-up mode: Host to IW416 Bluetooth wake-up (input)
35	RF_CNTL1_P	O	RF_CNTL1_P	Reserved Set to 1.
36	RF_CNTL0_N	O	RF_CNTL0_N	RF Control 0—RF Control Output Low (output) This pin is used as a configuration pin: CON[0] (input).
37	GND			Ground
38	RF_ANT			
39	GND			Ground
40	GND			Ground
41	GND			Ground
42	RF_CNTL2_N	O	RF_CNTL2_N	Reserved Do not pull-up externally.
43	RF_CNTL3_P	O	RF_CNTL3_P	Reserved
44	GND			Ground
45	BT_ANT SHARED	I		BT in (Feedback)
46	GND			Ground
47	BT_ANT DEDICATED	O		BT output
48	GND			Ground
49	GND			Ground
50	GND			Ground
51	GPIO(11) UART_RTS	I/O	GPIO[11]	GPIO mode: GPIO[11] (input/output) This pin is used as a configuration pin: CON[8] (input) UART mode: UART_RTSn - UART request-to-send (output) (active low). Do not drive this signal during boot-up
52	GPIO(0)	I/O	GPIO[0]	GPIO mode: GPIO[0] (input/output)
53	GPIO(13)	I/O	GPIO[13]	GPIO mode: GPIO[13] (input/output) UART mode: UART_DTRn - UART data-terminal-ready (output). Out-of-band wake-up mode: Host to IW416 Wi-Fi wake-up (input)
54	GPIO(10) UART_TXD	I/O	GPIO[10]	GPIO mode: GPIO[10] (input/output) UART mode: UART_SOUT - UART serial (output).

No.	Pin Name	Type	Connection to IC Pin Name	Description
55	SD_D3	I	SD_DAT[3]	SDIO 4-bit mode: Data line Bit[3] SDIO 1-bit mode: Reserved
56	SD_D1	I	SD_DAT[1]	SDIO 4-bit mode: Data line Bit[1] SDIO 1-bit mode: Interrupt
57-81	GND			Ground



Not all GPIO pins can be used for Host-to-SoC wake-up signals.

7.3 Configuration Pins

Table 8 shows the pins used as configuration inputs to set parameters following a reset. The definitions of these pins change immediately after reset to their usual function.

Table 8: Configuration Pins

Configuration Bits	Pin Name	Configuration Function
CON[9]	GPIO[1]	Reserved Set to 111.
CON[8]	GPIO[11]	
CON[7]	GPIO[8]	
CON[1]	RF_CNTL2_N	Firmware Boot Options: No hardware impacts. Software reads and boots accordingly. See Table 9 . Note: Boot code needs to use this host boot strap status to decide the correct boot sequence.
CON[0]	RF_CNTL0_N	

Table 9: Configuration Functions for Wi-Fi and Bluetooth/LE

CON[1]	CON[0]	Wi-Fi	Bluetooth/LE
1	0	SDIO	UART
1	1	Reserved	Reserved



To set a configuration bit to 0, attach a 50 kΩ - 100 kΩ resistor from the pin to ground. No external circuitry is required to set a configuration bit to 1.

7.4 Pin States

Pin states information for **Table 10** include:

- After firmware is downloaded, the pads (GPIO, Serial interface, RF control) are programmed in functional mode per the functionality of the pins.
- For SDIO, once the command is received from the host, the pads are configured accordingly.
- Pull-up and pull-down are only effective when the pad is in input mode.
- The power-down state shown is the default configuration. Many pads have programmable power-down values, which can be set by firmware.
- Do not need any termination to the open pins in input mode that have an Internal pull-up/pull-down resistor (PU/PD). Do not need any termination to the open pins in output mode.

Table 10: I/O State Table

Pin Name	Supply	No Pad Power State	Reset State	HW State ⁴	PD State ⁵	PD Prog ⁶	Internal PU/PD	Int'l Pull Value[Ω] ⁷
GPIO0	VIO	tristate	output	output	drive low	yes	nominal PU	90K
GPIO1	VIO	tristate	input	input	tristate	yes	weak PU	800K
GPIO2	VIO	tristate	input	input	tristate	yes	weak PU	800K
GPIO3	VIO	tristate	input	input	tristate	yes	weak PU	800K
GPIO4	VIO	tristate	output	input	tristate	yes	nominal PU	90K
GPIO5	VIO	tristate	input	input	tristate	yes	weak PU	800K
GPIO6	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO7	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO8	VIO	tristate	input	input	drive low	yes	weak PU	800K
GPIO9	VIO	tristate	output	input	tristate	yes	nominal PU	90K
GPIO10	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO11	VIO	tristate	output	input	drive high	yes	weak PU	800K
GPIO12	VIO	tristate	input	input	tristate	yes	nominal PU	90K
GPIO13	VIO	tristate	input	input	drive high	yes	nominal PU	90K
SD_CLK	VIO_SD	tristate	input	input	tristate	no	nominal PD	90K
SD_CMD	VIO_SD	tristate	input	input	tristate	no	nominal PD	90K
SD_D0	VIO_SD	tristate	input	input	tristate	no	nominal PD	90K
SD_D1	VIO_SD	tristate	input	input	tristate	no	nominal PD	90K
SD_D2	VIO_SD	tristate	input	input	tristate	no	nominal PD	90K

⁴ Hardware default state after reset

⁵ Power-down state

⁶ Power-down state programmable

⁷ Calculate appropriate external pull values with internal pull value

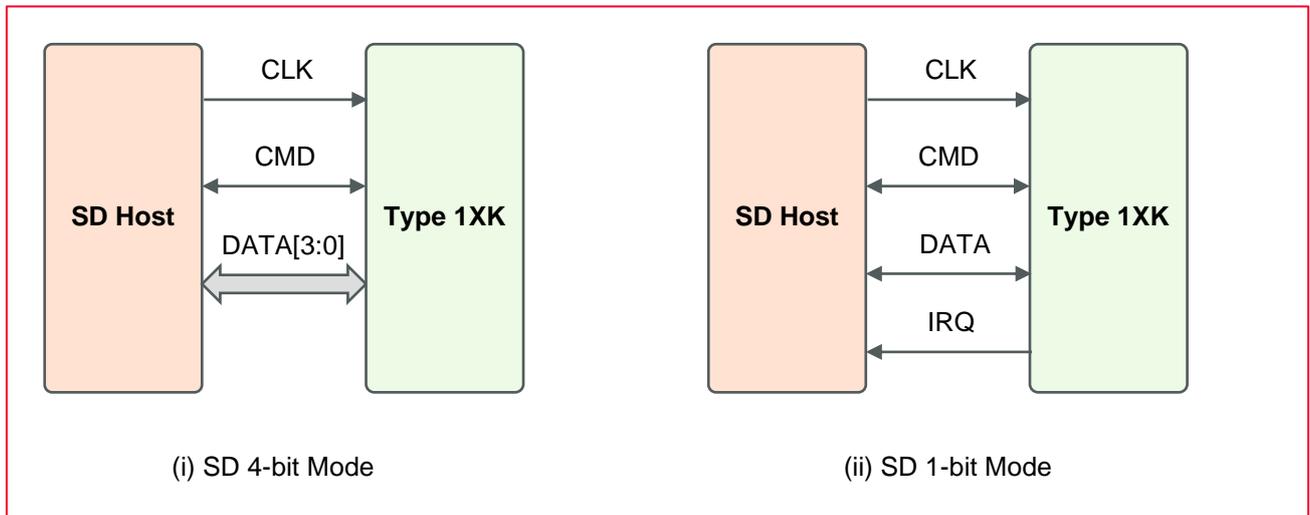
Pin Name	Supply	No Pad Power State	Reset State	HW State ⁴	PD State ⁵	PD Prog ⁶	Internal PU/PD	Int'l Pull Value[Ω] ⁷
SD_D3	VIO_SD	tristate	input	input	tristate	no	nominal PD	90K
RF_CNTL0_N	VIO_RF	tristate	input	output	drive low	yes	weak PU	800K
RF_CNTL1_P	VIO_RF	tristate	input	output	drive high	yes	weak PU	800K
RF_CNTL2_N	VIO_RF	tristate	input	output	drive low	yes	weak PU	800K
RF_CNTL3_P	VIO_RF	tristate	input	output	drive high	yes	weak PU	800K
SLP_CLK_IN	AVDD18	tristate	input	input	tristate	no	nominal PU	90K
WCI-2_SIN	AVDD18	tristate	input	input	tristate	no	weak PU	800K
WCI-2_OUT	AVDD18	tristate	output	output	tristate	no	weak PU	800K

Table 11 shows the pin descriptions for Type 1XK module. **Figure 5** shows the SDIO pin diagram for Type 1XK module.

Table 11: SDIO Pin Descriptions

No.	Pin Name	(i) SD 4-bit Mode		(ii) SD 1-bit Mode	
4	SDIO_CLK	CLK	Clock	CLK	Clock
5	SDIO_D0	DATA0	Data line 0	DATA	Data line
45	SDIO_D1	DATA1	Data line 1	IRQ	Interrupt
3	SDIO_D2	DATA2	Data line 2	RW	Read wait (optional)
46	SDIO_D3	DATA3	Data line 3	NC	Reserved
6	SDIO_CMD	CMD	Command/response	CMD	Command line

Figure 5: SDIO Pins



8 Absolute Maximum Ratings

The absolute maximum ratings are shown in **Table 12**.

Table 12: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-40	85	°C
Supply Voltage	VBAT	-0.3	6.0	V
	VIO		4.0	V



Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

9 Operating Conditions

9.1 Operating Conditions

The operating conditions are shown in **Table 13**.

Table 13: Operating Conditions

Parameter		Minimum	Typical	Maximum	Unit
Operating Temperature	Ta	-40	25	+85	°C
	Tj			+125	°C
Supply Voltage	VBAT	2.7		5.5	V
	VIO	1.62	1.8	1.98	V
		2.97	3.3	3.47	V
IO Current	VIO		0.1	0.5	mA
Peak Current	VBAT		550	850	mA



- Operation beyond the recommended operating conditions is neither recommended nor guaranteed.
- Peak current of VBAT (RF portion) is happen during DPD calibration when the firmware is downloaded.

9.2 External Sleep Clock Requirements

Table 14 shows the external sleep clock requirements for Type 1XK module.

Table 14: External Sleep Clock Requirements

Symbol	Parameter	Minimum	Typical	Maximum	Unit
CLK	Clock frequency range/accuracy: <ul style="list-style-type: none"> • CMOS input clock signal type • ± 250 ppm (initial, aging, temperature) 		32.768		kHz

Symbol	Parameter	Minimum	Typical	Maximum	Unit
PN	Phase Noise Requirement (@ 100 kHz)		-125		dBc/Hz
Jc	Cycle jitter		1.5		ns (RMS)
SR	Slew rate limit (10-90%)			100	ns
DC	Duty cycle tolerance	20		80	%



Voltage input level = 1.8V

9.3 PMIC_EN I/O Requirement

Table 14 shows the digital I/O requirements for Type 1XK module.

Table 15: PMIC_EN IO Requirements

Symbol	Parameter	Minimum	Maximum	Unit
V _{PMIC_EN_IH}	Input high voltage	1.2		V
V _{PMIC_EN_IL}	Input low voltage		0.4	V

9.4 Digital I/O Requirements

Table 16 shows the digital I/O requirements for Type 1XK module.

Table 16: Digital I/O Requirements Parameters

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V _{IH}	Input high voltage		0.7*V _{IO}		V _{IO} + 0.4	V
V _{IL}	Input low voltage		-0.4		0.3*V _{IO}	V
V _{HYS}	Input hysteresis		100			mV
V _{OH}	Output high voltage		V _{IO} -0.4			V
V _{OL}	Output low voltage				0.4	V

9.5 Package Thermal Conditions

The package thermal conditions as shown in **Figure 6** are as below:

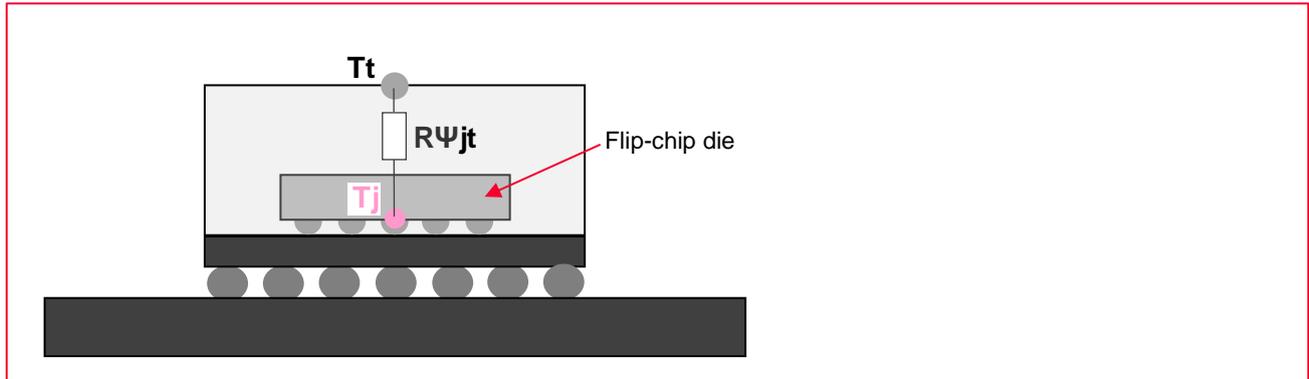
- $R\psi_{jt} : 3.56 \text{ } ^\circ\text{C/W}$
- $R\psi_{jt} = (T_j - T_t)/P$



T_j: Junction temperature (°C), T_t: Top temperature (°C), P: Total Power Consumption (W)

Figure 6 show the package thermal conditions.

Figure 6: Package Thermal Conditions



10 Power Sequence

This section describes the power-on and power-off sequences along with their parameters.

10.1 Power-On Sequence

- VBAT and VIO must be good (90%) at the same time or before assert PMIC_EN (= 0 to 1).
- Rump-up time of VIO must be < 100 ms

Figure 7: Power-On Sequence Graph

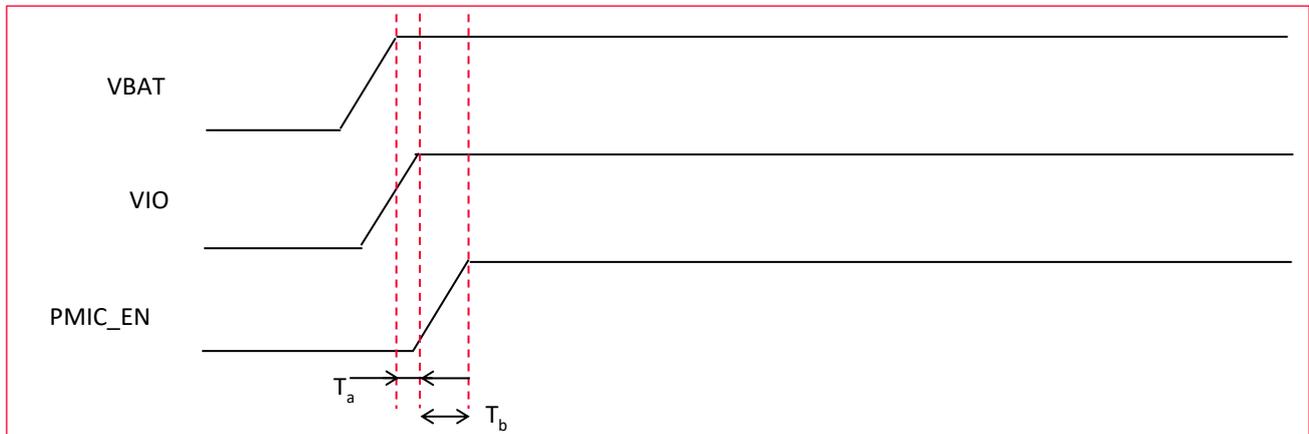


Table 17: Power-On Sequence Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_a	VBAT to VIO time	0			ms
T_b	VIO to PMIC_EN time	0			ms

10.2 Power-Off Sequence

10.2.1 Power-Off Sequence

- VBAT and VIO must be down at the same time or before de-assert PMIC_EN (= 1 to 0).
- Rump-down time of VIO must be < 100 ms

Figure 8: Power-Off Sequence Graph

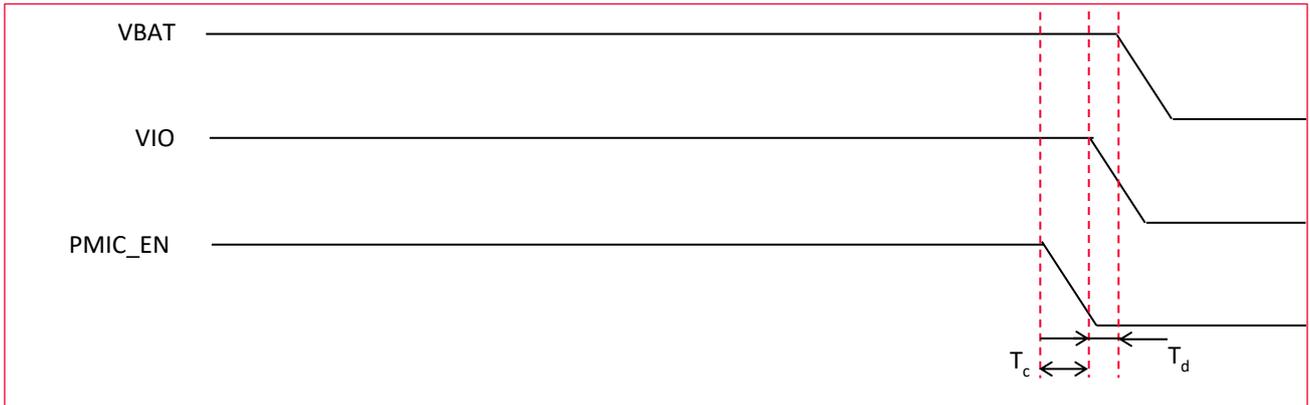


Table 18: Power-Off Sequence Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_c	PMIC_EN to VIO time	0			ms
T_d	VIO to VBAT time	0			ms

10.2.2 Host Power Off Pin (PMIC_EN) Usage

PMIC_EN must be asserted a minimum of 100 ms.

Figure 9: Host Power Off Pin (PMIC_EN) Usage Graph

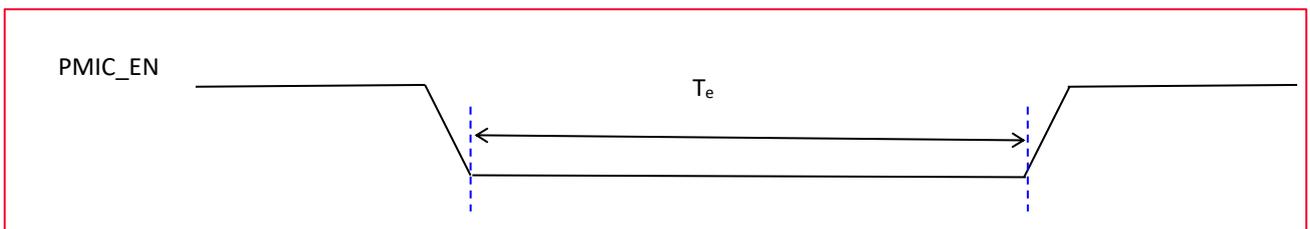


Table 19: Host Power Off Pin (PMIC_EN) Usage Parameters

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_e	PMIC_EN deassert to assert	100			ms

11 Interface Timing

This section describes the interface timing, its speed modes, related parameters, and graphs.

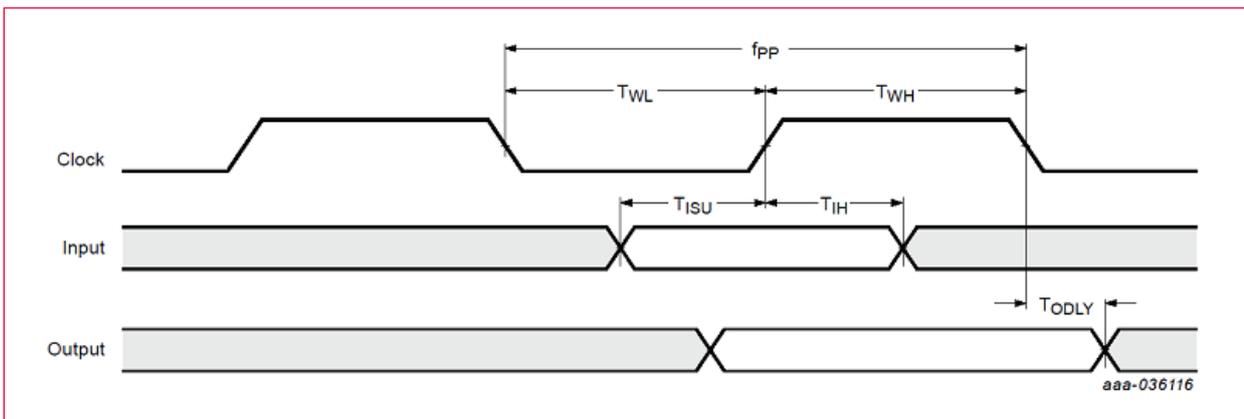
11.1 SDIO Timing

This section describes the SDIO timings for different modes.

11.1.1 Default Speed Mode

The default speed mode is shown in **Figure 10**.

Figure 10: SDIO Protocol Timing Diagram - Default Speed Mode



11.1.2 High Speed Mode

The high speed mode is shown in **Figure 11**.

Figure 11: SDIO Protocol Timing Diagram - High Speed Mode

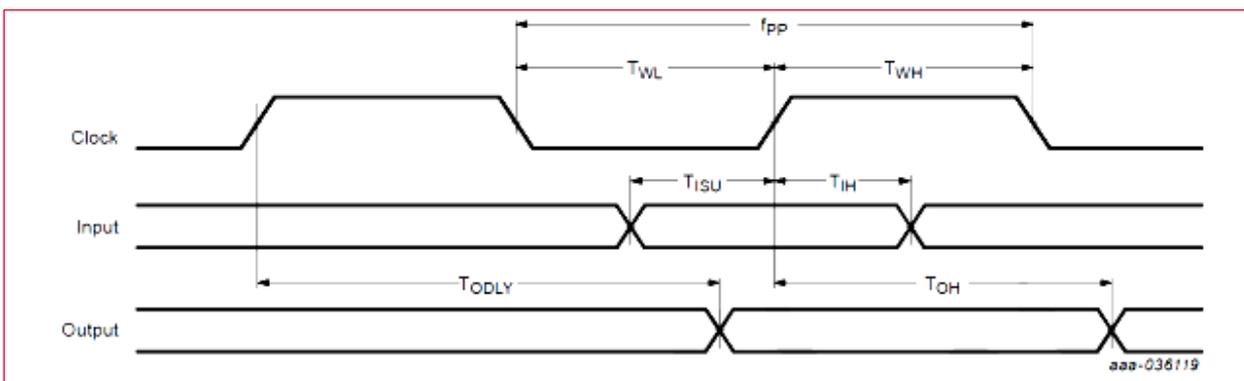


Table 20: SDIO Timing Data - High Speed Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{PP}	Clock frequency	Normal	0		25	MHz
		High speed	0		50	MHz
T_{WL}	Clock low time	Normal	10			ns
		High speed	7			ns

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T _{WH}	Clock high time	Normal	10			ns
		High speed	7			ns
T _{ISU}	Input Setup Time	Normal	5			ns
		High speed	6			ns
T _{IH}	Input hold Time	Normal	5			ns
		High speed	2			ns
T _{ODLY}	Output delay time	Normal			14	ns
	CL ≤ 40 pF (1 card)	High speed			14	ns
T _{OH}	Output hold time	High speed	2.5			ns



For SDIO 2.0 running at 25 MHz and 50 MHz clock frequency, VIO_SD must be 3.3V.

11.1.3 SDR12, SDR25, and SDR50 Modes up to 100 MHz (1.8 V)

Figure 12 shows the SDIO protocol timing diagram for SDR12, SDR25, SDR50 modes (up to 100 MHz & 1.8 V).

Figure 12: SDIO Protocol Timing Diagram - SDR12, SDR25, and SDR50 Modes

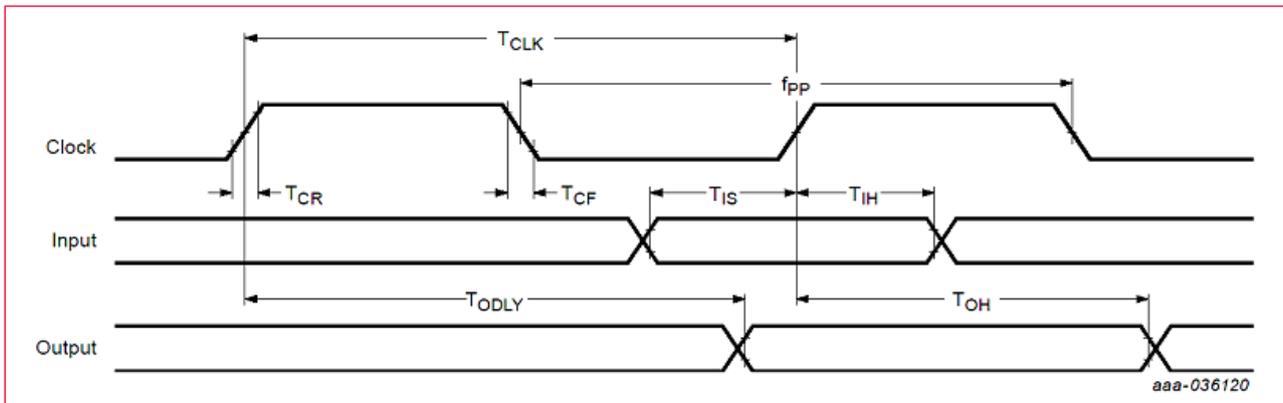


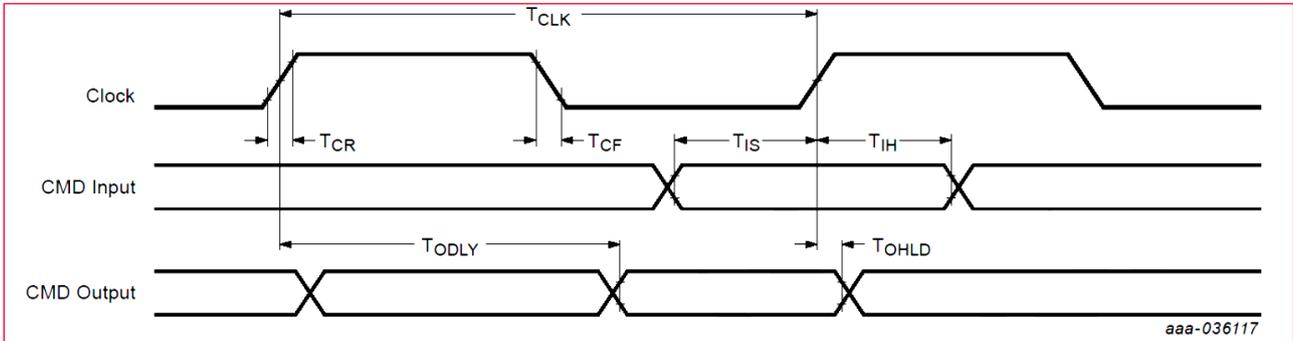
Table 21: SDIO Protocol Timing Parameters - SDR12, SDR25, and SDR50 Modes

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f _{PP}	Clock frequency	SDR12/25/50	25		100	MHz
T _{IS}	Input setup time	SDR12/25/50	3			ns
T _{IH}	Input hold time	SDR12/25/50	0.8			ns
T _{CLK}	Clock time	SDR12/25/50	10		40	ns
T _{CR} , T _{CF}	Rise time, fall time T _{CR} , T _{CF} < 2 ns (maximum) at 100 MHz C _{CARD} = 10 pF	SDR12/25/50			0.2 * T _{CLK}	ns
T _{ODLY}	Output delay time C _L ≤ 30 pF	SDR12/25/50			7.5	ns
T _{OH}	Output hold time C _L = 15 pF	SDR12/25/50	1.5			ns

11.1.4 DDR50 Mode at 50 MHz (1.8V)

Figure 13 shows the SDIO CMD timing diagram for DDR50 mode (up to 50 MHz and 1.8V).

Figure 13: SDIO CMD Timing Diagram - DDR50 Mode



In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line).

Figure 14 shows the SDIO DATA timing diagram for DDR50 mode.

Figure 14: SDIO DATA Timing Diagram - DDR50 Mode

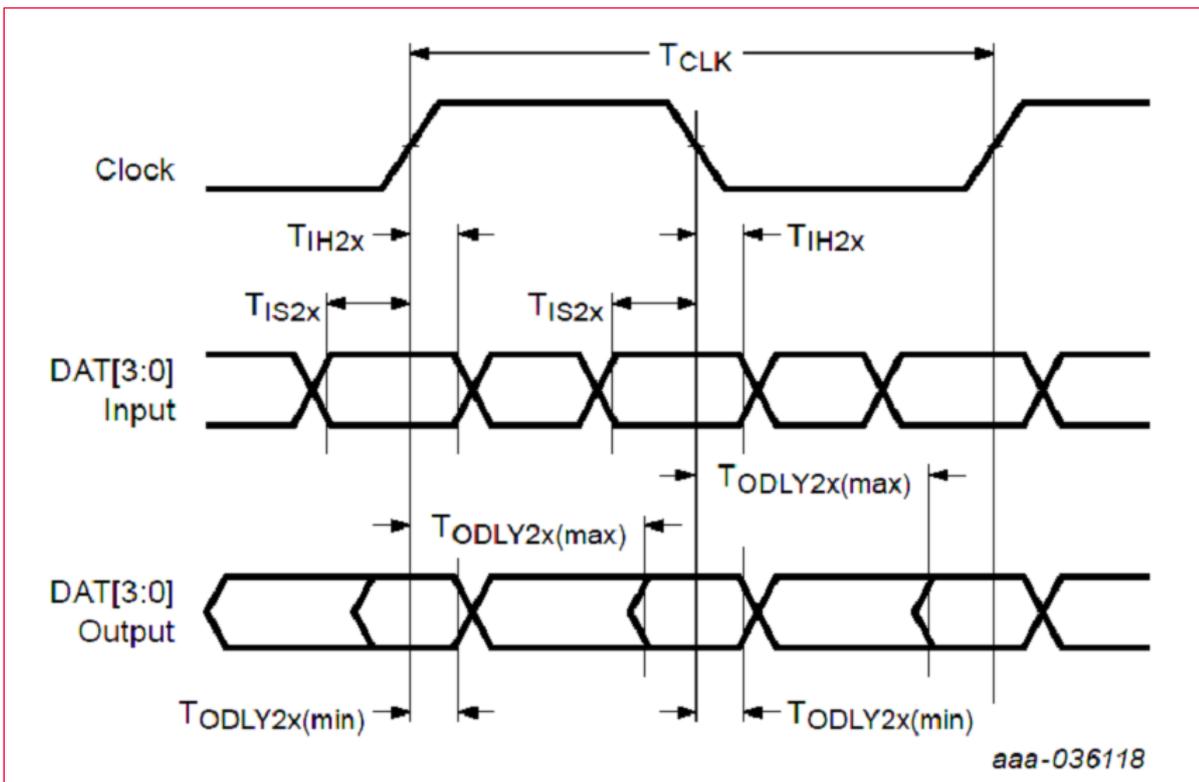


Table 22: SDIO Protocol Timing Parameters - DDR50 Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Clock						
T _{CLK}	Clock time 50 MHz (maximum) between rising edges	DDR50	20			ns
T _{CR} , T _{CF}	Rise time, fall time T _{CR} , T _{CF} < 4.00 ns(maximum) at 50 MHz C _{CARD} =10 pF	DDR50			0.2*T _{CLK}	ns
Clock Duty		DDR50	45		55	%
CMD Input (referenced to clock rising edge)						
T _{IS}	Input setup time C _{CARD} ≤ 10 pF (1 card)	DDR50	6			ns
T _{IH}	Input hold time C _{CARD} ≤ 10 pF (1 card)	DDR50	0.8			ns
CMD Output (referenced to clock rising edge)						
T _{ODLY}	Output delay time during data transfer mode C _L ≤ 30 pF (1 card)	DDR50			13.7	ns
T _{OHL D}	Output hold time C _L ≥ 15 pF (1 card)	DDR50	1.5			ns
DAT [3:0] Input (referenced to clock rising and falling edges)						
T _{IS2x}	Input setup time C _{CARD} ≤ 10 pF (1 card)	DDR50	3			ns
T _{IH2x}	Input hold time C _{CARD} ≤ 10 pF (1 card)	DDR50	0.8			ns
DAT [3:0] Output (referenced to clock rising and falling edges)						
T _{ODLY2x (max)}	Output delay time during data transfer mode C _L ≤ 25 pF (1 card)	DDR50			7.0	ns
T _{ODLY2x (min)}	Output hold time C _L ≥ 15 pF (1 card)	DDR50	1.5			ns

11.2 UART Timing (Default Mode)

Figure 15 show the UART timing default mode. The default baud rate is 115200 bps. Baud rate is configurable by the host stack.

Figure 15: UART Timing Diagram

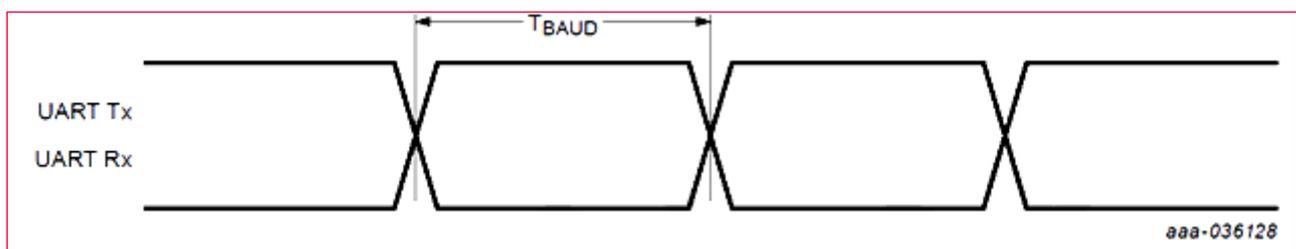


Table 23: UART Timing Data

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
TBAUD	Baud rate	38.4 MHz	250			ns



The acceptable deviation from the UART Rx target baud rate is $\pm 3\%$.

11.3 Bluetooth PCM Timing

This section describes the master and slave modes for Bluetooth PCM and data signals along with their parameters.

11.3.1 Master Mode

Figure 16 and **Figure 17** shows the timing diagram of master mode for Bluetooth data and PCM_SYNC signals.

Figure 16: Bluetooth Data Signal - Master Mode

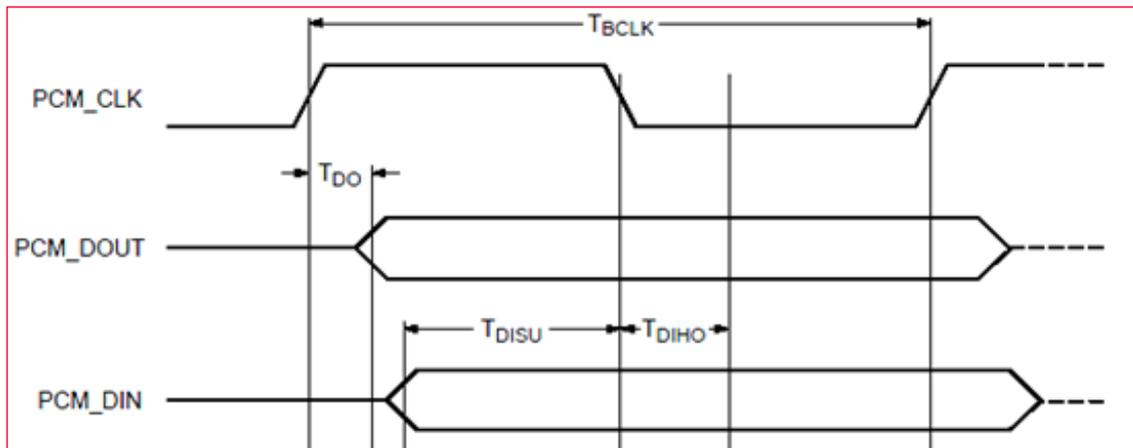


Figure 17: Bluetooth PCM_SYNC Signal - Master Mode

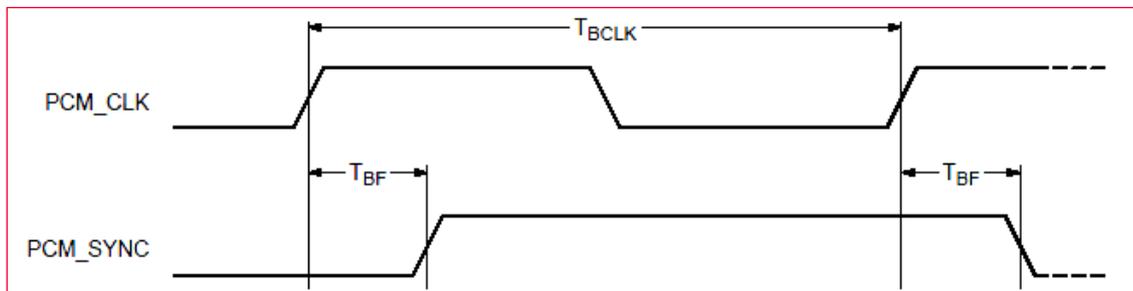


Table 24 lists information about the data and PCM_SYNC signals in master mode.

Table 24: Symbol Definition for Data Signal & PCM_SYNC Signal - Master Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
F_{BCLK}	Bit clock frequency			2/2.048		MHz
Duty Cycle $_{BCLK}$	Bit clock duty cycle		0.4	0.5	0.6	
$T_{BCLK\ rise/fall}$	PCM_CLK rise/fall time			3		ns
T_{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge				15	ns
T_{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge		20			ns
T_{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge		15			ns
T_{BF}	Delay from PCM_CLK rising edge to PCM_SYNC rising edge				15	ns

11.3.2 Slave Mode

Figure 18 and **Figure 19** shows the timing diagram of slave mode for data and PCM_SYNC signals. **Table 25** lists information about the data and PCM_SYNC signals in slave mode.

Figure 18: Bluetooth Data Signal - Slave Mode

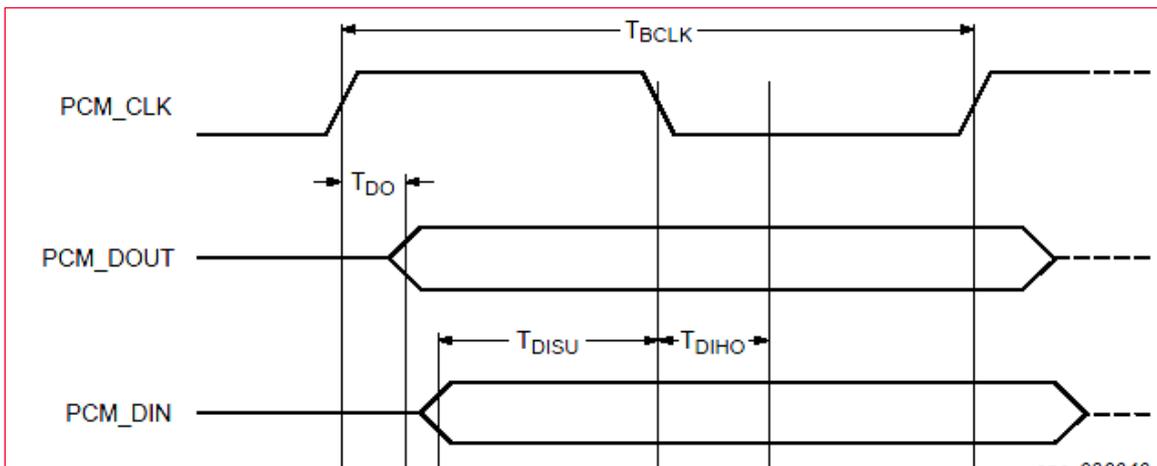


Figure 19: Bluetooth PCM_Sync Signal - Slave Mode

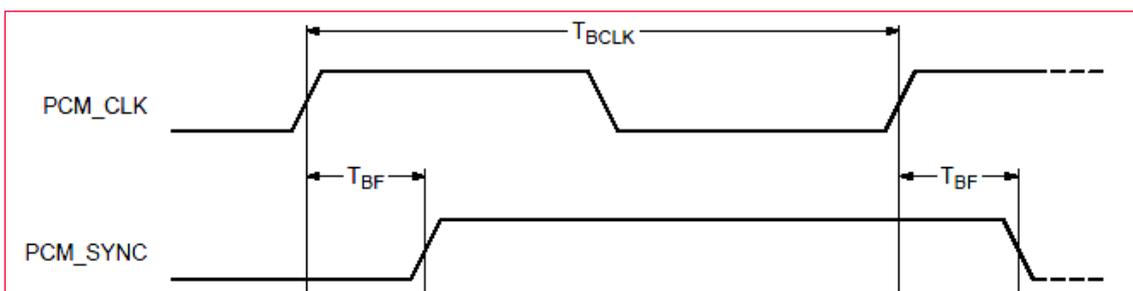


Table 25: Symbol Definition for Data Signal & PCM_SYNC Signal - Slave Mode

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
F _{BCLK}	Bit clock frequency			2/2.048		MHz
Duty Cycle _{BCLK}	Bit clock duty cycle		0.4	0.5	0.6	
T _{BCLK rise/fall}	PCM_CLK rise/fall time			3		ns
T _{DO}	Delay from PCM_CLK rising edge to PCM_DOUT rising edge				30	ns
T _{DISU}	Setup time for PCM_DIN before PCM_CLK falling edge		15			ns
T _{DIHO}	Hold time for PCM_DIN after PCM_CLK falling edge		10			ns
T _{BFSU}	Setup time for PCM_SYNC before PCM_CLK falling edge		15			ns
T _{BFHO}	Hold time for PCM_SYNC after PCM_CLK falling edge		10			ns

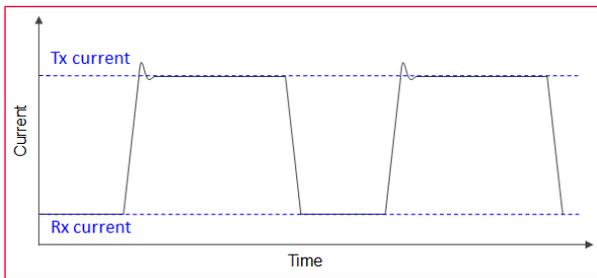
12 DC/RF Characteristics

All DC/RF characteristics are defined by following files as shown with file names in **Table 26**. **Figure 20** shows the burst current definition for Type 1XK module.

Table 26: DC/RF Characteristics and Files

Characteristics	Filenames
WLAN Tx Power	txpower_US.bin, txpower_CA.bin, txpower_EU.bin, txpower_JP.bin
WLAN Regulatory Limit	db.txt
Energy Detect	ed_mac.bin
Bluetooth Power	bt_power_config_1.sh (Class 1)

Figure 20: Burst Current Definition



12.1 DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Table 27: Characteristics Values for IEEE 802.11b - 2.4 GHz

Items	Contents
Specification	IEEE 802.11b
Mode	DSSS / CCK
Channel Frequency	2412 - 2472 MHz
Data Rate	1, 2, 5.5, 11 Mbps

12.1.1 High-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 17 dBm at module pad, 11 Mbps mode

Table 28: High-Rate Condition for IEEE 802.11b - 2.4 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		400	560	mA
• Rx mode		50	65	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	15.0	17.0	19.0	dBm
Spectrum Mask Margin				
• 1st side lobes (-30dBr)	0			dB
• 2nd side lobes (-50dBr)	0			dB
Power-on/off ramp			2.0	μs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Minimum Input Level (FER ≤ 8%)			-76	dBm
Maximum Input Level (FER ≤ 8%)	-10			dBm
Adjacent Channel Rejection (FER < 8%)	35			dB

12.1.2 Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 17 dBm at module pad, 1 Mbps mode

Table 29: Low-Rate Condition for IEEE 802.11b - 2.4 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		390	550	mA
• Rx mode		50	65	mA
Tx Characteristics				
Output Power	15.0	17.0	19.0	dBm
Spectrum Mask Margin				
• 1st side lobes (-30dB)	0			dB
• 2nd side lobes (-50dB)	0			dB
Power-on/off ramp			2.0	μs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics				
Minimum Input Level (FER ≤ 8%)			-80	dBm
Maximum Input Level (FER ≤ 8%)	-4			dBm
Adjacent Channel Rejection (FER < 8%)	35			dB

12.2 DC/RF Characteristics for IEEE 802.11g - 2.4 GHz

Table 30: Characteristics Values for IEEE 802.11g - 2.4 GHz

Items	Contents
Specification	IEEE 802.11g
Mode	OFDM
Channel Frequency	2412 - 2472 MHz
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.2.1 High-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 16 dBm at module pad, 54 Mbps mode

Table 31: High-Rate Condition for IEEE 802.11g - 2.4 GHz

Items	Contents			
DC Characteristics	Minimum	Typical	Maximum	Unit
DC Current				
• Tx mode		344	480	mA
• Rx mode		50	65	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	14.0	16.0	18.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM)			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Minimum Input Level (PER < 10%)			-65	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

12.2.2 Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 17 dBm at module pad, 6 Mbps mode

Table 32: Low-Rate Condition for IEEE 802.11g - 2.4 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		376	530	mA
• Rx mode		50	65	mA
Tx Characteristics				
Output Power	15.0	17.0	19.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics				
Minimum Input Level (PER < 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

12.3 DC/RF Characteristics for IEEE 802.11n (HT20) - 2.4 GHz

Table 33: Characteristics Values for IEEE 802.11n (HT20) - 2.4 GHz

Items	Contents
Specification	IEEE 802.11n 20 MHz BW
Mode	OFDM
Channel Frequency	2412 - 2472 MHz
Data Rate	MCS0-MCS7

12.3.1 High-Rate Condition for IEEE 802.11n (HT20) - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS7 mode

Table 34: High-Rate Condition for IEEE 802.11n (HT20) - 2.4 GHz

Items	Contents			
DC Characteristics	Minimum	Typical	Maximum	Unit
DC Current				
• Tx mode		320	450	mA
• Rx mode		50	65	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13.0	15.0	17.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.3.2 Low-Rate Condition for IEEE 802.11n (HT20) - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 16 dBm at module pad, MCS0 mode

Table 35: Low-Rate Condition for IEEE 802.11n (HT20) - 2.4 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		351	490	mA
• Rx mode		50	65	mA
Tx Characteristics				
Output Power	14.0	16.0	18.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
4. Constellation Error (EVM) (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics				
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.4 DC/RF Characteristics for IEEE 802.11a - 5 GHz

Table 36: Characteristics Values for IEEE 802.11a - 5 GHz

Items	Contents
Specification	IEEE 802.11a
Mode	OFDM
Channel Frequency	5180 to 5240 MHz, 5260 to 5320 MHz, 5500 to 5720 MHz, 5745 to 5825 MHz
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps

12.4.1 High-Rate Condition for IEEE 802.11a - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 16 dBm at module pad, 54 Mbps mode

Table 37: High-Rate Condition for IEEE 802.11a - 5 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		394	550	mA
• Rx mode		62	80	mA
Tx Characteristics				
Output Power	14.0	16.0	18.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics				
Minimum Input Level (PER ≤ 10%)			-65	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.4.2 Low-Rate Condition for IEEE 802.11a - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 16 dBm at module pad, 6 Mbps mode

Table 38: Low-Rate Condition for IEEE 802.11a - 5 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		394	550	mA
• Rx mode		62	80	mA
Tx Characteristics				
Output Power	14.0	16.0	18.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		-20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics				
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

12.5 DC/RF Characteristics for IEEE 802.11n (HT20) - 5 GHz

Table 39: Characteristics Values for IEEE 802.11n (HT20) - 5 GHz

Items	Contents
Specification	IEEE 802.11n
Mode	OFDM
Channel Frequency	5180 to 5240 MHz, 5260 to 5320 MHz, 5500 to 5720 MHz, 5745 to 5825 MHz
Data Rate	MCS0-MCS7

12.5.1 High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS7 mode

Table 40: High-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		373	520	mA
• Rx mode		62	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13.0	15.0	17.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit

Items	Contents			
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.5.2 Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 15 dBm at module pad, MCS0 mode

Table 41: Low-Rate Condition for IEEE 802.11n (HT20) - 5 GHz

Items	Contents			
DC Characteristics	Minimum	Typical	Maximum	Unit
DC Current				
• Tx mode		373	520	mA
• Rx mode		62	80	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	13.0	15.0	17.0	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Minimum Input Level (PER ≤ 10%)			-82	dBm
Maximum Input Level (PER < 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.6 DC/RF Characteristics for IEEE 802.11n (HT40) - 5 GHz

Table 42: Characteristics Values for IEEE 802.11n (HT40) - 5 GHz

Items	Contents
Specification	IEEE 802.11n
Mode	OFDM
Channel Frequency	5190 to 5795 MHz
Data Rate	MCS0-MCS7

12.6.1 High-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 14 dBm at module pad, MCS7 mode

Table 43: High-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Items	Contents			
DC Characteristics	Minimum	Typical	Maximum	Unit
DC Current				
• Tx mode		352	490	mA
• Rx mode		69	90	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power	12.0	14.0	16.0	dBm
Spectrum Mask Margin				
• 19 MHz to 21 MHz (0 ~ -20 dBr)	0			dB
• 21 MHz to 40 MHz (-20 ~ -28 dBr)	0			dB
• 40 MHz to 60 MHz (-28 ~ -40 dBr)	0			dB
• 60 MHz to 80 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5 470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Minimum Input Level (PER ≤ 10%)			-61	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.6.2 Low-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V, Output power setting = 14 dBm at module pad, MCS0 mode.

Table 44: Low-Rate Condition for IEEE 802.11n (HT40) - 5 GHz

Items	Contents			
	Minimum	Typical	Maximum	Unit
DC Characteristics				
DC Current				
• Tx mode		352	490	mA
• Rx mode		69	90	mA
Tx Characteristics				
Output Power	12.0	14.0	16.0	dBm
Spectrum Mask Margin				
• 19 MHz to 21 MHz (0 ~ -20 dBr)	0			dB
• 21 MHz to 40 MHz (-20 ~ -28 dBr)	0			dB
• 40 MHz to 60 MHz (-28 ~ -40 dBr)	0			dB
• 60 MHz to 80 MHz (-40 dBr)	0			dB
Constellation Error (EVM) (measured at enhanced mode)			-5	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics				
Minimum Input Level (PER ≤ 10%)			-79	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

12.7 DC/RF Characteristics for Bluetooth

Table 45: Characteristics Values for Bluetooth

Items	Contents
Bluetooth specification (power class)	Version 5.2 (Class 1)
Channel Frequency (spacing)	2402 to 2480 MHz (1 MHz)
Number of RF Channel	79

12.7.1 Basic Data Rate Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V (Test method: Bluetooth Core Spec Vol.3 Part D)

Table 46: Basic Data Rate Condition

Items	Contents			
	Minimum	Typical	Maximum	Unit
Current Consumption				
• Tx mode DH5		84	110	mA
• Rx mode DH5		65	90	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power@DH5	0	3.0	6.3	dBm
Frequency range	2400		2483.5	MHz
20 dB bandwidth			1	MHz
Adjacent Channel Power ⁸				
• [M-N] = 2			-20	dBm
• [M-N] ≥ 3			-40	dBm
Modulation characteristics				
• Modulation $\Delta f_{1\text{avg}}$	140	151	175	kHz
• Modulation $\Delta f_{2\text{max}}$	115			kHz
• Modulation $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	0.8	1		
Carrier Frequency Drift				
• 1slot	-25		25	kHz
• 3slot / 5slot	-40		40	kHz
• Maximum Drift Rate			20	kHz/50 μ s
Rx Characteristics	Minimum	Typical	Maximum	Unit
BDR Sensitivity (BER ≤ 0.1%)		-93	-70	dBm
Maximum Input Level (BER ≤ 0.1%)	-20			dBm

⁸ Up to three spurious responses within Bluetooth limits are allowed.

12.7.2 Enhanced Data Rate Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V (Test method: Bluetooth Core Spec Vol.3 Part D)

Table 47: Enhanced Data Rate Condition

Items	Contents			
Current Consumption	Minimum	Typical	Maximum	Unit
• Tx mode 2DH5		81	110	mA
• Rx mode 2DH5		65	90	mA
• Tx mode 3DH5		81	110	mA
• Rx mode 3DH5		65	90	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Output Power@2DH5/3DH5	-3.0	0	3.3	dBm
Frequency range	2400		2483.5	MHz
20 dB bandwidth			1	MHz
Adjacent Channel Power ⁹				
• [M-N] = 2			-20	dBm
• [M-N] ≥ 3			-40	dBm
EDR Relative Power	-4		1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
• ω_i	-75		75	kHz
• $\omega_i + \omega_o$	-75		75	kHz
• ω_o	-10		10	kHz
• RMS DEVM (DQPSK)			20	%
• Peak DEVM (DQPSK)			35	%
• 99% DEVM (DQPSK)			30	%
• RMS DEVM (8DPSK)			13	%
• Peak DEVM (8DPSK)			25	%
• 99% DEVM (8DPSK)			20	%
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
EDR Sensitivity (BER ≤ 0.007% @8DPSK)		-87	-70	dBm
Maximum Input Level (BER ≤ 0.1%)	-20			dBm

⁹ Up to three spurious responses within Bluetooth limits are allowed.

12.8 DC/RF Characteristics for Bluetooth Low Energy

Table 48: Characteristics Values for BLE

Items	Contents
Bluetooth specification (power class)	Version 5.2 (Class 1.5)
Channel Frequency (spacing)	2402 to 2480 MHz (2 MHz)
Number of RF Channel	40

12.8.1 1 Mbps PHY Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V (Test method: Bluetooth Core Spec Vol.6 Part F)

Table 49: 1 Mbps PHY Condition

Items	Contents			
Current Consumption	Minimum	Typical	Maximum	Unit
• Tx mode		80	110	mA
• Rx mode		73	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output Power	0	3.0	6.3	dBm
In-band emission				
• $f_{TX} \pm 2$ MHz			-20	dBm
• $f_{TX} \pm [3+n]$ MHz; n = 0,1,2...			-30	dBm
Modulation Characteristics				
• $\Delta f_{1\text{avg}}$	225		275	kHz
• $\Delta f_{2\text{max}}$ (at 99.9%)	185			kHz
• $\Delta f_{2\text{avg}} / \Delta f_{1\text{avg}}$	0.8			
Carrier frequency offset and drift				
• Frequency offset (f_n); n = 0,1,2,3...k	-150		150	kHz
• Frequency drift ($ f_0 - f_n $); n = 2,3,4...k			50	kHz
• Drift rate				
• $ f_1 - f_0 $			23	kHz
• $ f_n - f_{n-5} $; n = 6,7, 8,...k			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Receiver Sensitivity (PER < 30.8%)		-101	-70	dBm

Items	Contents			
Maximum input signal level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

12.8.2 2 Mbps PHY Condition

Conditions: 25 °C, VBAT = 3.3V, VIO = 1.8V (Test method: Bluetooth Core Spec Vol.6 Part F)

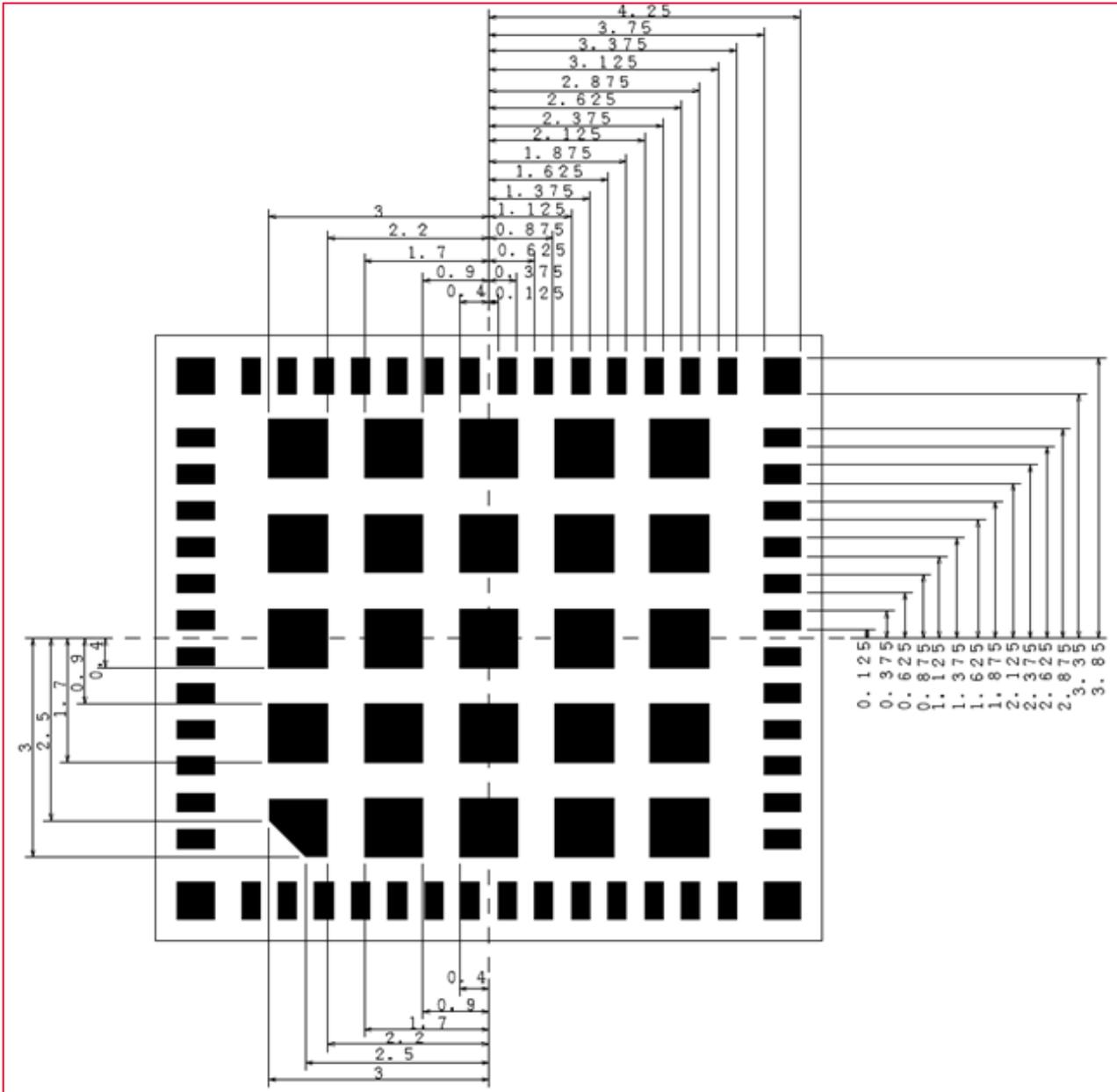
Table 50: 2 Mbps PHY Condition

Items	Contents			
Current Consumption	Minimum	Typical	Maximum	Unit
• Tx mode		76	100	mA
• Rx mode		73	95	mA
Tx Characteristics	Minimum	Typical	Maximum	Unit
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output Power	0	3.0	6.3	dBm
In-band emission				
• $f_{TX} \pm 4$ MHz			-20	dBm
• $f_{TX} \pm 5$ MHz			-20	dBm
• $f_{TX} \pm [6+n]$ MHz; $n = 0, 1, 2, \dots$			-30	dBm
Modulation Characteristics				
• Δf_{1avg}	450		550	kHz
• Δf_{2max} (at 99.9%)	370			kHz
• $\Delta f_{2avg} / \Delta f_{1avg}$	0.8			
Carrier frequency offset and drift				
• Frequency offset (f_n); $n = 0, 1, 2, 3, \dots k$	-150		150	kHz
• Frequency drift ($ f_0 - f_n $); $n = 2, 3, 4, \dots k$			50	kHz
• Drift rate				
• $ f_1 - f_0 $			23	kHz
• $ f_n - f_{n-5} $; $n = 6, 7, 8, \dots k$			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Rx Characteristics	Minimum	Typical	Maximum	Unit
Receiver Sensitivity (PER < 30.8%)		-99	-70	dBm
Maximum Input Signal Level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

13 Land Pattern

The land pattern is shown in **Figure 21**.

Figure 21: Land Pattern

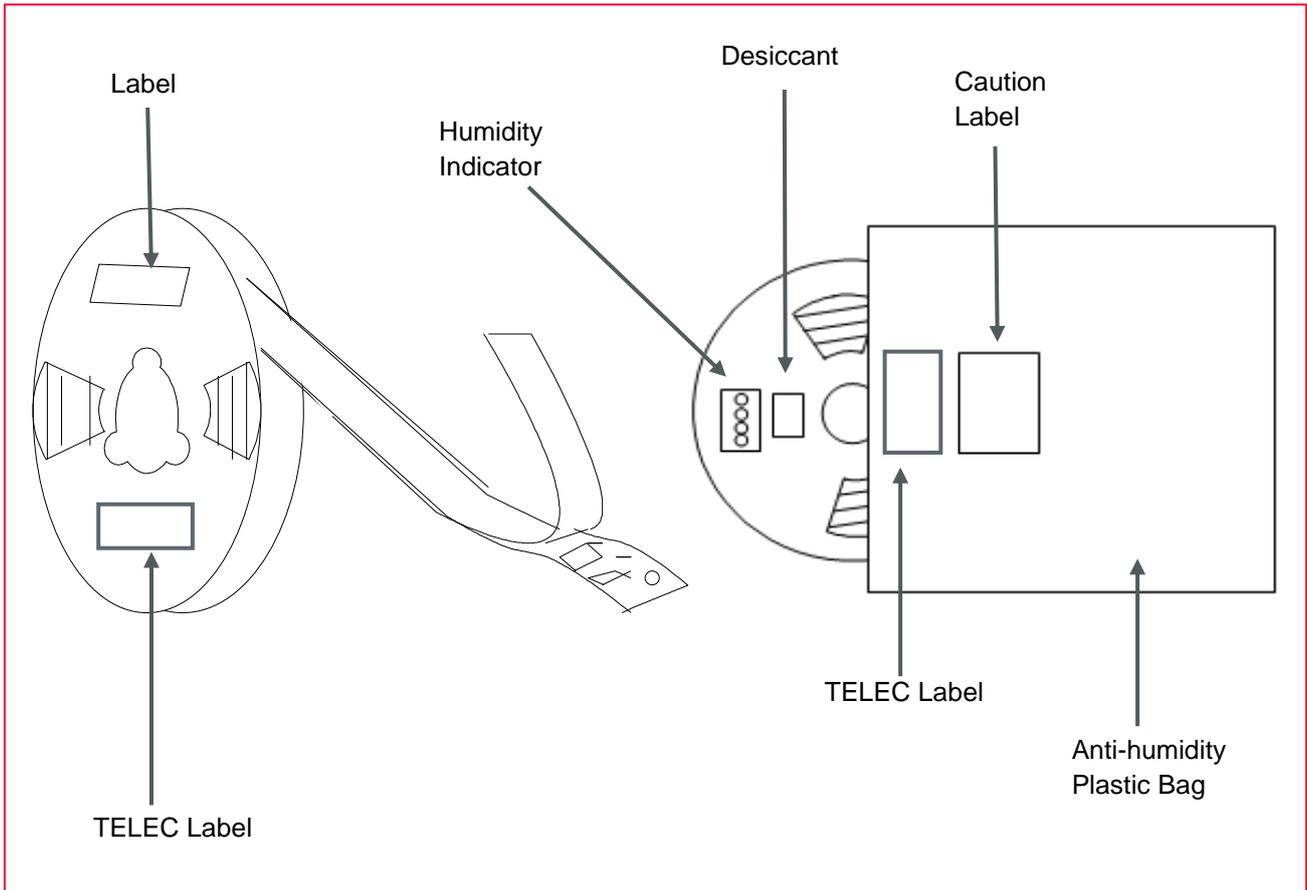


To avoid the short-circuit between the side shielding and a solder on the module land after the reflow, please locate the module land at 0.2 mm away from module outline as above figure.

13.1 Package Label

Figure 22 shows the package label information (Humidity Proof Packing)

Figure 22: Package Label (Humidity Proof Packing)



The package label may be attached on one side only.

Package label display example is shown in **Figure 23**.

Figure 23: Package Label Display Example





The above pictures are examples. It may be attached to only one of them.

13.2 Country of Origin

China

SHENZHEN MURATA TECHNOLOGY CO., LTD.

Some countries have applied for two countries, China, and Japan, in preparation for future factory changes, but the production site in the delivery specifications is the above-mentioned factory in China.

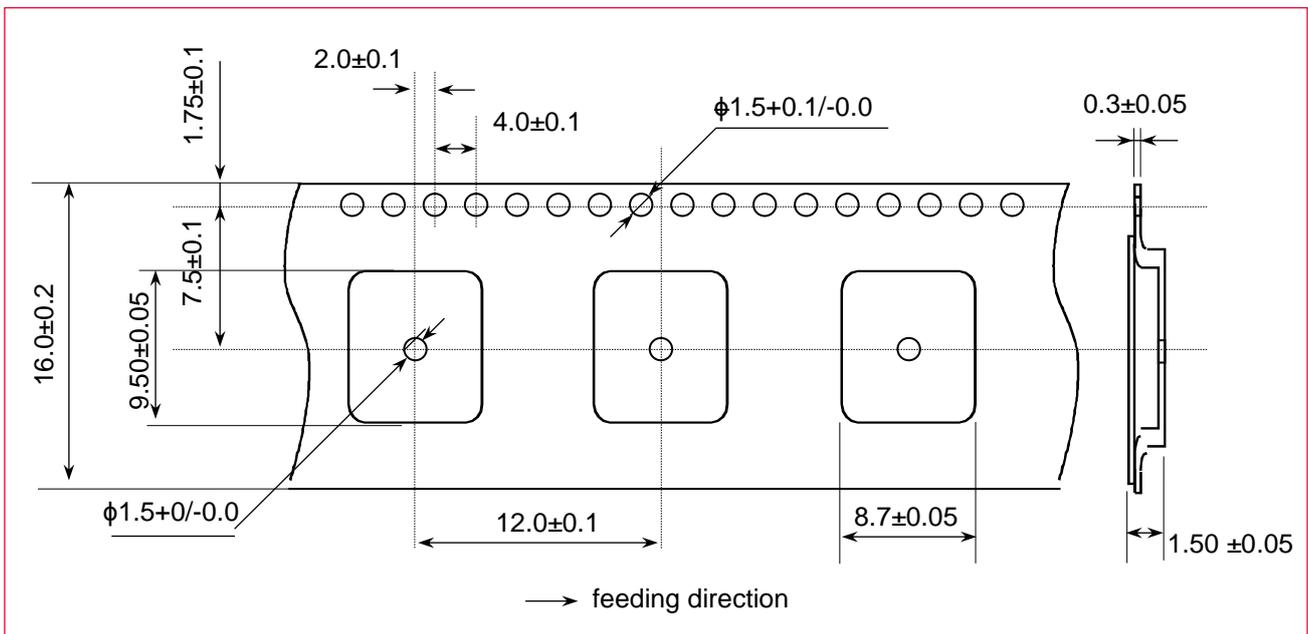
14 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

14.1 Dimensions of Tape (Plastic Tape)

Figure 24 is a graphical representation of the tape dimension (plastic tape)¹⁰

Figure 24: Dimensions of Tape (Unit: mm)

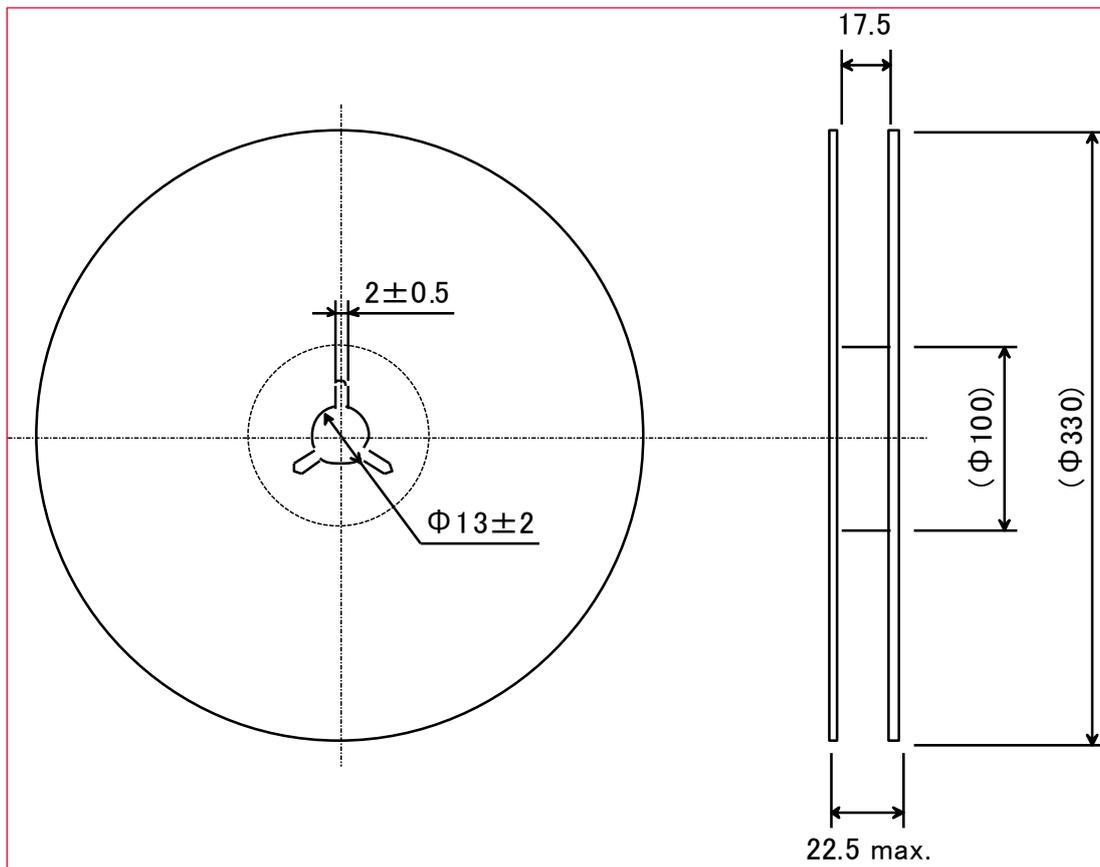


¹⁰ Cumulative tolerance of maximum 40 +/- 0.15 mm for every 10 pitches.

14.2 Dimension of Reel

Figure 25 shows the reel dimensions.

Figure 25: Dimensions of Reel (Unit: mm)



14.3 Taping Diagrams

Figure 26 shows the tapings diagrams.

Figure 26: Taping Diagrams

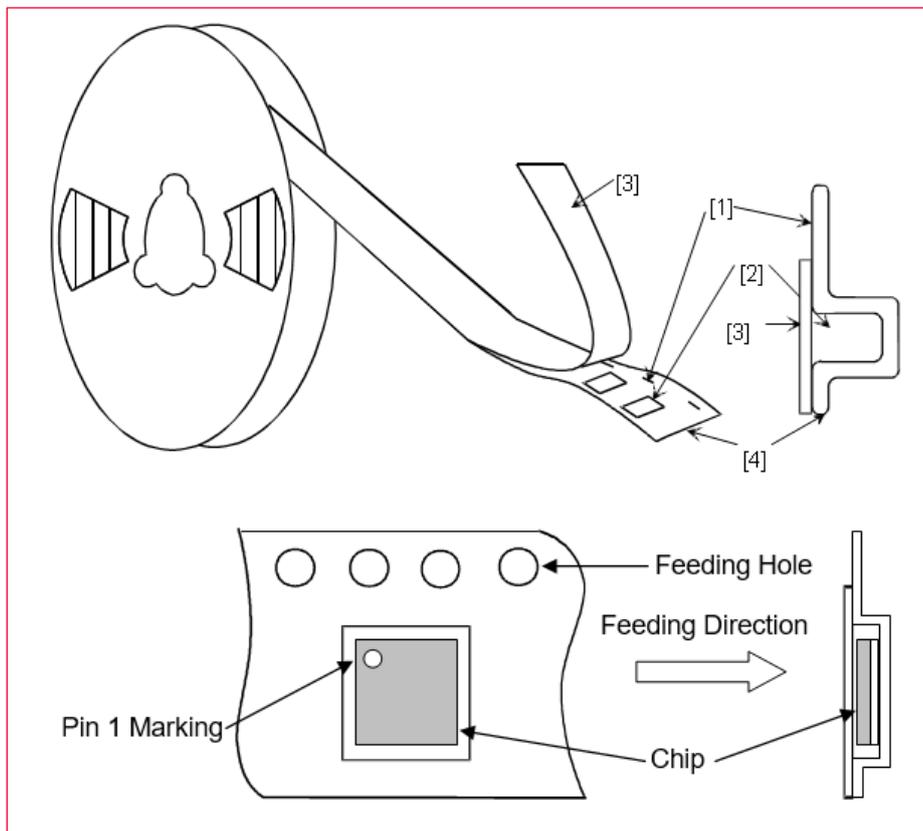


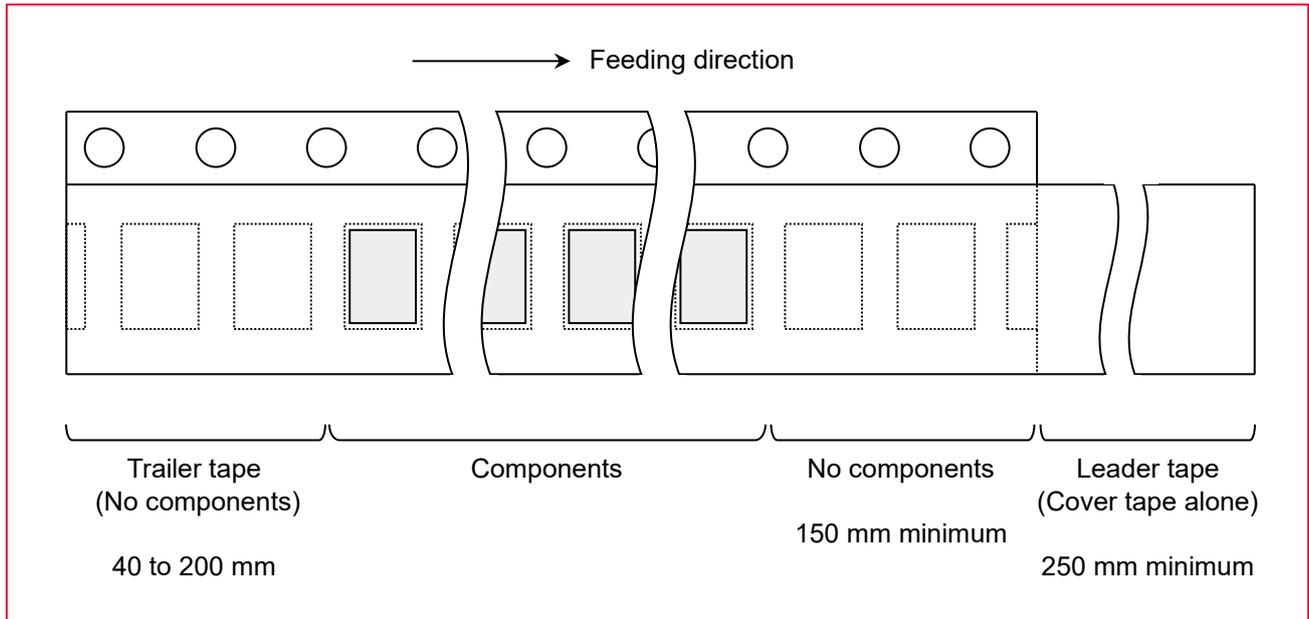
Table 51: Taping Specifications

Mark	Description
1	Feeding Hole. As specified in Dimensions of Tape (Plastic tape) ☞
2	Hole for chip. As specified in Dimensions of Tape (Plastic tape) ☞
3	Cover tape. 62 μm in thickness.
4	Base tape. As specified in Dimensions of Tape (Plastic tape) ☞

14.4 Leader and Tail Tape

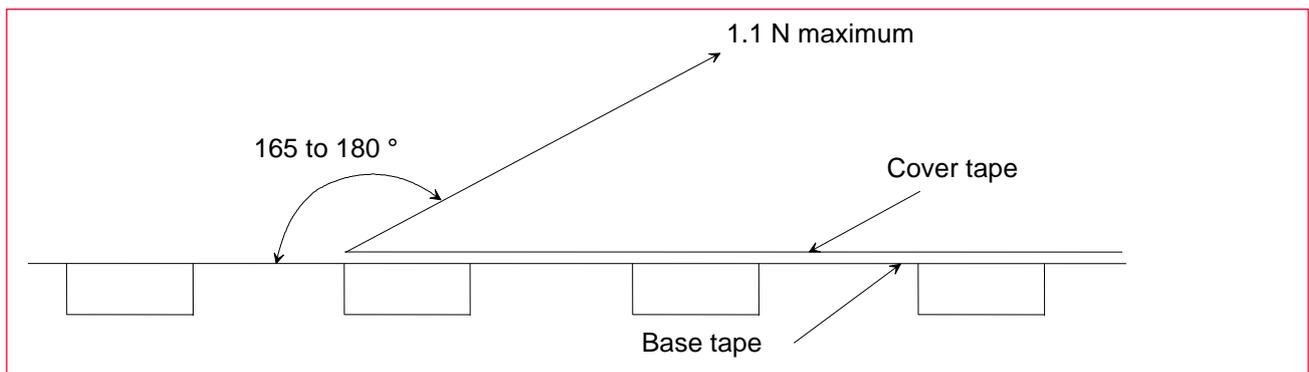
The leader and tail tape are shown in **Figure 27**.

Figure 27: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape: 5 N minimum.
- Packaging unit: 1000 pcs. / Reel
- Tape material:
 - Base tape: Plastic
 - Reel: Plastic
 - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling off force: 1.1 N maximum in the direction of peeling as shown in **Figure 28**.

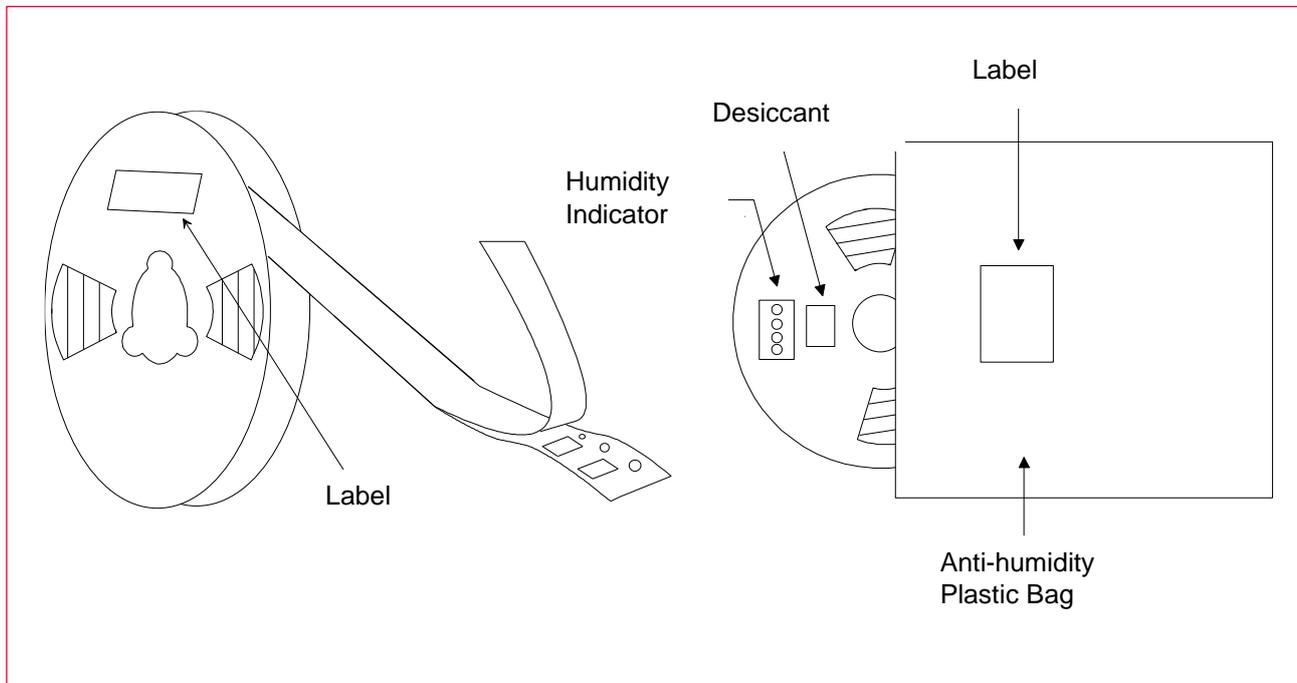
Figure 28: Peeling Force



14.5 Packaging (Humidity Proof Packing)

Figure 29 shows the humidity proof Packaging.

Figure 29: Humidity Proof Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

15 Notice

15.1 Storage Conditions

- Please use this product within 6 months after receipt.
- The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (Packing materials may be deformed at the temperature over 40 °C).
- The product left more than 6 months after reception; the solderability needs to be confirmed before it is used.
- The product shall be stored in non-corrosive gas (Cl₂, NH₃, SO₂, NO_x, etc.).
- Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object, and dropping the product, shall not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on IPC/JEDEC J-STD-020)
 - After the packing opened, the product shall be stored at <30 °C / <60 %RH and the product shall be used within 168 hours.
 - When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products shall be baked on the heat-resistant tray because the material (Base Tape, Reel Tape and Cover Tape) is not heat-resistant.

15.2 Handling Conditions

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bare hands that may result in poor solder ability and destroy by static electrical charge.

15.3 Standard PCB Design (Land Pattern and Dimensions):

- All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.
- The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

15.4 Notice for Chip Placer

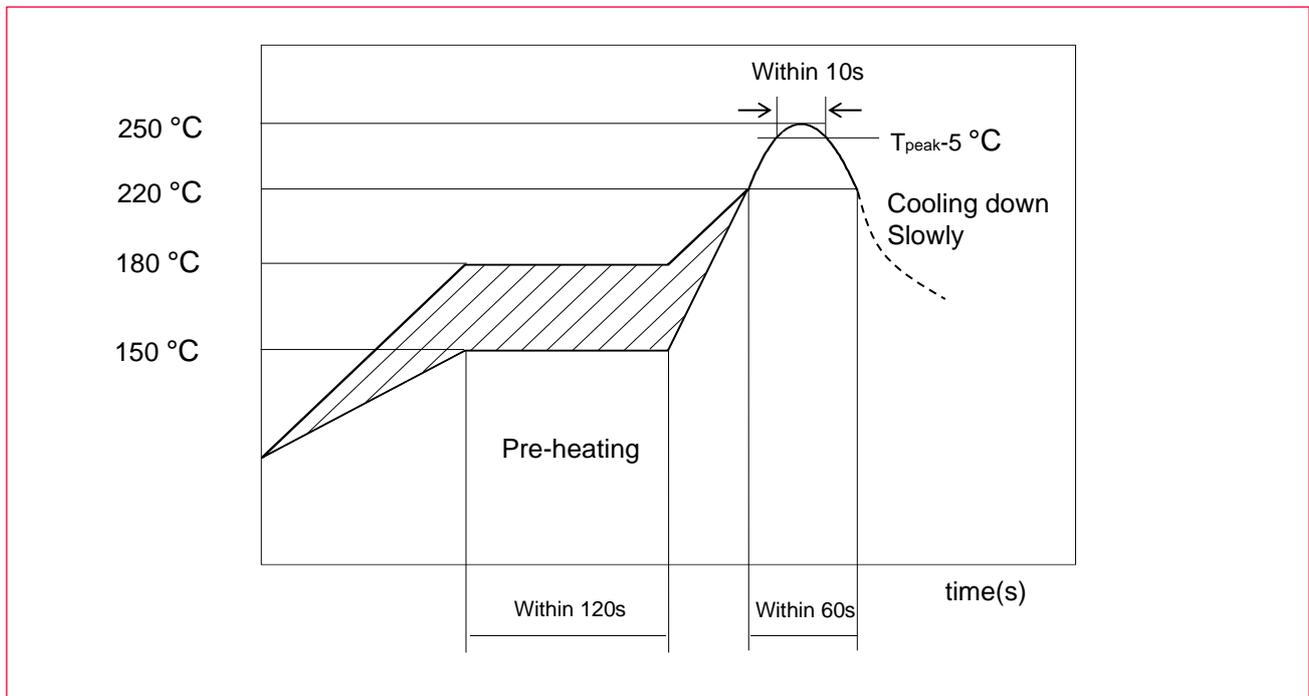
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

15.5 Soldering Conditions

The recommendation conditions of soldering are shown in **Figure 30**.

Soldering must be carried out by the above-mentioned conditions to prevent products from damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use if concerning other soldering conditions.

Figure 30: Reflow Soldering Standard Conditions (Example)



Please use the reflow within 2 times.

Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt. % or less.

15.6 Cleaning

This product is moisture sensitive; therefore, any cleaning is not recommended. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

15.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (Cl₂, NH₃, SO_x, NO_x etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.



If there are possibilities for products to be used under the preceding clause, consult with Murata before actual use.



Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

16 Preconditions to Use Our Products



PLEASE READ THIS NOTICE BEFORE USING OUR PRODUCTS.

Please make sure that your product has been evaluated and confirmed from the aspect of the fitness for the specifications of our product when our product is mounted to your product.

All the items and parameters in this product specification/datasheet/catalog have been prescribed on the premise that our product is used for the purpose, under the condition and in the environment specified in this specification. You are requested not to use our product deviating from the condition and the environment specified in this specification.

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- Aerospace equipment.
- Undersea equipment.
- Power plant control equipment.
- Medical equipment.
- Traffic signal equipment.

- Burning / explosion control equipment.
- Disaster prevention / crime prevention equipment.
- Transportation equipment (vehicles, trains, ships, elevator, etc.).
- Application of similar complexity and/ or reliability requirements to the applications listed in the above.
- We expressly prohibit you from analyzing, breaking, reverse-engineering, remodeling altering, and reproducing our product. Our product cannot be used for the product which is prohibited from being manufactured, used, and sold by the regulations and laws in the world.

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Revision History

Revision Code	Date	Changed Item	Comment
1	2020.12.16	First Issue	
2 (A)	2021.03.23	Top page 4. Block Diagram 9. Operating Conditions 11.2 High-speed UART specifications 12. DC/RF Characteristics	<ul style="list-style-type: none"> Removed "ac" Updated Updated operating temperature. Added default baud rate information. Added 802.11n 40 MHz in 2.4 GHz. Added Tx power values.
3 (B)	2021.03.31	14. Reference Circuit 15. Tape and Reel Packing	<ul style="list-style-type: none"> Added circuit for dedicated BT antenna. Added
4 (C)	2021.04.05	2. Key feature & 5.2 Bluetooth Qualification 7.1 Pin Assignments 7.2 Pin Descriptions	<ul style="list-style-type: none"> Added a comment on supported Bluetooth functions Corrected pin number Corrected pin number
5 (D)	2021.04.14	14. Reference Circuit	<ul style="list-style-type: none"> Corrected circuit for dedicated BT antenna
6 (E)	2021.05.19	2. Key Features 7.5 Pin States 14. Reference Circuit 12.8 DC/RF Characteristics for Bluetooth 12.9 DC/RF Characteristics for Bluetooth Low Energy	<ul style="list-style-type: none"> Added Weight Added Internal pull values Corrected circuit for Shard BT antenna Updated Output Power Updated Output Power
7 (F)	2021.06.10	12. DC/RF Characteristics	<ul style="list-style-type: none"> Delete 802.11n 40 MHz in 2.4 GHz.
8 (G)	2021.07.30	5. Certification Information 9. Operating Conditions 14. Reference Circuit	<ul style="list-style-type: none"> Added Certification Information Added DC current Removed dedicated BT antenna
9 (H)	2021.09.15	13. Land patterns	<ul style="list-style-type: none"> Updated figure
10 (I)	2021.10.14	3. Ordering Information 7. Module Pin Descriptions 12. DC / RF Characteristics 14. Reference Circuit	<ul style="list-style-type: none"> Added part number for MP Updated description of GPIOs and WCI IF Corrected values of Wi-Fi Current consumption. Corrected typo
11 (J)	2021.11.19	11.1.2 High Speed Mode 15. Tape and Reel Packing	<ul style="list-style-type: none"> Corrected the note on SDIO 2.0 mode. Corrected Dimensions of Tape
12 (K)	2021.11.25	6. Dimensions, Marking and Terminal Configurations	<ul style="list-style-type: none"> Corrected Dimensions <ul style="list-style-type: none"> a) e1: 0.38 → 0.375 b) e3: 0.48 → 0.475
13 (L)	2021.12.14	7.2 Pin Descriptions 7.4 Pin States 9.1 Operating Conditions 9.2 External Sleep Clock Requirements 10. Power Sequence 14. Reference Circuit	<ul style="list-style-type: none"> Added comments to pin 10 Added SLP_CLK_IN, WCI-2_SIN and WCI-2_SOUT. Defined IO current and Peak current Added a comment Defined timing parameters Pull-down RF_CNTL2_N and updated descriptions.

Revision Code	Date	Changed Item	Comment
14 (M)	2022.02.01	7.2 Pin Descriptions 7.3 Configuration Pins	<ul style="list-style-type: none"> Revised typo about the description in #52:GPIO[0]. Added Description for configuration pins
15 (N)	2022.04.19	9.1 Operating Conditions 9.4 Package Thermal Conditions 12.7 DC/RF Characteristics for Bluetooth 12.8 DC/RF Characteristics for Bluetooth	<ul style="list-style-type: none"> Defined Ta and Tj. Added Added test method Added test method
16 (O)	2022.04.27	14. Reference Circuit	<ul style="list-style-type: none"> Corrected Typo
17 (P)	2022.07.01	7.2 Pin Descriptions 7.3 Configuration Pins 14. Reference Circuit Appendix	<ul style="list-style-type: none"> Corrected GPIO[0], Deleted JTAG Added Description for configuration pins Corrected typo (P.22 VBAT) Translated Japanese to English Corrected diagram C
18 (Q)	2022.12.02	2. Key Features 10. Power Sequence 12. DC/RF Characteristics	<ul style="list-style-type: none"> Added fit Added 10.2.2 host power off pin (PMIC_EN) usage Corrected Wi-Fi 11a/b/g/n DC current Tx power
19 (R)	2023.01.13	2. Key Features 3. Ordering Information 6. Dimensions, Markings and Terminal Configurations 7.4 Pin States 14. Reference Circuit Appendix	<ul style="list-style-type: none"> Added more information. Added Embedded Artists' M.2 module information. Added Identification mark Added comment about termination of open pins. Moved section to HW app note. Moved antenna sections to HW app note. Moved Appendix information into Sections 14 and 15. <p>Updated to new format</p>
20 (S)	23.04.28	9.3 PMIC_EN I/O Requirement	<ul style="list-style-type: none"> Added PMIC_EN I/O Requirement (Base IC datasheet revision : 4)
21	2025.02.14	Revision History 6. Dimensions, Markings... 12. DC/RF Characteristics... (14. General for Radio...) (15. Radio Regulatory Cert...) 16. Preconditions to Use...	<ul style="list-style-type: none"> Changed Revision rule Added a structure figure and warning message Corrected typo of spectrum mask Removed stable modulation spec Removed the section Removed the section Updated



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