Datasheet

Type 1XA Wi-Fi™ + Bluetooth® Module

Infineon Chipset CYW54591 for 802.11a/b/g/n/ac 2x2 MIMO, RSDB + Bluetooth® 5.2

Datasheet - Rev. 15

- Design Name: Type 1XA
- Module P/N: LBEE5XV1XA-540

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About This Document

Type 1XA is a small and very high-performance module based on Infineon CYW54591 combo chipset which supports Wi-Fi™ 802.11a/b/g/n/ac 2×2 MIMO RSDB + Bluetooth 5.2 BR/EDR/LE. This datasheet describes Type 1XA module in detail.

Please be aware that an important notice concerning availability, standard warranty and use in critical applications of Murata products and disclaimers thereto appears at the end of this specification sheet.

Audience & Purpose

Intended audience includes any customer looking to integrate this module into their product; specifically RF, hardware, software, and systems engineers.

Document Conventions

Table 1 describes the document conventions.

Table 1: Document Conventions

Conventions	Description
	Warning Note Indicates very important note. Users are strongly recommended to review.
	Info Note Intended for informational purposes. Users should review.
	Menu Reference Indicates menu navigation instructions. **Example**: Insert➔Tables➔Quick Tables➔Save Selection to Gallery
	External Hyperlink This symbol indicates a hyperlink to an external document or website. **Example**: Murata Click on the text to open the external link.
	Internal Hyperlink This symbol indicates a hyperlink within the document. **Example**: Scope Click on the text to open the link.
`Console input/output or code snippet`	**Console I/O or Code Snippet** This text ***Style*** denotes console input/output or a code snippet.
`# Console I/O comment` `// Code snippet comment`	**Console I/O or Code Snippet Comment** This text ***Style*** denotes a console input/output or code snippet comment. • Console I/O comment (preceded by "#") is for informational purposes only and does not denote actual console input/output. • Code Snippet comment (preceded by "//") may exist in the original code.

1 Scope

This specification characterizes the IEEE 802.11a/b/g/n/ac 2x2 MIMO + Bluetooth 5.2 BR/EDR/LE combo module.

2 Key Features

- Infineon CYW54591 inside
- Supports IEEE 802.11a/b/g/n/ac specification: Dual band 2.4 GHz and 5 GHz
- 2x2 MIMO with 20 MHz, 40 MHz, and 80 MHz channels
- Supports RSDB (Real Simultaneous Dual Band)
- Up to MCS9 data rates (866 Mbps)
- Supports Bluetooth specification version 5.2
- For supported Bluetooth functions, refer to Bluetooth SIG site
- WLAN interface: PCIe 3.0
- Bluetooth interface: HCI UART and PCM
- Temperature Range: -40 °C to 85 °C
- Dimensions 11.4 x 8.9 x 1.4 mm
- Weight: 0.36 g
- MSL: 3
- Surface-mount type
- RoHS compliant
- Total Fit: 336.82

3 Ordering Information

Table 2 shows the ordering information.

Table 2: Ordering Information

Ordering Part Number	Description
LBEE5XV1XA-540	Module order
LBEE5XV1XA-SMP	Sample module order (If module samples are not available through distribution, contact Murata referencing this part number)
EAR00373	Embedded Artists Type 1XA M.2 EVB (default EVB available through distribution)

4 Block Diagram

The Type 1XA block diagram is presented in **Figure 1** and **Figure 2**.

Figure 1: Type1XA Block Diagram for Two Antenna Configuration

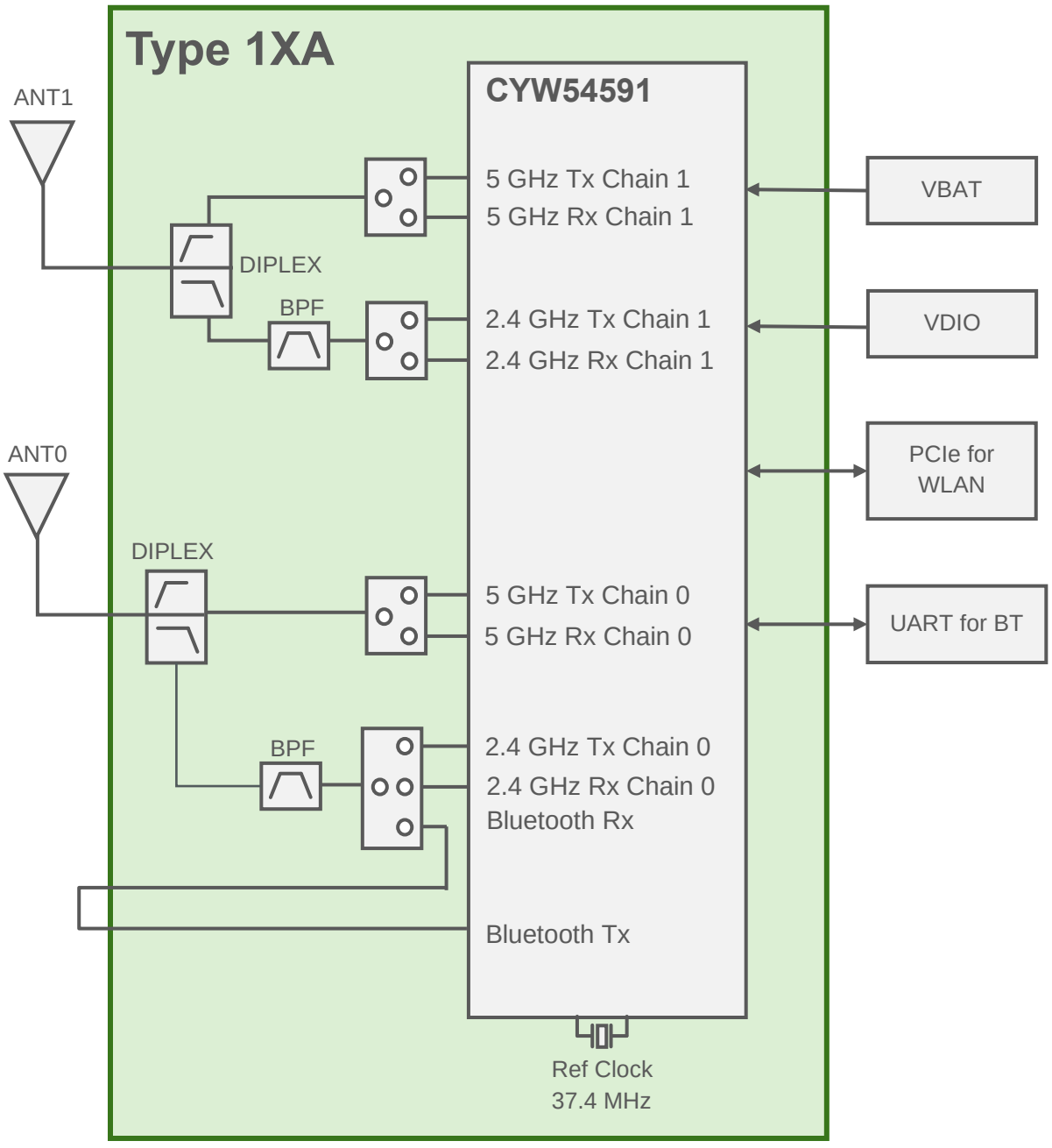
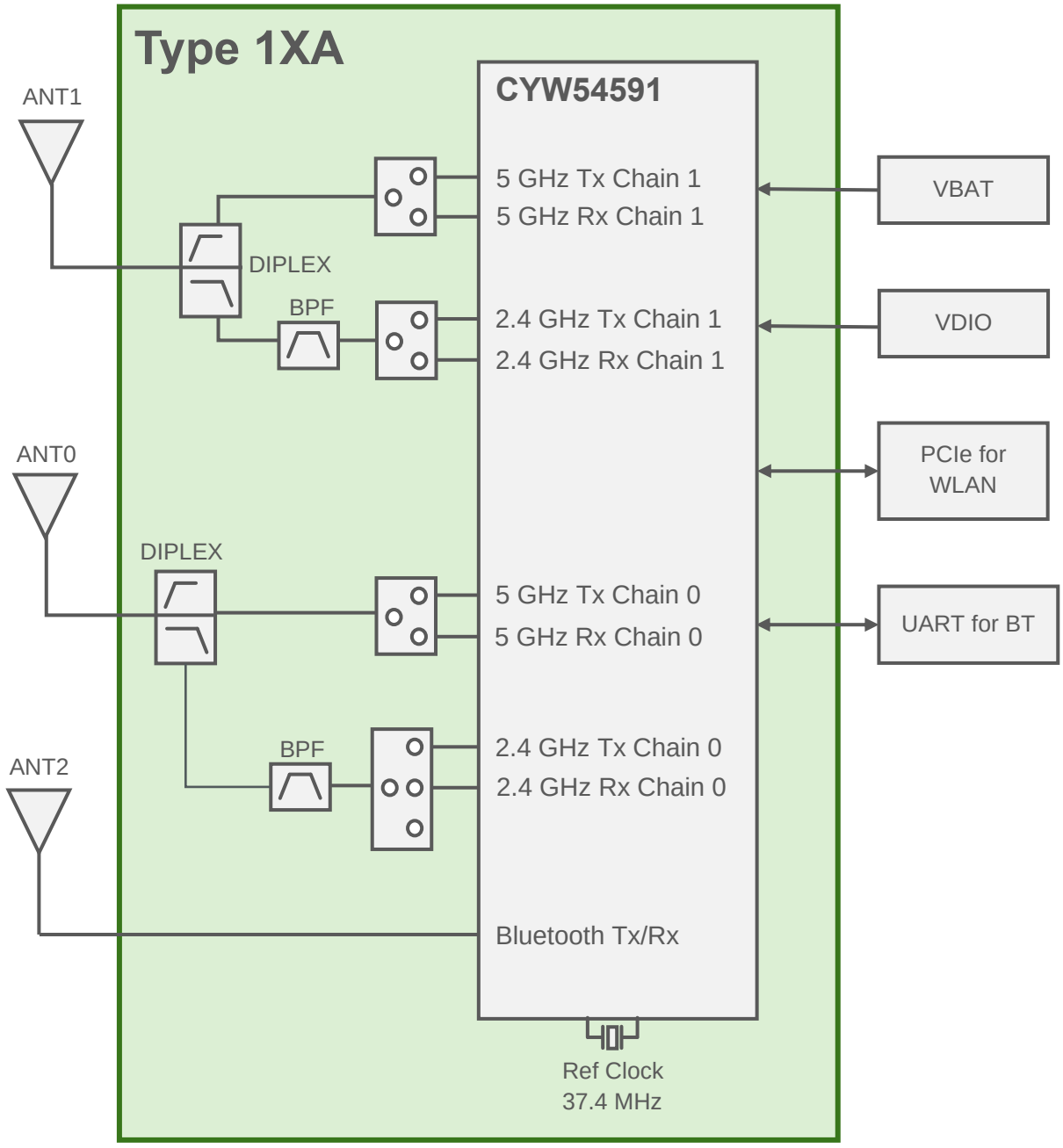


Figure 2: Type1XA Block Diagram for Three Antenna Configuration



5 Dimensions, Markings and Terminal Configurations

This section has information on dimensions, markings, and terminal configurations for Type 1XA.

Figure 3: Dimensions, Markings and Terminal Configurations

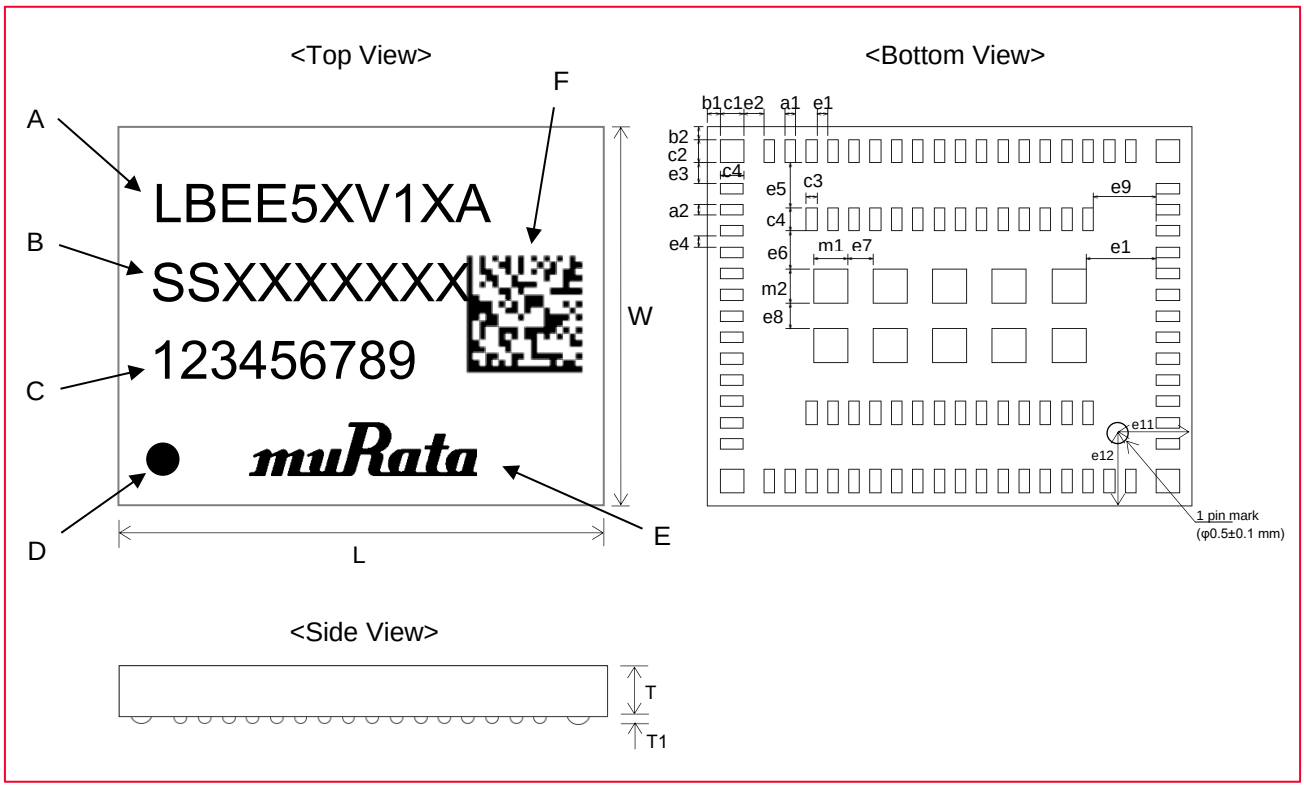


Table 3 describes the marking labels for the top and bottom view as shown in **Figure 3**.

Table 3: Markings

Marking	Meaning
A	Module Part Number
B	Inspection Number
C	Serial Number
D	Pin 1 Marking
E	Murata Logo
F	2D code

Table 4 describes the Type 1XA dimensions.

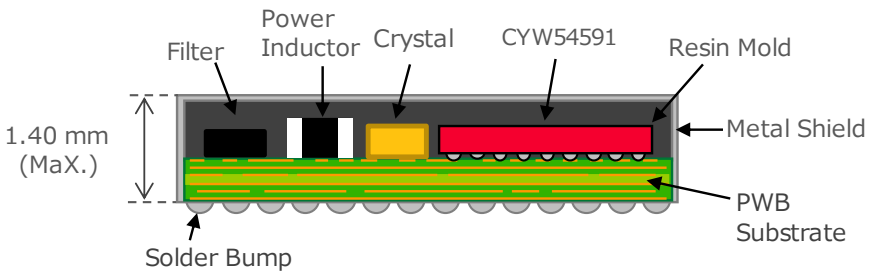
Table 4: Dimensions

Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)
L	11.4 ± 0.2	W	8.9 ± 0.2	T	1.4 max.	T1	0.04 typ.
a1	0.25 ± 0.1	a2	0.25 ± 0.1	b1	0.3 ± 0.2	b2	0.3 ± 0.2
c1	0.55 ± 0.1	c2	0.55 ± 0.1	c3	0.25 ± 0.1	c4	0.55 ± 0.1
e1	0.25 ± 0.1	e2	0.475 ± 0.1	e3	0.475 ± 0.1	e4	0.25 ± 0.1
e5	1.05 ± 0.1	e6	0.9 ± 0.1	e7	0.6 ± 0.1	e8	0.6 ± 0.1
e9	1.475 ± 0.1	e10	1.65 ± 0.1	e11	1.787 ± 0.2	e12	1.609 ± 0.2

Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)	Mark	Dimensions (mm)
m1	0.8 ± 0.1	m2	0.8 ± 0.1				

Figure 4 shows the Type 1XA structure.

Figure 4: Structure



The sides of the module are GND shielded. In order to avoid contact between the GND shield and the electrodes on the mother board, please carefully evaluate the standoff before use the module.

6 Module Pin Descriptions

This section describes the module pin assignments layout descriptions along with the pin descriptions.

6.1 Pin Assignments

The pin assignment (top view) layout is shown in **Figure 5**.

Figure 5: Pin Assignments - Top View

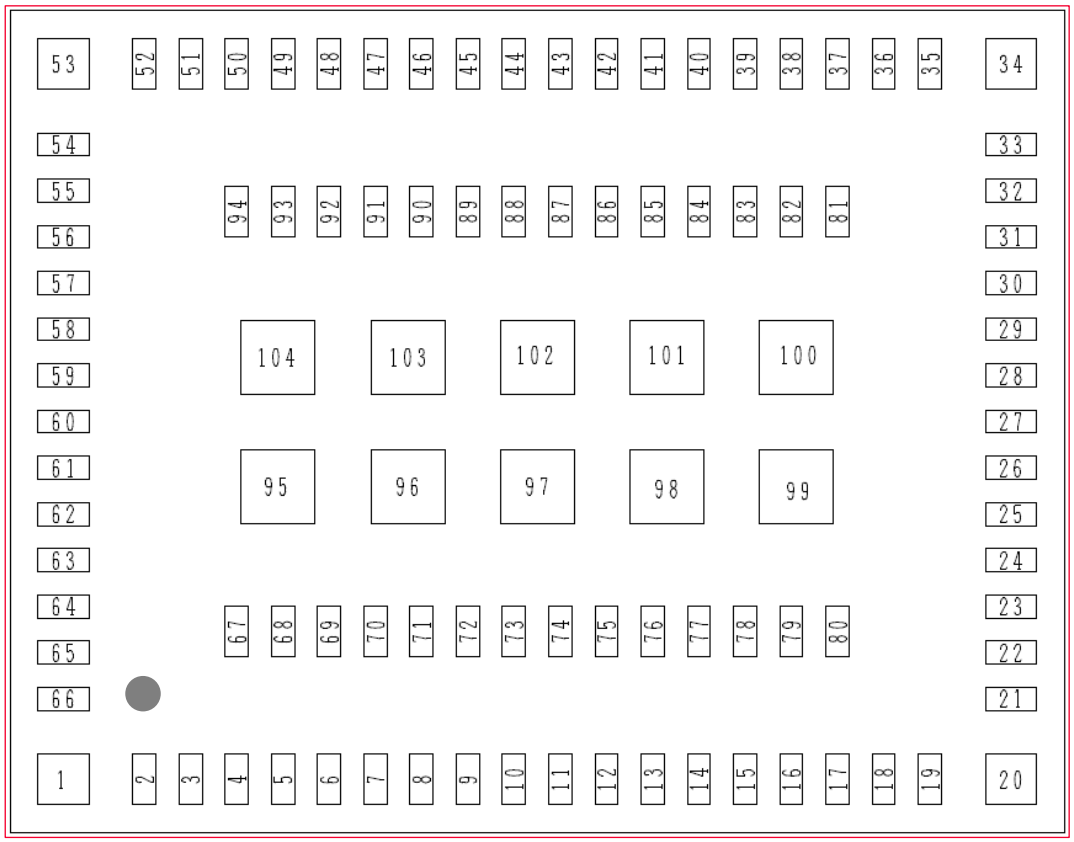


Table 5 illustrates the terminal configurations for Type 1XA.

Table 5: Terminal Configurations

No.	Terminal Name	No.	Terminal Name	No.	Terminal Name
1	GND	31	RF_SW_CTRL11	61	NC
2	GPIO_17	32	GND	62	NC
3	GPIO_18	33	ANT_1	63	NC
4	GPIO_19	34	GND	64	GND
5	WL_REG_ON	35	GND	65	VBAT
6	BT_REG_ON	36	BT_UART_RTS_N	66	VBAT
7	GND	37	BT_UART_CTS_N	67-73	GND
8	VDDIO	38	BT_UART_RXD	74	BT_PCM_IN
9	GND	39	BT_UART_TXD	75	BT_PCM_OUT
10	GND	40	GPIO_5	76	BT_PCM_CLK
11	GND	41	GPIO_4	77	BT_PCM_SYNC
12	BT_OUT	42	GPIO_7	78	GND
13	GND	43	GPIO_6	79	RF_SW_CTRL4
14	BT_IN	44	PCIE_PME_L	80	GND
15	GND	45	PCIE_PERST_L	81	RF_SW_CTRL12
16	RF_SW_CTRL5	46	PCIE_CLKREQ_L	82	BT_GPIO_5
17	GND	47	GND	83	BT_GPIO_4
18	GND	48	PCIE_RDN	84	BT_GPIO_2
19	ANT_0	49	PCIE_RDP	85	BT_GPIO_3
20	GND	50	GND	86	GPIO_3
21	GND	51	PCIE_REFCLKP	87	JTAG_SEL
22	BT_HOST_WAKE	52	PCIE_REFCLKN	88	GPIO_2
23	BT_DEV_WAKE	53	GND	89	GPIO_1
24	CLK_REQ	54	PCIE_TDN	90	GPIO_0
25	LPO_IN	55	PCIE_TDP	91	GPIO_8
26	BT_I2S_DO	56	GND	92	GPIO_9
27	BT_I2S_DI	57	VDDIO	93	GPIO_10
28	BT_I2S_CLK	58	NC	94	GPIO_11
29	BT_I2S_WS	59	NC	95-104	GND
30	GND	60	NC		

6.2 Pin Descriptions

Table 6 describes Type 1XA pins.

Table 6: Pin Descriptions

No.	Pin name	Type	Connection to IC Pin Name	Description
1	GND			Ground
2	GPIO_17	I/O	GPIO_17	Programmable GPIO Pin
3	GPIO_18	I/O	GPIO_18	Programmable GPIO Pin
4	GPIO_19	I/O	GPIO_19	Programmable GPIO Pin

No.	Pin name	Type	Connection to IC Pin Name	Description
5	WL_REG_ON	I	WL_REG_ON	Used by PMU to power up or power down the internal CYW54591 regulators used by the WLAN section. Also, when de-asserted, this pin holds the WLAN section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
6	BT_REG_ON	I	BT_REG_ON	Used by PMU to power up or power down the internal CYW54591 regulators used by the Bluetooth section. Also, when de-asserted, this pin holds the Bluetooth section in reset. This pin has an internal 200 kΩ pull-down resistor that is enabled by default. It can be disabled through programming.
7	GND			Ground
8	VDDIO	I	SYS_VDDIO WCC_VDDIO BT_VDDO VDDIO	IO supply
9	GND			Ground
10	GND			Ground
11	GND			Ground
12	BT_OUT			
13	GND			Ground
14	BT_IN			
15	GND			Ground
16	RF_SW_CTRL5	O	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
17	GND			Ground
18	GND			Ground
19	ANT_0			RF Port for WLAN (2.4GHz & 5GHz) and BT
20	GND			Ground
21	GND			Ground
22	BT_HOST_WAKE	O	BT_HOST_WAKE	Host wake-up: Signal from the module to the host indicating that the module requires attention.
23	BT_DEV_WAKE	I	BT_DEV_WAKE	Bluetooth device wake-up: Signal from the host to the module indicating that the host requires attention.
24	CLK_REQ	I/O	CLK_REQ	Reference clock request (shared by BT and WLAN). If not used, this can be no-connect.
25	LPO_IN	I	LPO_IN	External sleep clock input (32.768 kHz)
26	BT_I2S_DO	I/O	BT_I2S_DO	I^2S data output
27	BT_I2S_DI	I/O	BT_I2S_DI	I^2S data input
28	BT_I2S_CLK	I/O	BT_I2S_CLK	I^2S clock, can be master (output) or slave (input).
29	BT_I2S_WS	I/O	BT_I2S_WS	I^2S WS, can be master (output) or slave (input).
30	GND			Ground
31	RF_SW_CTRL11	O	RF_SW_CTRL11	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
32	GND			Ground
33	ANT_1			RF Port for WLAN (2.4 GHz & 5 GHz)
34	GND			Ground
35	GND			Ground
36	BT_UART_RTS_N	O	BT_UART_RTS_N	UART request-to-send. Active-low request-to-send signal for the HCI UART interface. BT LED control pin.
37	BT_UART_CTS_N	I	BT_UART_CTS_N	UART clear-to-send. Active-low clear-to-send signal for the HCI UART interface.
38	BT_UART_RXD	I	BT_UART_RXD	UART serial input. Serial data input for the HCI UART interface.

No.	Pin name	Type	Connection to IC Pin Name	Description
39	BT_UART_TXD	O	BT_UART_TXD	UART serial output. Serial data output for the HCI UART interface.
40	GPIO_5		GPIO_5	Programmable GPIO pins.
41	GPIO_4		GPIO_4	
42	GPIO_7		GPIO_7	
43	GPIO_6		GPIO_6	
44	PCIE_PME_L	OD	PCIE_PME_L	PCI power management event output. Used to request a change in the device.
45	PCIE_PERST_L	I	PCIE_PERST_L	PCIe System Reset. This input is the PCIe reset as defined in the PCIe base specification version 1.1. PCIE_PERST_L pad excludes internal pull-up.
46	PCIE_CLKREQ_L	OD	PCIE_CLKREQ_L	PCIe clock request signal which indicates when the REFCLK to the PCIe interface can be gated. **1** = the clock can be gated. **0** = the clock is required.
47	GND	-	-	Ground
48	PCIE_RDN	I	PCIE_RDN0	Receiver differential pair (x1 lane).
49	PCIE_RDP	I	PCIE_RDP0	Receiver differential pair (x1 lane).
50	GND	-	-	Ground
51	PCIE_REFCLKP	I	PCIE_REFCLKP	PCIE Differential Clock inputs (negative and positive). 100 MHz differential.
52	PCIE_REFCLKN	I	PCIE_REFCLKN	
53	GND	-	-	Ground
54	PCIE_TDN	O	PCIE_TDN0	Transmitter differential pair (×1 lane).
55	PCIE_TDP	O	PCIE_TDP0	
56	GND			Ground
57	VDDIO	I	VDDIO	IO supply
58	NC			No Connect
59	NC			No Connect
60	NC			No Connect
61	NC			No Connect
62	NC			No Connect
63	NC			No Connect
64	GND			Ground
65	VBAT		SR_VDDBAT5V LDO_VDDBAT5V	VBAT supply
66				
67-73	GND			Ground
74	BT_PCM_IN	I	BT_PCM_IN	PCM data input.
75	BT_PCM_OUT	O	BT_PCM_OUT	PCM data output.
76	BT_PCM_CLK	I/O	BT_PCM_CLK	PCM clock; can be master (output) or slave (input).
77	BT_PCM_SYNC	I/O	BT_PCM_SYNC	PCM sync; can be master (output) or slave (input).
78	GND	-	-	Ground
79	RF_SW_CTRL4	O	RF_SW_CTRL4	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
80	GND	-	-	Ground

No.	Pin name	Type	Connection to IC Pin Name	Description
81	RF_SW_CTRL12	O	RF_SW_CTRL12	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
82	BT_GPIO_5	I/O	BT_GPIO_5	Bluetooth general-purpose I/O.
83	BT_GPIO_4	I/O	BT_GPIO_4	
84	BT_GPIO_2	I/O	BT_GPIO_2	
85	BT_GPIO_3	I/O	BT_GPIO_3	
86	GPIO_3	I/O	GPIO_3	Programmable GPIO pins.
87	JTAG_SEL	I/O	JTAG_SEL	JTAG select pull high to select the JTAG interface. If the JTAG interface is not used this pin may be left floating or connected to ground.
88	GPIO_2	I/O	GPIO_2	Programmable GPIO pins.
89	GPIO_1	I/O	GPIO_1	
90	GPIO_0	I/O	GPIO_0	
91	GPIO_8	I/O	GPIO_8	
92	GPIO_9	I/O	GPIO_9	
93	GPIO_10	I/O	GPIO_10	
94	GPIO_11	I/O	GPIO_11	
95-104	GND			Ground

7 Absolute Maximum Ratings

The minimum and maximum ratings are shown in **Table 7.**

Table 7: Absolute Maximum Ratings

Parameter		Minimum	Maximum	Unit
Storage Temperature		-40	+85	°C
Supply Voltage	VBAT	-0.5	+6.0	V
	VDDIO	-0.5	+3.9	V

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability. No damage assuming only one parameter is set at limit at a time with all other parameters are set within operating condition.

8 Operating Conditions

The operating conditions are shown **Table 8**.

Table 8: Operating Conditions

Parameter		Minimum	Typical	Maximum	Unit
Operating Temperature Range		-40	25	85	°C
Specification Temperature		-10	25	70	°C
Operating Voltage	VBAT	3.0	3.3	4.8	V
	VDDIO	1.62	1.8 or 3.3	3.63	V

9 External LPO_IN Signal Requirements

The external LPO_IN signal requirements are shown in **Table 9**.

Table 9: External LPO_IN Signal Requirements

Parameter	External LPO_IN Clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-250	ppm
Duty cycle	30-70	%
Input signal amplitude	200 - 3300	mV, p-p
Signal type	Square-wave or sinewave	-
Input impedance[1]	> 100k	Ω
	< 5	pF
Clock jitter (during initial start-up)	<10,000	ppm

[1] When power is applied or switch off

10 I/O States

The following notations are used in I/O State Table.

- **I:** Input signal
- **O:** Output signal
- **I/O:** Input/Output signal
- **PU:** Pulled up
- **PD**: Pulled down
- **NoPull:** Neither pulled up nor pulled down
- Where applicable, the default value is shown in bold brackets (for example, [default value])

Table 10: IO State Table

Name	I/O	Keeper	Active Mode	Low Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset: Before SW Download (BT_REG_ON High. WL_REG_ON High)	Power-down (WL_REG_ON High and BT_REG_ON=0) and VDDIOs Are Present	Power Rail
WL_REG_ON BT_REG_ON	I	N	I: PD Pull-down can be disabled	I: PD Pull-down can be disabled	I: PD (of 200K)	I: PD (of 200K)	I: PD (of 200K)	
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	I: PD	I: PD	VDDIO
GPIO_1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPullb	I: NoPull	VDDIO
GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO

Name	I/O	Keeper	Active Mode	Low Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset: Before SW Download (BT_REG_ON High. WL_REG_ON High)	Power-down (WL_REG_ON High and BT_REG_ON=0) and VDDIOs Are Present	Power Rail
GPIO_8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_9	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [NoPull]	I: PU	I: PU	I:PU	VDDIO
GPIO_10	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_11	I/O	Y	I/O: PU, PD, NoPull Programmable [PU]	I/O: PU, PD, NoPull Programmable [PU]	I: PU	I: PU	I:PU	VDDIO
GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_18	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
GPIO_19	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull	I: NoPull	VDDIO
RF_SW_CTRL_X	O	N	O: No Pull	O: No Pull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RF
CLK_REQ	O	Y	Open drain or push-pull (programmable) Active high.	Open drain or push-pull (programmable).Active high.	High-Z, NoPull	Open drain. Active high	Open drain. Active high	BT_VDDO
BT_HOST_WAKE	O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PD	BT_VDDO
BT_DEV_WAKE	I	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_GPIO_2 BT_GPIO_3	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_GPIO_4 BT_GPIO_5	I/O	Y	Input/Output; PU, PD, NoPull (programmable)	Input/Output; PU, PD, NoPull (programmable)	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO

Name	I/O	Keeper	Active Mode	Low Power State/Sleep (All Power Present)	Power-down (BT_REG_ON and WL_REG_ON Held Low)	Out-of-Reset: Before SW Download (BT_REG_ON High. WL_REG_ON High)	Power-down (WL_REG_ON High and BT_REG_ON=0) and VDDIOs Are Present	Power Rail
BT_UART_CTS_N	I	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_RTS_N	O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_RXD	I	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_UART_TXD	O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PU	Input, PU	BT_VDDO
BT_PCM_CLK	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_IN	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_OUT	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_PCM_SYNC	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I²S_CLK	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	BT_VDDO
BT_I²S_DO	I/O	Y	Output, NoPull	Output, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I²S_DI	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	Input, PD	Input, PD	BT_VDDO
BT_I²S_WS	I/O	Y	Input, NoPull	Input, NoPull	High-Z, NoPull	High-Z, NoPull	High-Z, NoPull	BT_VDDO

11 Power Sequences

This section describes the Power-On and Power-Off Sequences along with their parameters.

11.1 Power-On Sequence

For this sequence:

- VBAT and VDDIO should not rise 10%-90% faster than 40 microseconds.
- VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present fast or be held high before VBAT is high.
- WL_REG_ON and BT_REG_ON should be up after sleep clock oscillation is stabilized.
- Please proceed reset by WL_REG_ON and BT_REG_ON until it starts normally if it doesn't wake from sleep properly, or it is presented with uncertain status.
- Please keep repeats power off sequence and power on sequence several times until it started normally.
- The CYW54591 has an internal Power-On reset (POR) circuit. The device will be held in reset for a maximum of 110 ms after internal regulators and VDDIO have passed the POR threshold. Wait at least 150 ms after WL_REG_ON is driven high before initiating PCIe accesses.

Figure 6 shows the power-on sequence for WLAN On and BT ON.

Figure 6: Power-On Sequence for WLAN ON and BT ON

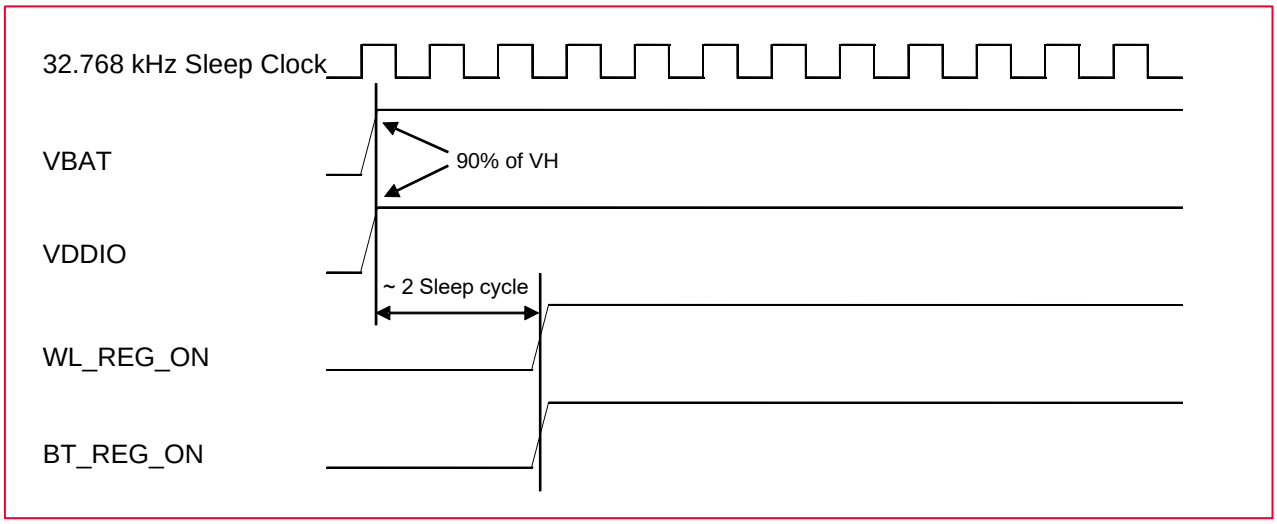


Figure 7 shows the power-on sequence for WLAN OFF and BT OFF.

Figure 7: Power-On Sequence for WLAN OFF and BT OFF

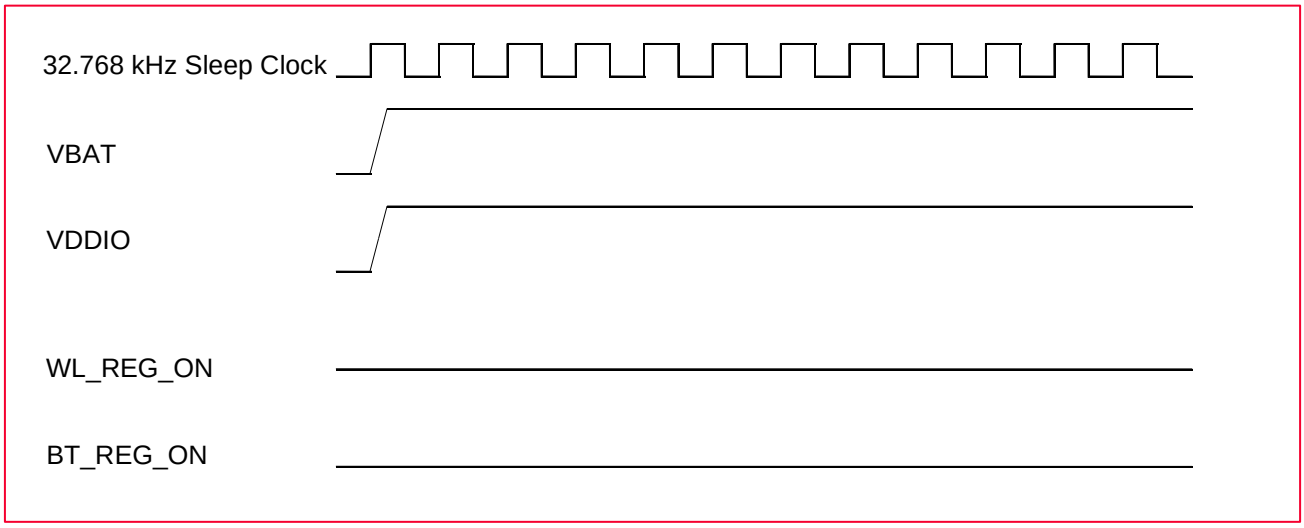


Figure 8 shows the power-on sequence for WLAN ON and BT OFF.

Figure 8: Power-On Sequence for WLAN ON and BT OFF

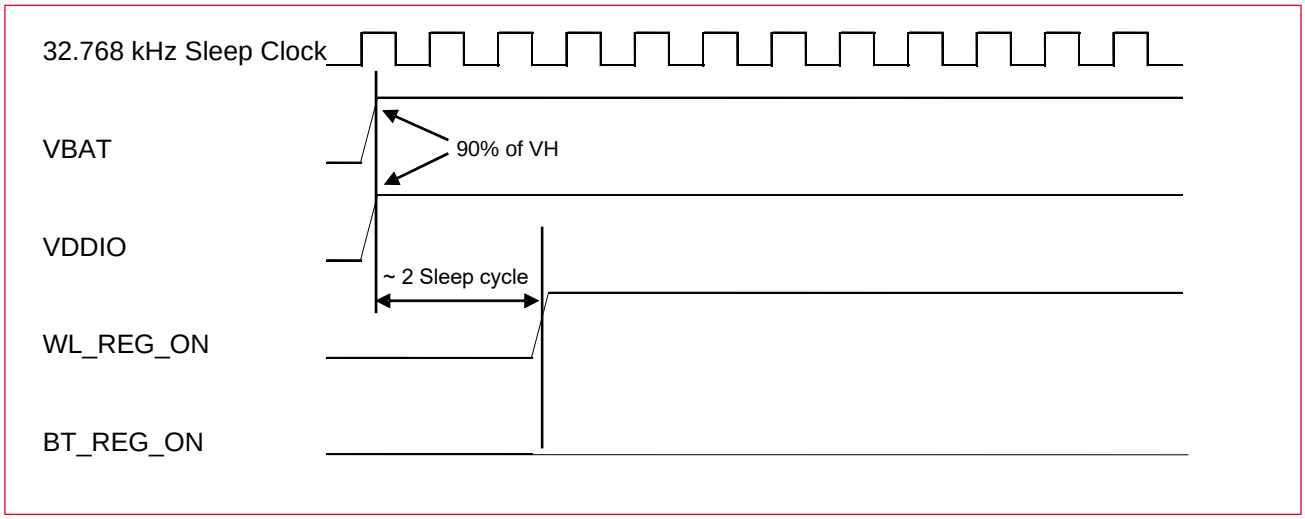
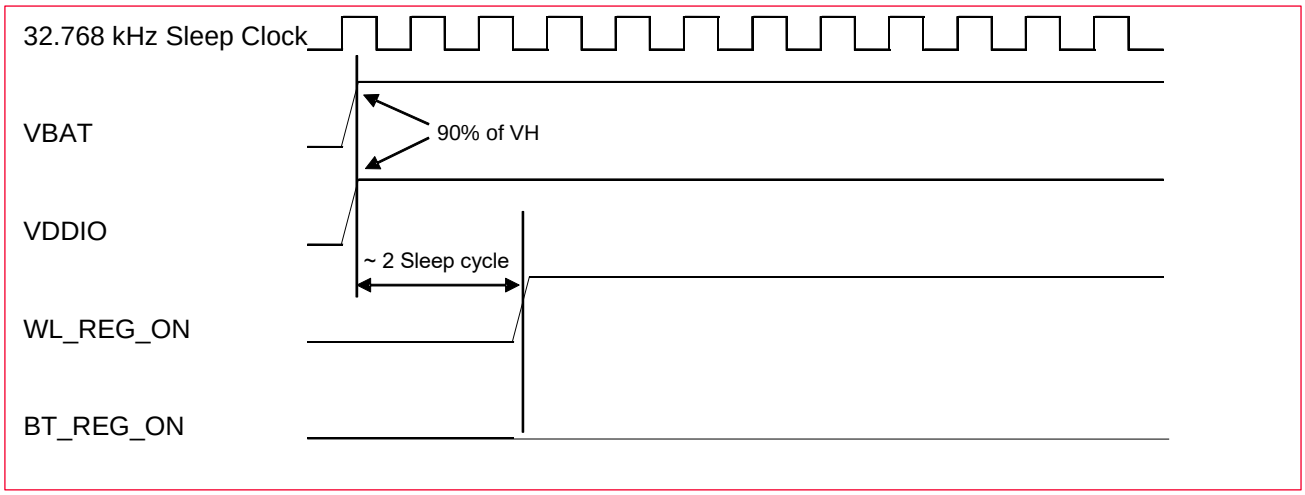


Figure 9 shows the power-on sequence for WLAN OFF and BT ON.

Figure 9: Power-On Sequence for WLAN OFF and BT ON



11.2 Power-Off Sequence

For power-off sequence:

- VDDIO should be down before or at the same time as VBAT. VBAT should NOT be down earlier than VDDIO low. VDDIO becomes low state is prior to VBAT low.
- VBAT and VDDIO should be down after WL_REG_ON and BT_REG_ON are low. Waiting time from REG_ON down to power supply off is not prescribed.

Figure 10 shows the power-off sequence for WLAN ON and BT ON.

Figure 10: Power-Off Sequence for WLAN ON and BT ON

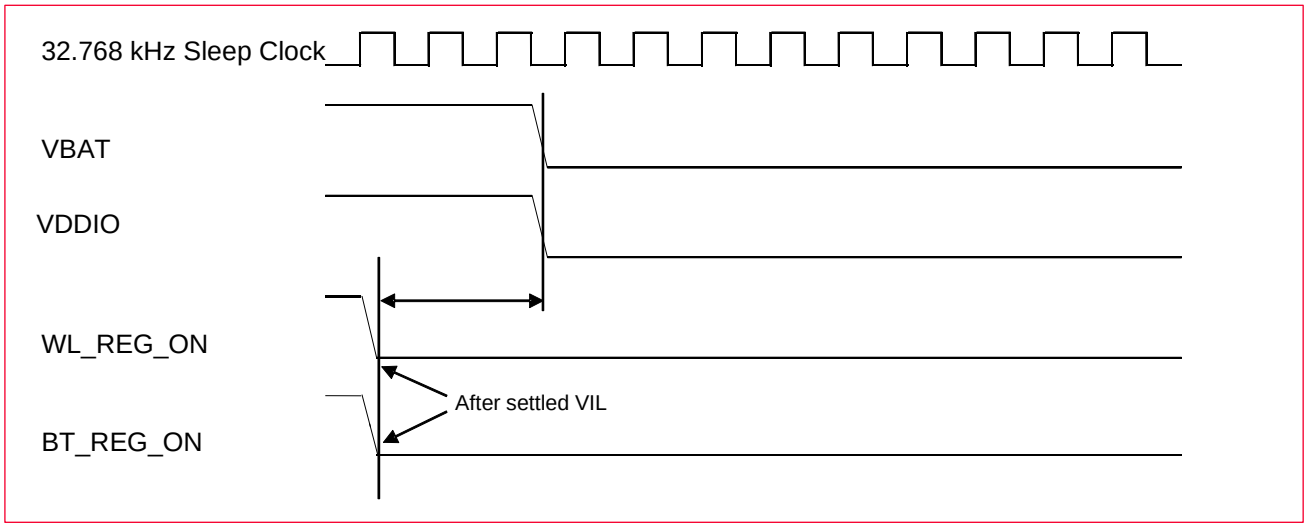


Figure 11 shows the power-off sequence for WLAN OFF and BT OFF.

Figure 11: Power-Off Sequence for WLAN OFF and BT OFF

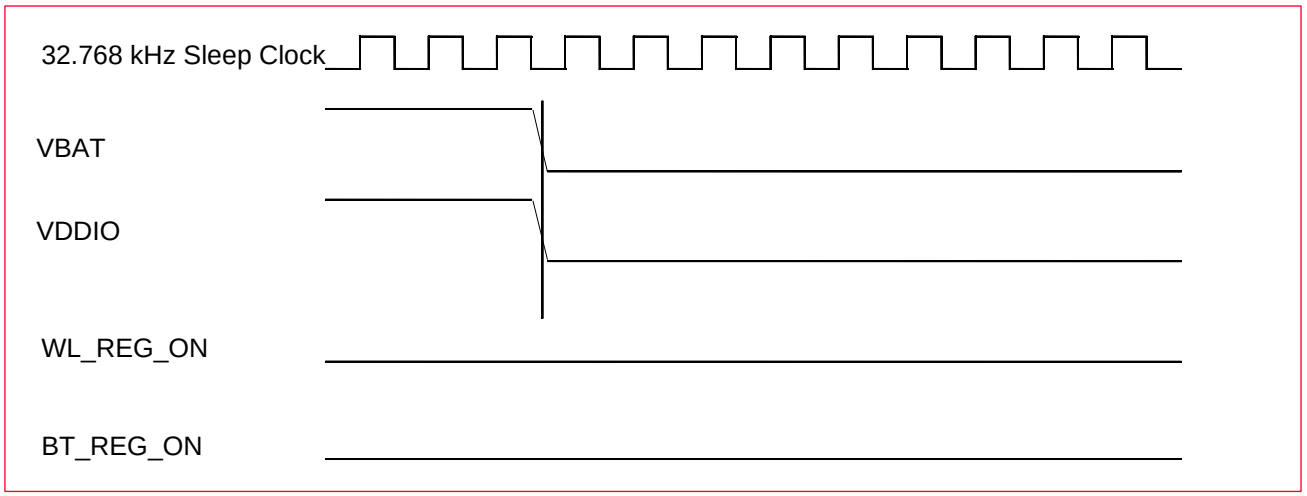


Figure 12 shows the power-off sequence for WLAN ON and BT OFF.

Figure 12: Power-Off Sequence for WLAN ON and BT OFF

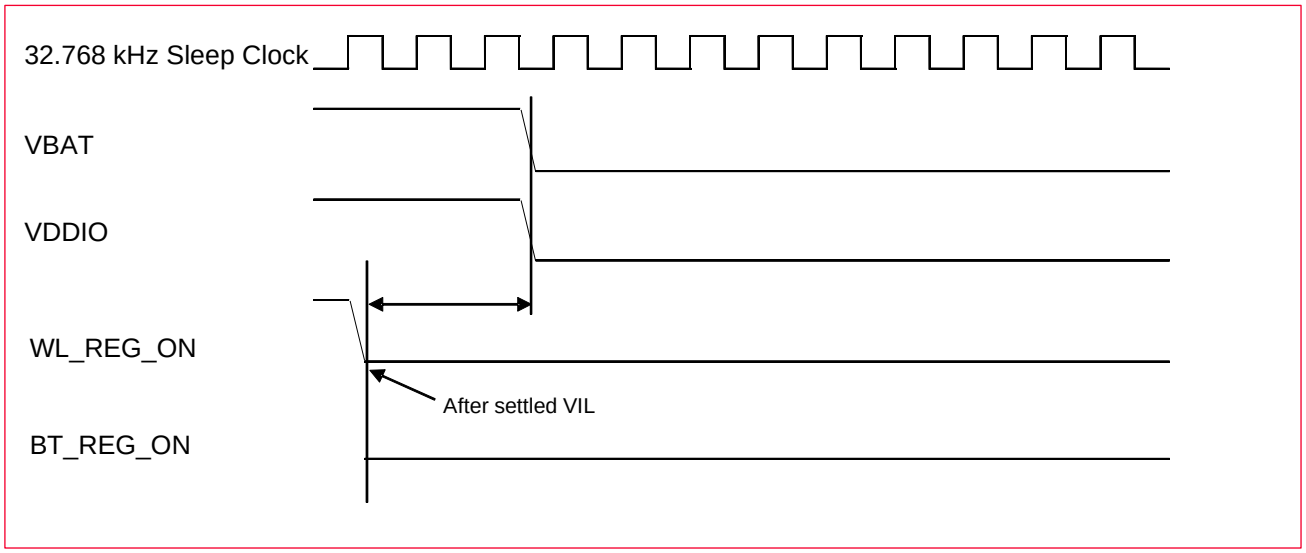
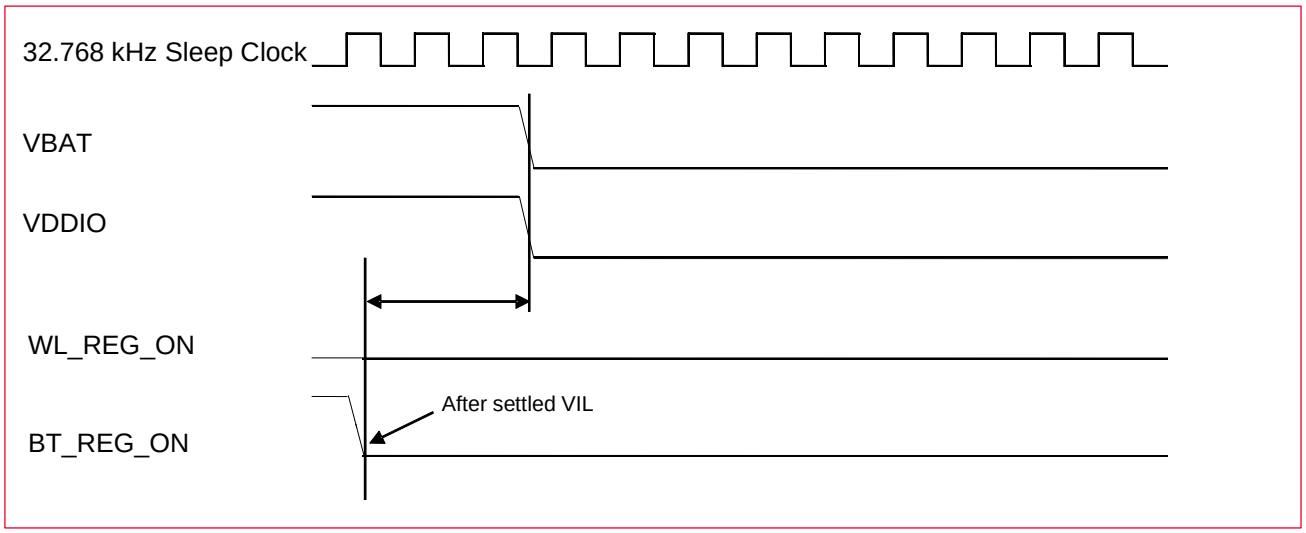


Figure 13 shows the power-off sequence for WLAN OFF and BT ON.

Figure 13: Power-Off Sequence for WLAN OFF and BT ON



12 Interface Timing and AC Characteristics

This section has sequence diagrams for Bluetooth UART timing, Bluetooth startup signaling sequence, Bluetooth PCM interface timing and Bluetooth I²S interface timing.

12.1 Bluetooth UART Timing

Bluetooth UART timing diagram and parameters are shown in **Figure 14** and **Table 11**.

Figure 14: UART Timing Diagram

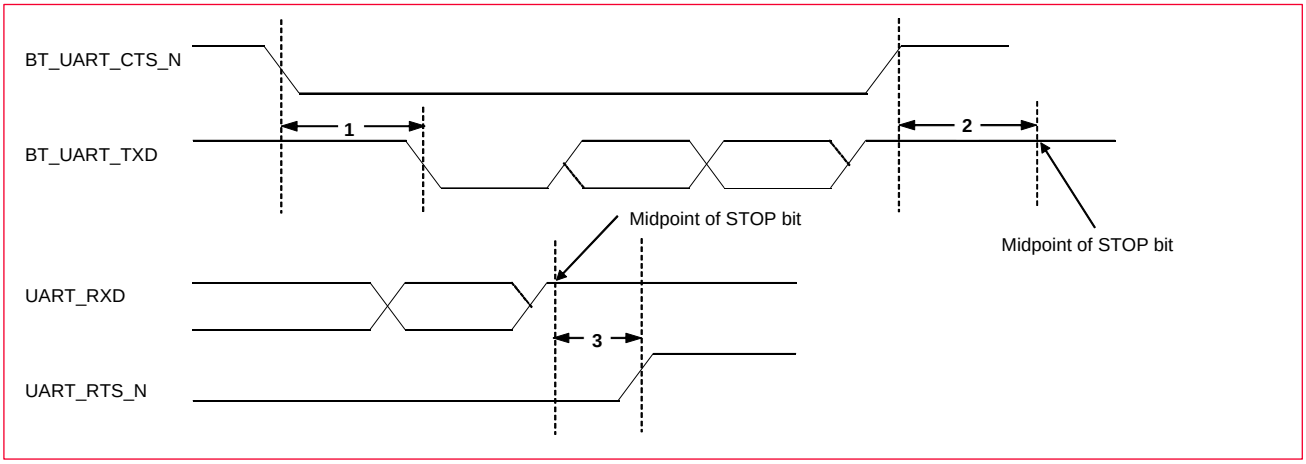


Table 11: UART Timing Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid			1.5	Bit periods
2	Setup time, UART_CTS_N high before midpoint of stop bit			0.5	Bit periods
3	Delay time, midpoint of stop bit to UART_RTS_N high			0.5	Bit periods

12.2 Bluetooth Startup Signaling Sequence

Bluetooth startup signaling sequence graph and its parameters is shown in **Figure 15** and **Table 12**.

Figure 15: Bluetooth Startup Signaling Sequence Graph

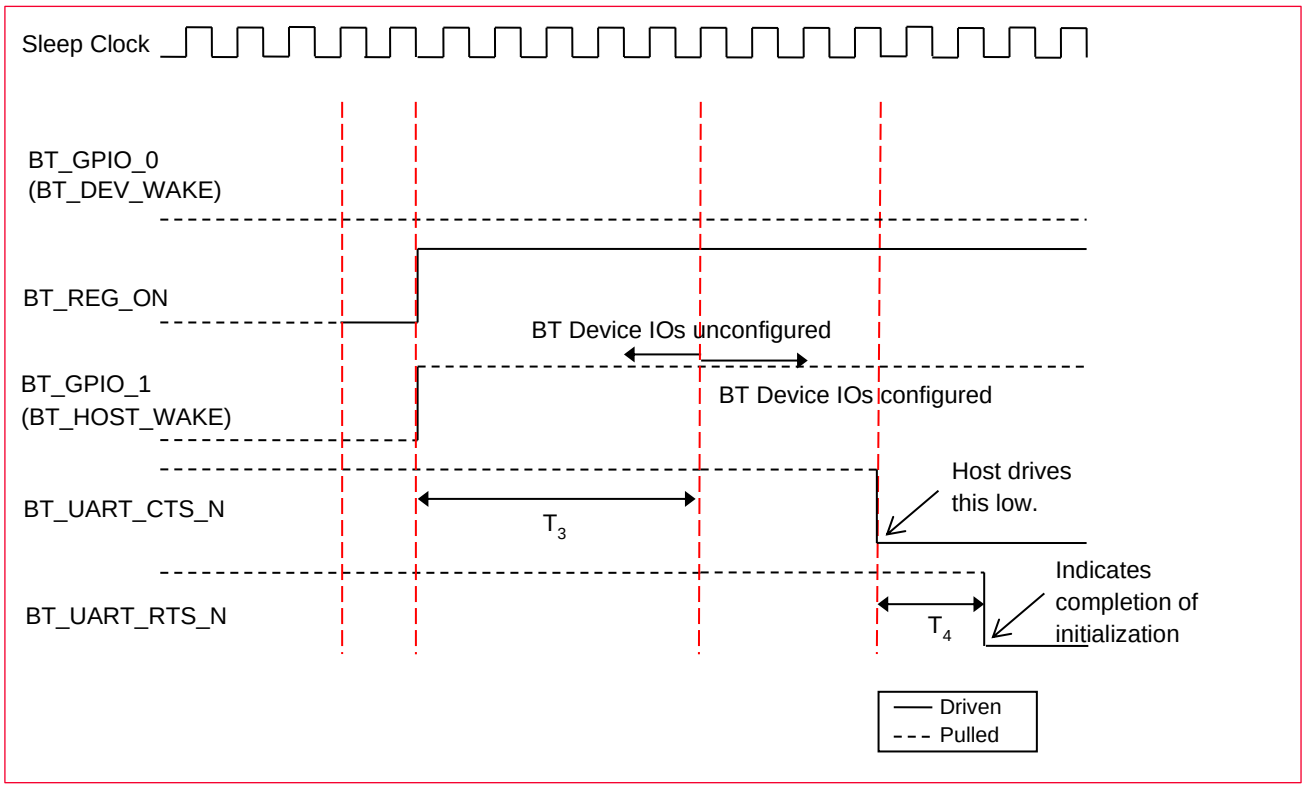


Table 12: Bluetooth Startup Signaling Sequence Parameters

Reference	Description	Minimum	Typical	Maximum	Unit
T_3	Time for the BT device to settle its IOs after BT_REG_ON is asserted.			40.0	ms
T_4	Time for the BT device to drive UART_RTS_N low after the host drives UART_CTS_N low			10.0	ms

12.3 Bluetooth PCM Timing

This section describes data formatting, wideband speech support, and various sync modes.

12.3.1 Data Formatting

The IC used in the module may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the IC uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sigh bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

12.3.2 Wideband Speech Support

When the host encodes wideband speech (WBS) packets in transparent mode, the encoded packets are transferred over the PCM bus for an eSCO voice connection. In this mode, the PCM bus is typically configured in master mode for a 4 kHz sync rate with 16-bit samples, resulting in a 64-kbps bit rate. The IC also supports slave transparent mode using a proprietary rate-matching scheme. IN SBC-code mode, linear 16-bit data at 16 kHz (256 kbps rate) is transferred over the PCM bus.

12.3.3 Short Frame Sync (Master Mode)

Figure 16 and **Table 13** show the short frame sync signal and its parameters in master mode.

Figure 16: Short Frame Sync Signal - Master Mode

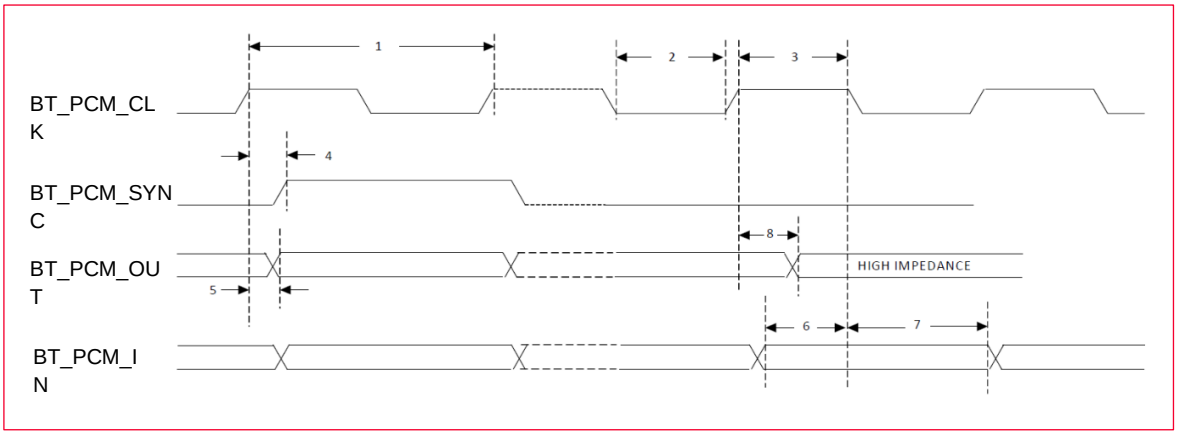


Table 13: Short Frame Sync Signal Parameters - Master Mode

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC delay	0		25.0	ns
5	PCM_OUT delay	0		25.0	ns
6	PCM_IN setup	8			ns
7	PCM_IN hold	8			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0		25.0	ns

12.3.4 Short Frame Sync (Slave Mode)

Figure 17 and **Table 14** show the short frame sync signal and its parameters in slave mode.

Figure 17: Short Frame Sync Signal - Slave Mode

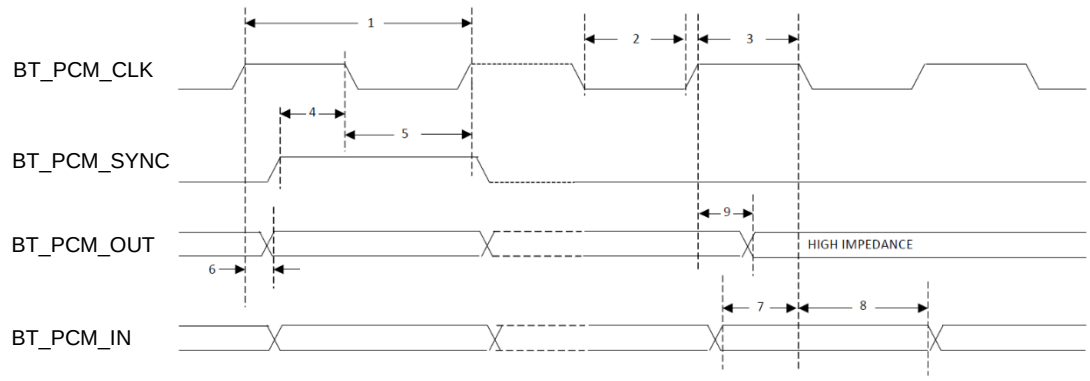


Table 14: Short Frame Sync Signal Parameters - Slave Mode

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC setup	8.0			ns
5	PCM_SYNC hold	8.0			ns
6	PCM_OUT delay	0		25.0	ns
7	PCM_IN setup	8.0			ns
8	PCM_IN hold	8.0			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0		25.0	ns

12.3.5 Long Frame Sync (Master Mode)

Figure 18 and **Table 15** show the long frame sync signal and its parameters in master mode.

Figure 18: Long Frame Sync Signal - Master Mode

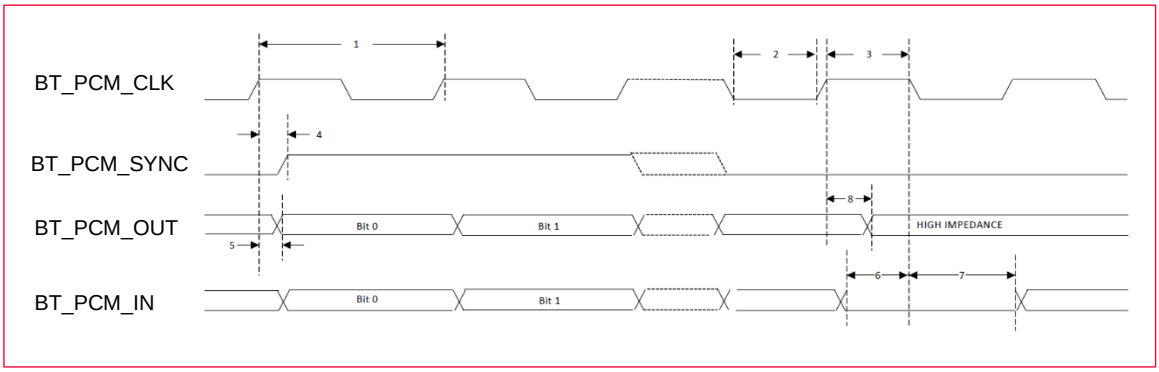


Table 15: Long Frame Sync Signal Parameters - Master Mode

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC delay	0		25.0	ns
5	PCM_ OUT delay	0		25.0	ns
6	PCM_IN setup	8.0			ns
7	PCM_IN hold	8.0			ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0		25.0	ns

12.3.6 Long Frame Sync (Slave Mode)

Figure 19 and **Table 16** show the long frame sync signal and its parameters in slave mode data.

Figure 19: Long Frame Sync Signal - Slave Mode

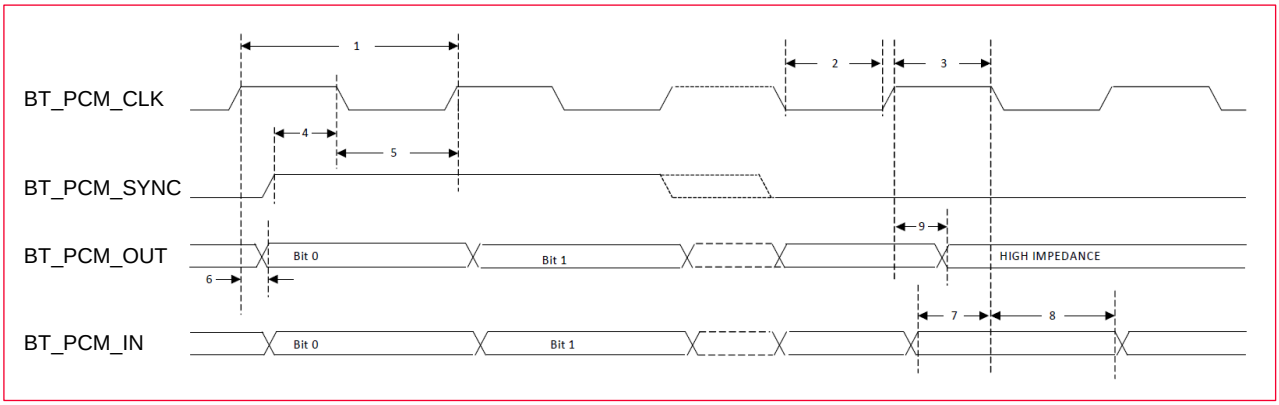


Table 16: Long Frame Sync Signal Parameters - Slave Mode

Reference	Description	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency			12.0	MHz
2	PCM bit clock High	41.0			ns
3	PCM bit clock Low	41.0			ns
4	PCM_SYNC Setup	8.0			ns
5	PCM_SYNC hold	8.0			ns
6	PCM_OUT delay	0		25.0	ns
7	PCM_IN Setup	8.0			ns
8	PCM_IN Hold	8.0			ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance.	0		25.0	ns

12.4 Bluetooth I²S Interface Timing

The IC used in the module supports I2S format. The module supports only PCM digital audio ports through I²S format.

The I2S signals are:

- I²S clock: I²S SCK (Module pin: BT_PCM_CLK)
- I²S Word Select: I²S WS (Module pin: BT_PCM_SYNC)
- I²S Data Out: I²S SDO (Module pin: BT_PCM_OUT)
- I²S Data In: I²S SDI (Module pin: BT_PCM_IN)

I²S SCK and I²S WS become outputs in master mode and inputs in slave mode, while I²S SDO always stays as an output. The channel word length is 16 bits, and the data is justified so that the MSB of the let-channel data is aligned with the MSB of the I²S bus, per the I²S specification. The MSB of each data word is transmitted one bit clock cycle after the I²S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I²S WS is low, and right-channel data is transmitted when I²S WS is high. Data bits sent by the CYW89335 are synchronized with the falling edge of I²S_SCK and should be sampled by the receiver on the rising edge of I²S_SCK.

The clock rate in master mode is either of the following:

- 48 kHz x 32 bits per frame = 1.536 MHz
- 48 kHz x 50 bits per frame = 2.400 MHz

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz

Table 17: Timing for I²S Transmitters and Receivers

	Transmitter				Receiver				Notes
	Lower Limit		Upper Limit		Lower Limit		Upper Limit		
	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
Clock Period T	T_{tr}				T_r				a
Master Mode: Clock generated by transmitter or receiver									
$HIGHt_{HC}$	$0.35T_{tr}$				$0.35T_{tr}$				b
LOW t_{LC}	$0.35T_{tr}$				$0.35T_{tr}$				b
Slave Mode: Clock accepted by transmitter or receiver									
HIGH t_{HC}		$0.35T_{tr}$				$0.35T_{tr}$			c
LOW t_{LC}		$0.35T_{tr}$				$0.35T_{tr}$			c
Rise time t_{RC}			$0.15T_{tr}$						d
Transmitter									
Delay t_{dtr}				0.8T					e
Hold time t_{htr}	0								d
Receiver									
Setup time t_{sr}						0.2Tr			f
Hold time t_{hr}						0			f

a) The system clock period T must be greater than T_{tr} and T_r because both the transmitter and receiver have to be able to handle the data transfer rate.

b) At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason, t_{HC} and t_{LC} specified with respect to T.

c) In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than $0.35T_{tr}$ any clock that meets the requirements can be used.

d) Because the delay(t_{dtr}) and the maximum transmitter speed (defined by T_{tr}) are related, a fast transmitter driven by a slow clock edge can result in t_{dtr} not exceeding t_{RC} which means thtr becomes zero or negative. Therefore, the transmitter has guarantee that thtr is greater than or equal to zero, so long as the clock rise-time t_{RC} is not more than t_{RC} where t_{RCmax} is not less than $0.15T_{tr}$.

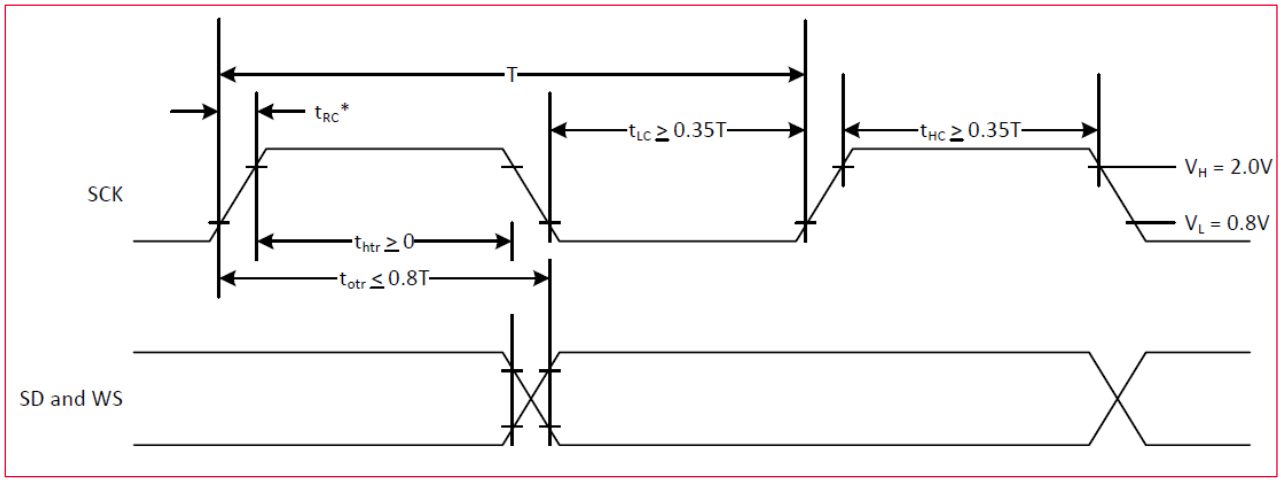
e) To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.

f) The data setup and hold time must not be less than the specified receiver setup and hold time.

The time periods specified in below figures are defined by the transmitter speed. The receiver specifications must match transmitter performance.

Figure 20 shows the I²S transmitters timing sequence.

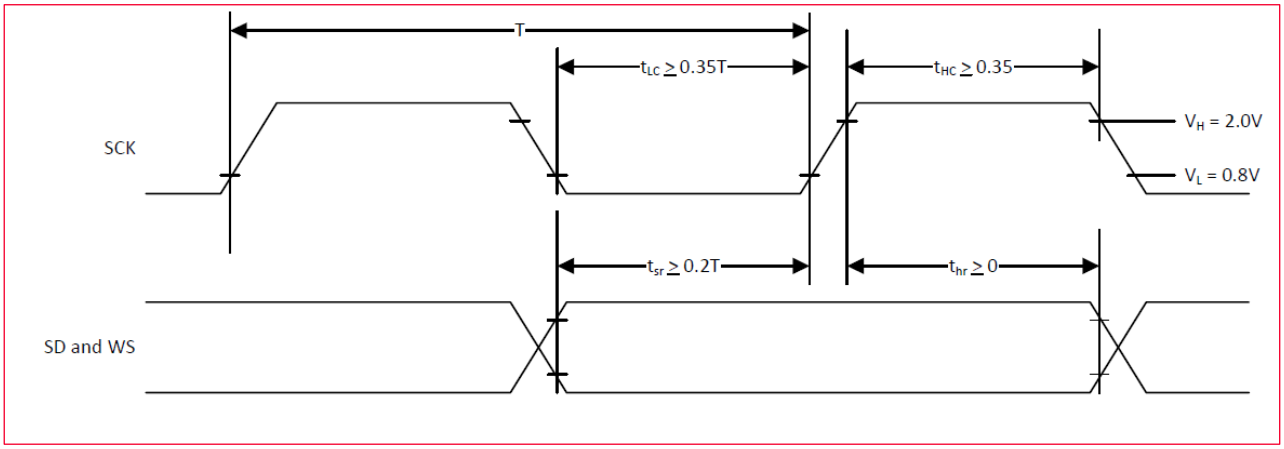
Figure 20: I²S Transmitters Timing Sequence



- T = Clock period
- T_{tr} = Minimum allowed clock period for transmitter
- $T = T_{tr}$
- t_{RC} is only relevant for transmitters in slave mode.

Figure 21 shows the I²S receivers timing sequence.

Figure 21: I²S Receivers Timing Sequence



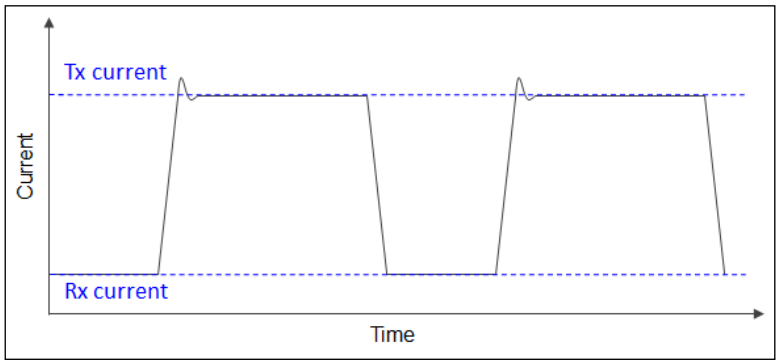
- T = Clock period
- T_r = Minimum allowed clock period for transmitter
- $T > T_r$

13 DC/RF Characteristics

This section describes the electrical characteristics of the Type 1XA module.

Burst current definition is shown in **Figure 22**.

Figure 22: Burst Current Definition



13.1 DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, 11 Mbps mode unless otherwise specified.

Table 18: DC/RF Characteristics for IEEE 802.11b - 2.4 GHz

Items	Contents			
Specification	IEEE 802.11b - 2.4 GHz			
Mode	DSSS / CCK			
Channel Frequency	2412 to 2472 MHz (5 MHz)			
Data Rate	1, 2, 5.5,11 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		370	470	mA
• Rx mode		100	150	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	14.5	17	19.5	dBm
Spectrum Mask Margin				
• 1st side lobes (-30 dBr)	0			dB
• 2nd side lobes (-50 dBr)	0			dB
Power-on/off ramp			2.0	µs
RF Carrier Suppression	15			dB
Modulation Accuracy			35	%
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW =100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (FER ≤ 8%)			-76	dBm
Maximum Input Level (FER ≤ 8%)	-10			dBm
Adjacent Channel Rejection (FER ≤ 8%)	35			dB

13.2 DC/RF Characteristics for IEEE 802.11g - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, VDDIO = 3.3V, 54 Mbps mode unless otherwise specified.

Table 19: DC/RF Characteristics for IEEE 802.11g - 2.4 GHz

Items	Contents			
Specification	IEEE 802.11g - 2.4 GHz			
Mode	OFDM			
Channel Frequency	2412 to 2472 MHz (5 MHz)			
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		330	430	mA
• Rx mode		100	150	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	12.5	15	17.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 -74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 8 7.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-65	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-1			dB

13.3 DC/RF Characteristics for IEEE 802.11n - 2.4 GHz

Conditions: 25 °C, VBAT = 3.3V, 65 Mbps (MCS7 – HT 20 MHz) mode unless otherwise specified.

Table 20: DC/RF Characteristics for IEEE 802.11n - 2.4 GHz

Items	Contents			
Specification	IEEE 802.11n - 2.4 GHz			
Mode	OFDM			
Channel Frequency	2412 to 2472 MHz (5 MHz)			
Data Rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		330	430	mA
• Rx mode		100	150	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	12.5	15	17.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (Measured at enhanced mode)			-27	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 -74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 8 7.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER ≤ 10%)	-20			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-2			dB

13.4 DC/RF Characteristics for IEEE 802.11a - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, 54 Mbps mode unless otherwise specified.

Table 21: DC/RF Characteristics for IEEE 802.11a - 5 GHz

Items	Contents			
Specification	IEEE 802.11a - 5 GHz			
Mode	OFDM			
Channel Frequency	5180 to 5825 MHz			
Data Rate	6, 9, 12, 18, 24, 36, 48, 54 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		400	500	mA
• Rx mode		120	170	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	11.5	14	16.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -40 dBr)	0			dB
• 30 MHz to 33 MHz (-40 dBr)	0			dB
Constellation Error			-25	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-65	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-1			dB

13.5 DC/RF Characteristics for IEEE 802.11n (HT20) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, 65 Mbps (MCS7 - HT 20 MHz) mode unless otherwise specified.

Table 22: DC/RF Characteristics for IEEE 802.11n (HT20) - 5 GHz

Items	Contents			
Specification	IEEE 802.11n - 5 GHz			
Mode	OFDM			
Channel Frequency	5180 to 5825 MHz			
Data Rate	6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		380	480	mA
• Rx mode		120	170	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	10.5	13	15.5	dBm
Spectrum Mask Margin				
• 9 MHz to 11 MHz (0 ~ -20 dBr)	0			dB
• 11 MHz to 20 MHz (-20 ~ -28 dBr)	0			dB
• 20 MHz to 30 MHz (-28 ~ -45 dBr)	0			dB
• 30 MHz to 33 MHz (-45 dBr)	0			dB
Constellation Error (Measured at enhanced mode)			-27	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-64	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	16			dB

13.6 DC/RF Characteristics for IEEE 802.11n (HT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, 135 Mbps (MCS7 - HT 40 MHz) mode unless otherwise specified.

Table 23: DC/RF Characteristics for IEEE 802.11n (HT40) - 5 GHz

Items	Contents			
Specification	IEEE 802.11n - 5 GHz			
Mode	OFDM			
Channel Frequency	5180 to 5825 MHz			
Data Rate	13.5,27,40.5,54,81,108,121.5,135 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		410	510	mA
• Rx mode		140	190	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	9.5	12	14.5	dBm
Spectrum Mask Margin				
• 19 MHz to 21 MHz (0 ~ -20 dBr)	0			dB
• 21 MHz to 40 MHz (-20 ~ -28 dBr)	0			dB
• 40 MHz to 60 MHz (-28 ~ -45 dBr)	0			dB
• 60 MHz to 80 MHz (-45 dBr)	0			dB
Constellation Error (Measured at enhanced mode)			-27	dB
Frequency tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW =1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-61	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-2			dB

13.7 DC/RF Characteristics for IEEE 802.11ac (HT40) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, 180 Mbps (MCS9 - HT 40 MHz) mode unless otherwise specified.

Table 24: DC/RF Characteristics for IEEE 802.11ac (HT40) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ac - 5 GHz			
Mode	OFDM			
Channel Frequency	5190 to 5795 MHz			
Data Rate	13.5, 27, 40.5, 54, 81, 108, 121.5, 135, 162, 180 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		420	520	mA
• Rx mode		140	200	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	7.5	10	12.5	dBm
Spectrum Mask Margin				
• 19 MHz to 21 MHz (0 ~ -20 dBr)	0			dB
• 21 MHz to 40 MHz (-20 ~ -28 dBr)	0			dB
• 40 MHz to 60 MHz (-28 ~ -40 dBr)	0			dB
• 60 MHz to 80 MHz (-40 dBr)	0			dB
Constellation Error (Measured at enhanced mode)			-32	dB
Frequency Tolerance	-20		20	ppm
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-54	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER ≤ 10%)	-9			dB

13.8 DC/RF Characteristics for IEEE 802.11ac (HT80) - 5 GHz

Conditions: 25 °C, VBAT = 3.3V, 390 Mbps (MCS9 - HT 80 MHz) mode unless otherwise specified.

Table 25: DC/RF Characteristics for IEEE 802.11ac (HT80) - 5 GHz

Items	Contents			
Specification	IEEE 802.11ac - 5 GHz			
Mode	OFDM			
Channel Frequency	5210 to 5775 MHz			
Data Rate	29.3, 58.5, 87.8,117,175.5,234,263.3,292.5,351,390 Mbps			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		440	540	mA
• Rx mode		180	250	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Power Levels	7.5	10	12.5	dBm
Spectrum Mask				
• 39 MHz to 41 MHz (0 ~ -20 dBr)	0			dB
• 41 MHz to 80 MHz (-20 ~ -28 dBr)	0			dB
• 80 MHz to 120 MHz (-28 ~ -40 dBr)	0			dB
• 120 MHz to 140 MHz (-40 dBr)	0			dB
Constellation Error (Measured at enhanced mode)			-32	dB
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 5150 MHz (BW = 1 MHz)			-30	dBm
• 5350 - 5470 MHz (BW = 1 MHz)			-30	dBm
• 5725 - 26000 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Minimum Input Level (PER ≤ 10%)			-51	dBm
Maximum Input Level (PER ≤ 10%)	-30			dBm
Adjacent Channel Rejection (PER < 10%)	-9			dB

13.9 DC/RF Characteristics for Bluetooth

Conditions: 25 °C, VBAT = 3.3V

Table 26: DC/RF Characteristics - Bluetooth

Items	Contents			
Bluetooth Specification (power class)	Version 5.2 (Class 2)			
Channel Frequency (spacing)	2402 to 2480 MHz (1 MHz)			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• DH5 Packet 50% Rx/Tx Slot Duty Cycle		50	65	mA
• 2DH5 Packet 50% Rx/Tx Slot Duty Cycle		40	55	mA
• 3DH5 Packet 50% Rx/Tx Slot Duty Cycle		40	45	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Output Power (at DH5)	7.5	11	14.5	dBm
Output Power (at 2DH5, 3DH5)	3.5	7	10.5	dBm
Frequency Range	2400		2483.5	MHz
20 dB bandwidth			1	MHz
Adjacent Channel Power[2]				
• [M-N] = 2			-20	dBm
• [M-N] ≥ 3			-40	dBm
Modulation Characteristics				
• Modulation $\Delta f1_{avg}$	140		175	kHz
• Modulation $\Delta f2_{max}$	115			kHz
• Modulation $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier Frequency Drift				
• 1slot	-25		+25	kHz
• 3slot / 5slot	-40		+40	kHz
• Maximum Drift Rate	-20		+20	kHz/50µs
EDR Relative Power	-4		+1	dB
EDR Carrier Frequency Stability and Modulation Accuracy				
• Ωi	-75		+75	kHz
• ωi+ωo	-75		+75	kHz
• ωo	-10		+10	kHz
• RMS DEVM (DQPSK)			20	%
• Peak DEVM (DQPSK)			35	%
• 99% DEVM (DQPSK)			30	%
• RMS DEVM (8DPSK)			13	%
• Peak DEVM (8DPSK)			25	%
• 99% DEVM (8DPSK)			20	%
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm

[2] Up to three spurious responses within Bluetooth limits are allowed.

Items	Contents			
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
BR (DFSK) Sensitivity (BER < 0.1%)			-80	dBm
Maximum Input Level (BER < 0.1%)	-20			dBm
EDR (8DPSK) Sensitivity (BER ≤ 0.007%)			-70	dBm

13.10 DC/RF Characteristics for Bluetooth Low Energy

Conditions: 25 °C, VBAT = 3.3V, 1Mbps

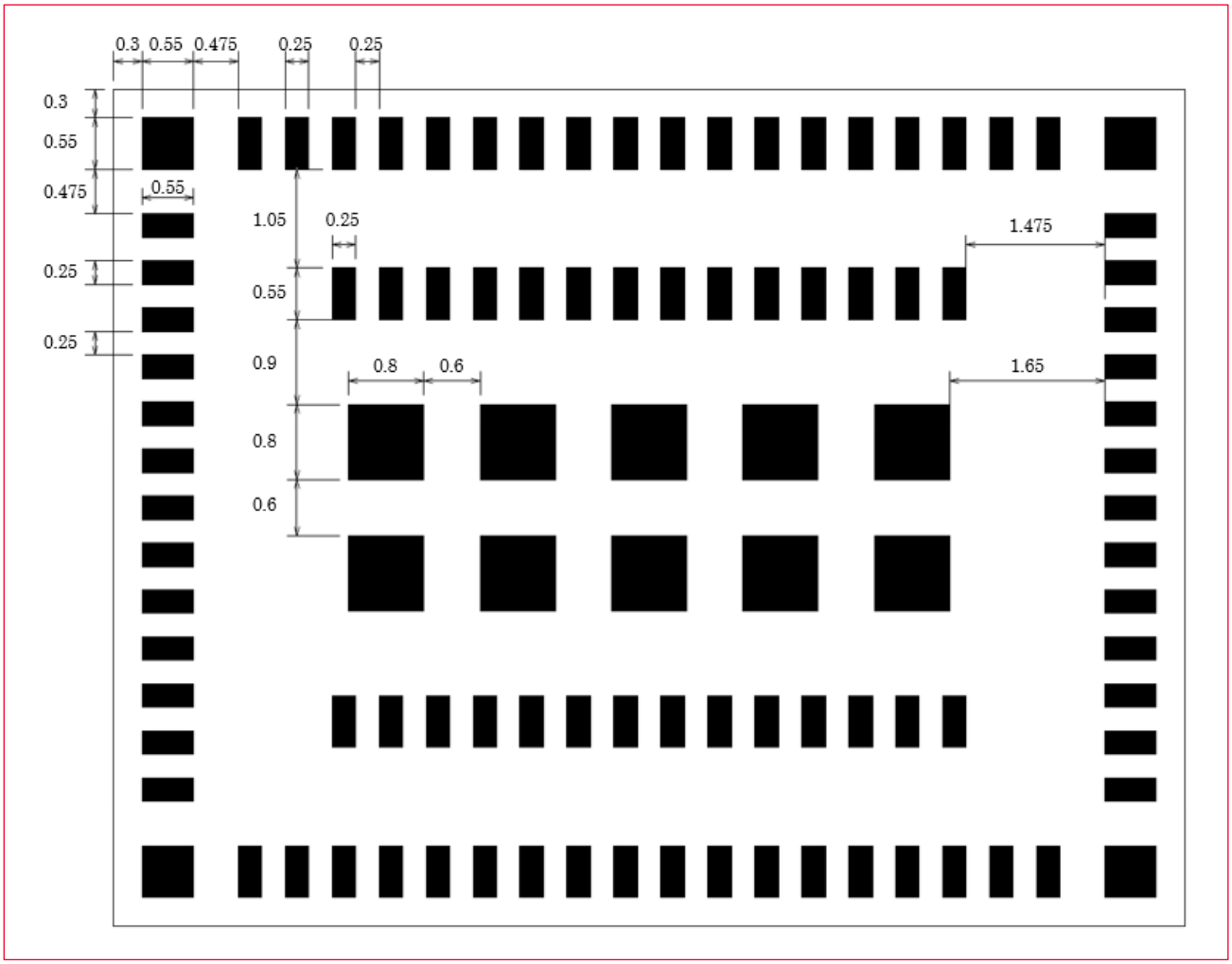
Table 27: DC/RF Characteristics - BLE

Items	Contents			
Bluetooth Specification (power class)	Version 5.2(LE)			
Channel Frequency (spacing)	2402 to 2480 MHz (2 MHz)			
Number of RF Channel	40			
Current Consumption	**Minimum**	**Typical**	**Maximum**	**Unit**
• Tx mode		30	45	mA
• Rx mode		15	25	mA
Transmitter	**Minimum**	**Typical**	**Maximum**	**Unit**
Center Frequency	2402		2480	MHz
Channel Spacing		2		MHz
Number of RF channel		40		
Output Power	0	3	7.5	dBm
In-band emission				
• f_{TX} +/-2 MHz			-20	dBm
• f_{TX} +/-[3+n] MHz; n = 0,1,2…			-30	dBm
Modulation Characteristics				
• $\Delta f1_{avg}$	225		275	kHz
• $\Delta f2_{max}$ (at 99.9%)	185			kHz
• $\Delta f2_{avg}$ / $\Delta f1_{avg}$	0.8			
Carrier Frequency Offset and Drift				
• Frequency Offset			150	kHz
• Frequency Drift			50	kHz
• Drift Rate			20	kHz
Spurious Emissions				
• 30 - 47 MHz (BW = 100 kHz)			-36	dBm
• 47 - 74 MHz (BW = 100 kHz)			-54	dBm
• 74 - 87.5 MHz (BW = 100 kHz)			-36	dBm
• 87.5 - 118 MHz (BW = 100 kHz)			-54	dBm
• 118 - 174 MHz (BW = 100 kHz)			-36	dBm
• 174 - 230 MHz (BW = 100 kHz)			-54	dBm
• 230 - 470 MHz (BW = 100 kHz)			-36	dBm
• 470 - 862 MHz (BW = 100 kHz)			-54	dBm
• 862 - 1000 MHz (BW = 100 kHz)			-36	dBm
• 1000 - 12750 MHz (BW = 1 MHz)			-30	dBm
Receiver	**Minimum**	**Typical**	**Maximum**	**Unit**
Receiver Sensitivity (PER < 30.8%)			-70	dBm
Maximum Input Signal Level (PER < 30.8%)	-10			dBm
PER Report Integrity (-30 dBm input)	50		65.4	%

14 Land Pattern

The land pattern diagram for Type 1XA module is shown in **Figure 23.**

Figure 23: Land Pattern (Unit: mm)



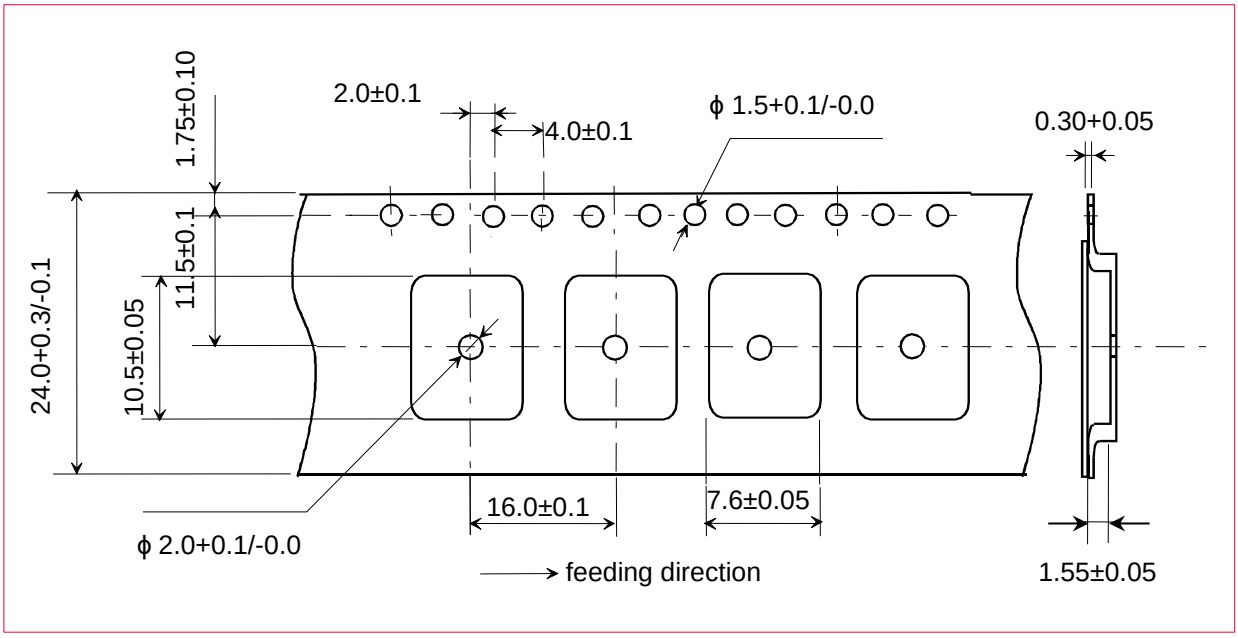
15 Tape and Reel Packing

This section provides the general specifications for tape and reel packing.

15.1 Dimensions of Tape (Plastic Tape)

Figure 24 is a graphical representation of the tape dimension (plastic tape).

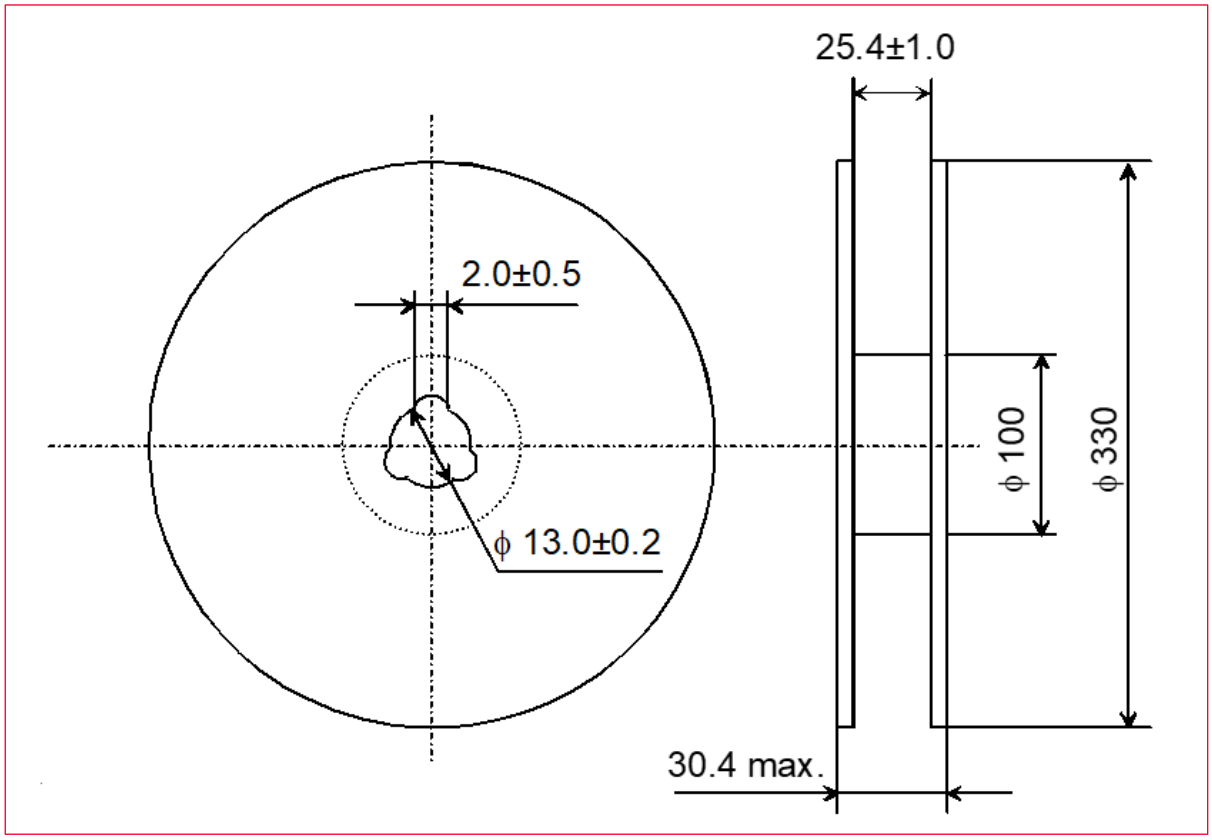
Figure 24: Dimensions of Tape (Unit: mm)



15.2 Dimension of Reel

Figure 25 shows the reel dimensions.

Figure 25: Dimension of Reel (Unit: mm)



15.3 Taping Diagrams

Figure 26 shows the tapings diagrams.

Figure 26: Taping Diagrams

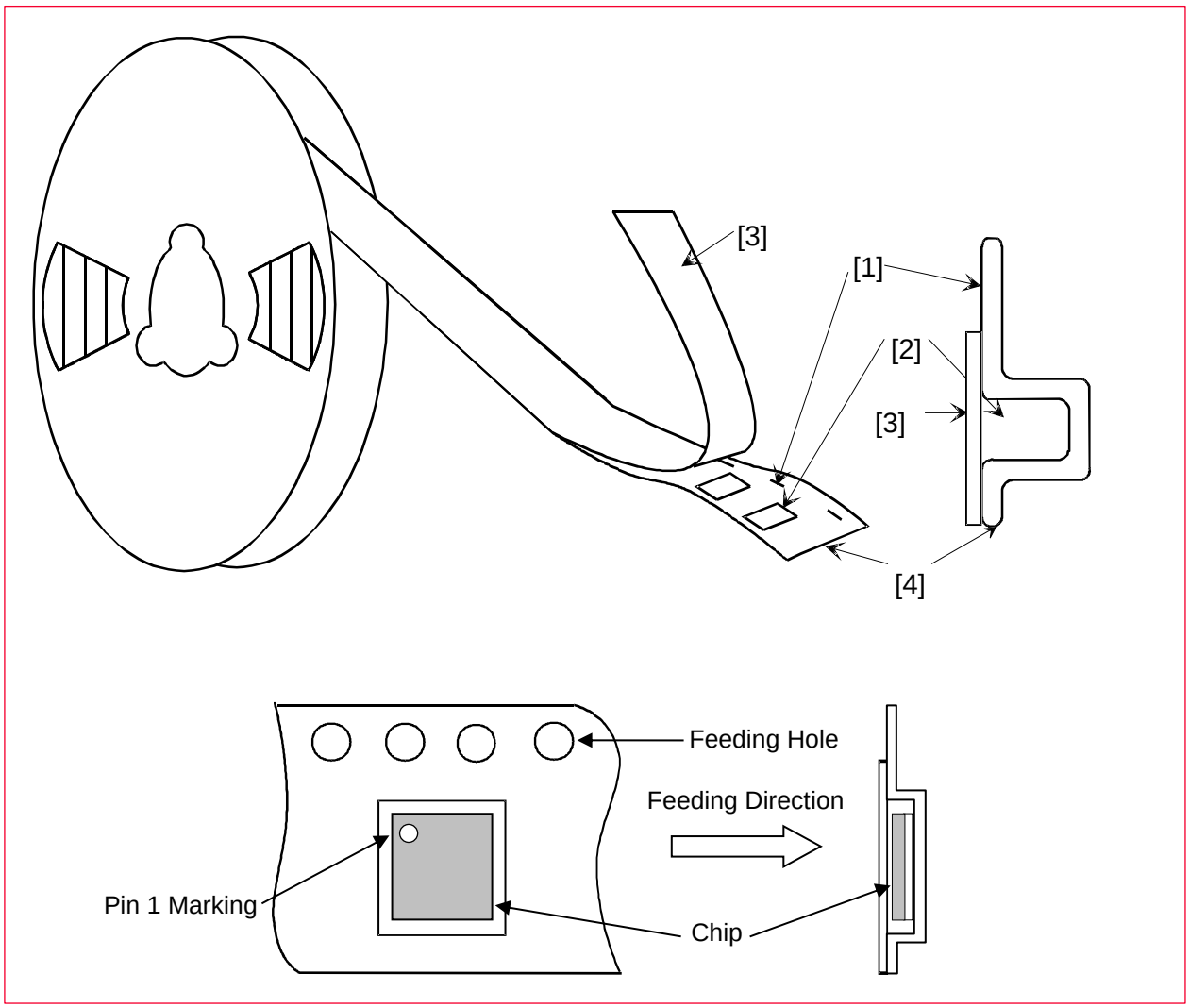


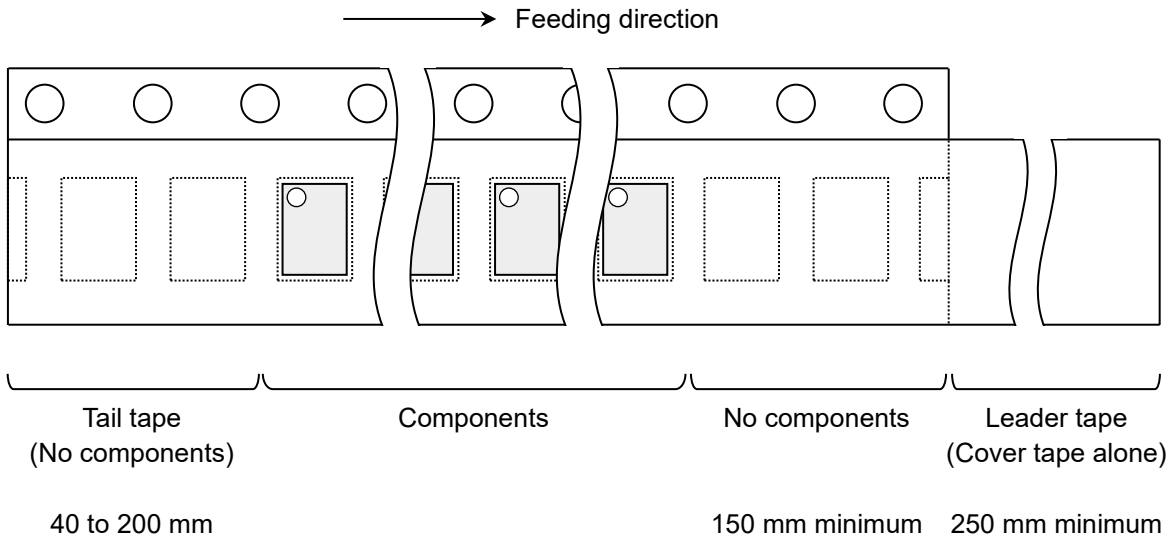
Table 28: Taping Specifications

Mark	Descriptions
[1] Feeding Hole	As specified in Dimensions of Tape
[2] Hole for chip	As specified in Dimensions of Tape
[3] Cover tape	62 µm in thickness
[4] Base tape	As specified in Dimensions of Tape

15.4 Leader and Tail Tape

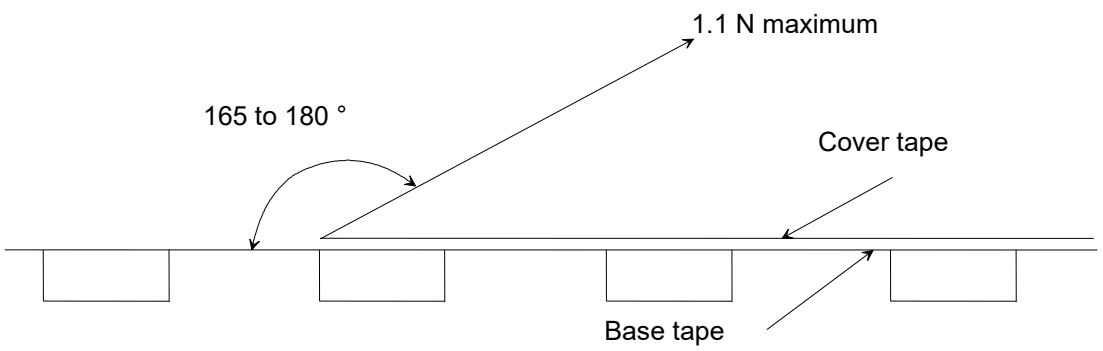
The leader and tail tape are shown in **Figure 27**.

Figure 27: Leader and Tail Tape



- The tape for chips is wound clockwise, the feeding holes to the right side as the tape is pulled toward the user.
- The cover tape and base tape are not adhered at no components area for 250 mm minimum.
- Tear off strength against pulling of cover tape: 5 N minimum.
- Packaging unit: 1000 pcs. / Reel
- Tape material:
  - Base tape: Plastic
  - Reel: Plastic
  - Cover tape, cavity tape and reel are made the anti-static processing.
- Peeling off force: 1.1 N maximum in the direction of peeling as shown in **Figure 28**.

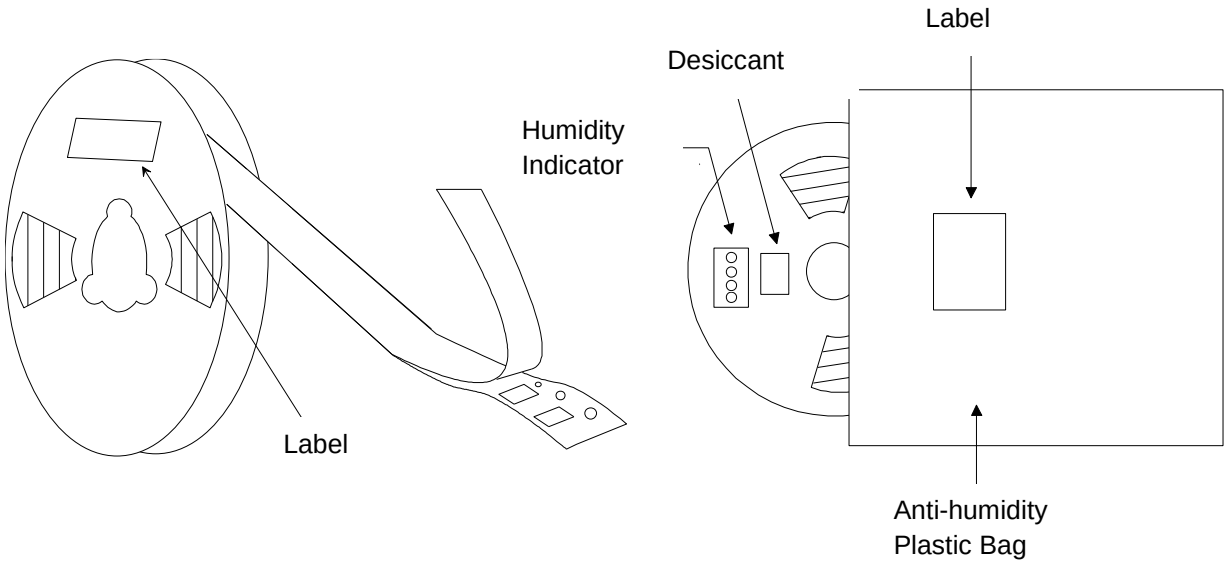
Figure 28: Peeling Off Force



15.5 Packaging (Humidity Proof Packing)

Figure 29 shows the humidity proof packaging.

Figure 29: Humidity Proof Packaging



Tape and reel must be sealed with the anti-humidity plastic bag. The bag contains the desiccant and the humidity indicator.

16 Notice

16.1 Storage Conditions

- Please use this product within 6 months after receipt.
  - The product shall be stored without opening the packing under the ambient temperature from 5 to 35 °C and humidity from 20 ~ 70 %RH (Packing materials may be deformed at the temperature over 40 °C).
  - The product left more than 6 months after reception; it needs to be confirmed the solderability before used.
  - The product shall be stored in noncorrosive gas (Cl_2, NH_3, SO_2, NO_X, etc.).
  - Any excess mechanical shock including, but not limited to, sticking the packing materials by sharp object and dropping the product, shall not be applied in order not to damage the packing materials.
- This product is applicable to MSL3 (Based on JEDEC Standard J-STD-020)
  - After the packing is opened, the product shall be stored at ≤ 30 °C / ≤ 60 %RH and the product shall be used within 168 hours.
  - When the color of the indicator in the packing changed, the product shall be baked before soldering.
- Baking condition: 125 +5/-0 °C, 24 hours, 1 time
- The products shall be baked on the heat-resistant tray because the materials (Base Tape, Reel Tape and Cover Tape) are not heat-resistant.

16.2 Handling Conditions

- Be careful in handling or transporting products because excessive stress or mechanical shock may break products.
- Handle with care if products may have cracks or damages on their terminals, the characteristics of products may change. Do not touch products with bear hands that may result in poor solderability and damage by static electrical charge.

16.3 Standard PCB Design (Land Pattern and Dimensions):

- All the ground terminals should be connected to the ground patterns. Furthermore, the ground pattern should be provided between IN and OUT terminals. Please refer to the specifications for the standard land dimensions.
- The recommended land pattern and dimensions is as Murata's standard. The characteristics of products may vary depending on the pattern drawing method, grounding method, land dimensions, land forming method of the NC terminals and the PCB material and thickness. Therefore, be sure to verify the characteristics in the actual set. When using non-standard lands, contact Murata beforehand.

16.4 Notice for Chip Placer

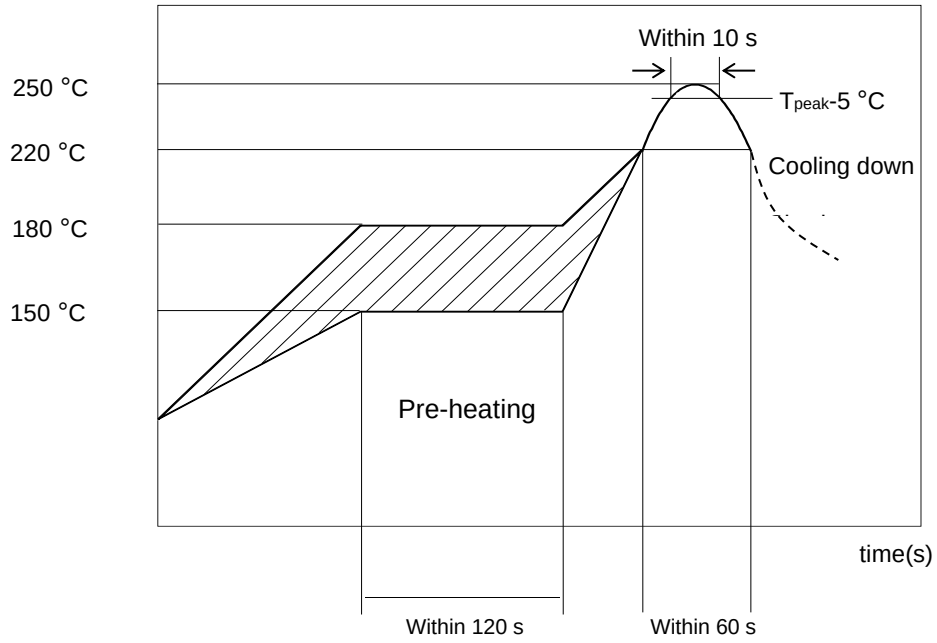
When placing products on the PCB, products may be stressed and broken by uneven forces from a worn-out chucking locating claw or a suction nozzle. To prevent products from damages, be sure to follow the specifications for the maintenance of the chip placer being used. For the positioning of products on the PCB, be aware that mechanical chucking may damage products.

16.5 Soldering Conditions

The recommendation conditions of soldering are shown in **Figure 30.**

Soldering must be carried out by the above-mentioned conditions to prevent products damage. Set up the highest temperature of reflow within 260 °C. Contact Murata before use concerning other soldering conditions.

Figure 30: Reflow Soldering Standard Conditions (Example)



Please use the reflow within 2 times.
Use rosin type flux or weakly active flux with a chlorine content of 0.2 wt % or less

16.6 Cleaning

This product is moisture sensitive therefore, cleaning is not permitted. If any cleaning process is done the customer is responsible for any issues or failures caused by the cleaning process.

16.7 Operational Environment Conditions

Products are designed to work for electronic products under normal environmental conditions (ambient temperature, humidity, and pressure). Therefore, products have no problems to be used under the similar conditions to the above-mentioned. However, if products are used under the following circumstances, it may damage products and leakage of electricity and abnormal temperature may occur.

- In an atmosphere containing corrosive gas (CL_2, NH_3, SO_X, NO_X, etc.).
- In an atmosphere containing combustible and volatile gases.
- Dusty place.
- Direct sunlight place.
- Water splashing place.
- Humid place where water condenses.
- Freezing place.

If there are possibilities for products to be used under the preceding clause, make sure to consult with Murata before actual use.

Do not apply static electricity or excessive voltage while assembling and measuring, as it might be a cause of degradation or destruction to apply static electricity to products.

16.8 Input Power Capacity

Products shall be used in the input power capacity as specified in this specification.

Inform Murata beforehand, in case that the components are used beyond such input power capacity range.

17 Precondition to Use Our Products

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Revision History

Revision	Date	Changed Item	Comment
1	Apr 18, 2019	First Issue	
2 (A)	June 05, 2020	9. Module Pin Descriptions	• Changed then name of pin 57 from VDDIO_SD to VDDIO. • Changed the name of pin 31 from RF_SW_CTRL13 to RF_SW_CTRL11.
3 (B)	Jul 07, 2020	8. Dimensions	Added Solder bump and defined T1 dimension
4 (C)	Oct 10, 2020	2. Key Feature 4. Sample Ordering Information 6. Operating Condition 11. I/O States 14. Electrical Characteristics	• Added Weight information. • Changed sample and EVB P/N. • Added operating temperature spec. • Corrected Typ. VBAT from 3.6V to 3.3V • Added I/O State Table • Added Output power spec.
5 (D)	Nov 11, 2020	8. Dimensions, Marking And Terminal Configurations 10. Reference Peripheral Circuit	• Added Marking information. • Added Reference circuit.
6 (E)	Dec 14, 2020	1. Scope 14.9. DC/RF Characteristics for Bluetooth	• Modified Bluetooth version. • Corrected Minimum output power.
7 (F)	Jan 28, 2021	8. Dimensions, Marking And Terminal Configurations 14. Electorical Characteristics	• Added pin 1 mark information on Bottom view. • Added current consumption information.
8 (G)	Feb 01, 2021	14.7. DC/RF Characteristics for IEEE802.11ac(HT 40MHz) - 5GHz 14.8. DC/RF Characteristics for IEEE802.11ac(HT 80MHz) - 5GHz	Optimized the max value of current consumption for VHT40/80 of 5GHz mode.
9 (H)	Mar 02, 2021	Appendix.	Added User's guide of certification.
10 (I)	Apr 01, 2021	10. Reference Peripheral Circuit	Applied the regulatory certification condition.
11 (J)	Nov 29, 2021	6. Operating Condition	Added Specification Temperature
12 (K)	June 30, 2022	Cover Page 2. Key Feature	Changed IC vendor name to Infineon
13 (L)	Sep 13, 2023	2. Key Features 4. Sample Ordering Information 10. Reference Peripheral Circuit 14. Electrical Characteristics Appendix	• Updated information • Added Embedded Artists' M.2 module information. Renamed section. Moved to before Block Diagram. • Moved section to HW app note. • Renamed section • Moved Appendix information into Section 15. • Added transmit power tables. • Added Europe section. • Moved antenna sections to HW app note. Updated to new format
14 (M)	Sep 10, 2024	2. Key Features 3 Ordering Information	• Add Fit value • Remove murata-EVB parts No

Revision	Date	Changed Item	Comment
		4. Block Diagram 15. Radio Regulatory Certification by Country for LBEE5XV1XA	• Modify Block diagram • Remove certification Information
15	Mar 31, 2025	4. Block Diagram 5 Dimensions, Markings and Terminal Configurations 13 DC/RF Characteristics	• Modify Block diagram • Add structure • Format change, name change from (13 Electrical Characteristics) • Updated (Base IC datasheet revision: E)