

# Extrem-Broadband Silicon Capacitor XBSC 0201 22nF BV30



Rev. 3.02

## General description

XBSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The XBSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 73 KHz to 150 GHz+.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 22 nF (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value for GHz range), combined in a 0201 [0.8x0.6mm] case.

The XBSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

XBSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature.

**Assembly:** Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminated) or flex platforms.

**Bump finishing:** ENIG

Copper pads optional for embedding version and SAC305 type 6 for pre-bumping version, as an optional finishing.

## Key features

- Ultra-Large band performance up to 150 GHz
- Resonance free
- Phase stability
- Insertion loss < 1.2dB Typ. up to 150 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 100 µm
- Break down voltage: 30V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0201 footprint

## Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. capacitance per unit volume)
- Broadband test equipment



## Functional diagram

The next figure provides implementation set-up diagram.

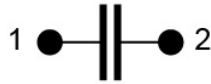


Figure 1 Block Diagram

## Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	22	-	nF
$\Delta C_P$	Capacitance tolerance <sup>(1)</sup>	@+25°C	-15	-	+15	%
T <sub>OP</sub>	Operating temperature		-55	20	150	°C
T <sub>STG</sub>	Storage temperature <sup>(2)</sup>		-70	-	165	°C
$\Delta C_T$	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV <sub>DC</sub>	Rated voltage <sup>(3)</sup>		-	-	16 <sup>(4)</sup> 14.7 <sup>(5)</sup>	V <sub>DC</sub>
BV	Break down voltage	@+25°C	30	-	-	V
$\Delta C_{RVDC}$	Capacitance voltage variation	From 0 V to RV <sub>DC</sub> , @+25°C	-	-	0.1	%/V <sub>DC</sub>
IR	Insulation resistor	@RV <sub>DC</sub> , +25°C, 120s	-	10	-	GΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	20	-	pH
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	220	-	mΩ
Fc-3dB	Cut-off frequency at 3dB <sup>(6)</sup>	@+25°C	-	73	86	kHz
IL	Insertion loss <sup>(6)</sup>	@ 20 GHz, +25°C	-	0.2	-	dB
		@ 40 GHz, +25°C	-	0.3	-	dB
		@ 60 GHz, +25°C	-	0.3	-	dB
		@ 80 GHz, +25°C	-	0.6	-	dB
		@ 110 GHz, +25°C	-	0.9	-	dB
		@ 150 GHz, +25°C	-	1.2	-	dB
RL	Return loss <sup>(6)</sup>	Up to 150 GHz, +25°C	13	-	-	dB
ESD	HBM stress <sup>(7)</sup>	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

<sup>(1)</sup>: other tolerance available upon request.

<sup>(2)</sup>: without packaging.

<sup>(3)</sup>: Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.

<sup>(4)</sup>: 10 years of intrinsic life time prediction at 100°C continuous operation.

<sup>(5)</sup>: 10 years of intrinsic life time prediction at 150°C continuous operation.

<sup>(6)</sup>: Simulation.

<sup>(7)</sup>: please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.



**Module of S-parameters of 22nF XBSC in transmission mode**

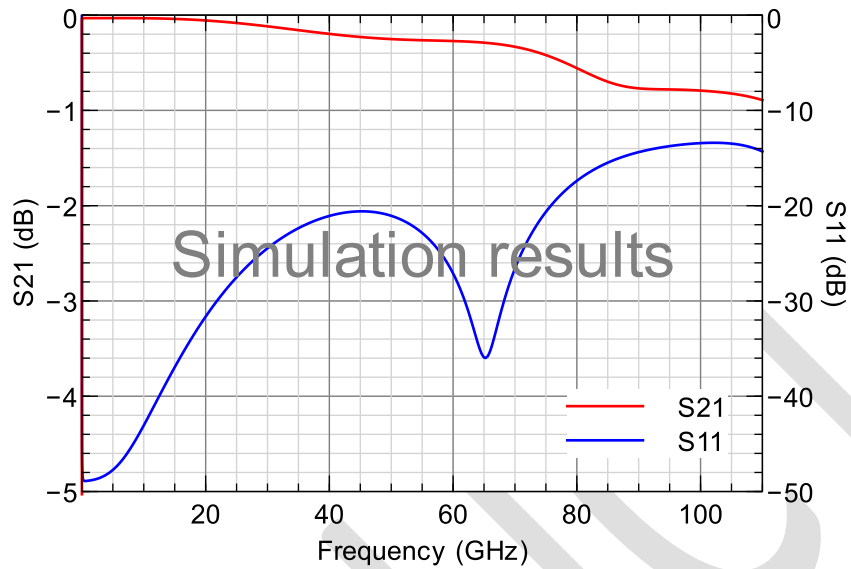
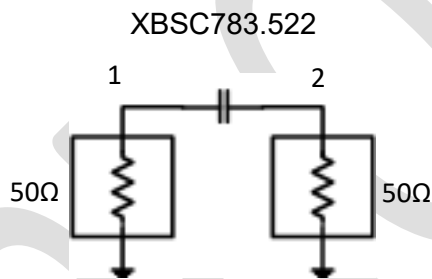


Figure 2 - 22nF XBSC simulation results (module of S-parameters)

**Schematic of 22nF XBSC in transmission mode**



**Example of 0201 surface mounted**

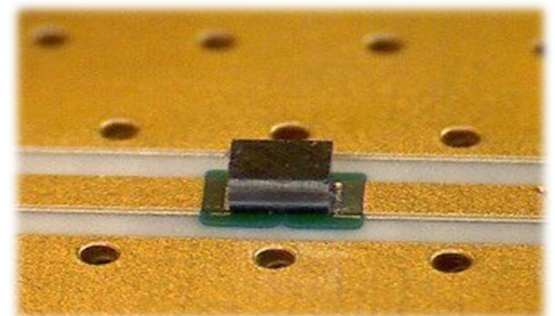


Figure 4 – micro picture of XBSC mounted on board in coplanar mode

**6.6-mil Rogers 4350B.**

Microstrip mode – line width = 0.400mm and gap = 0.300 mm. (nominal 50 ohm characteristic impedance).

Figure 3 - 22nF XBSC measurement schematic



## Pinning definition

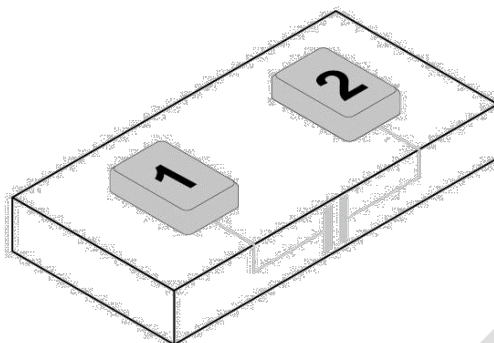


Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-225.0 / 0.0
2	Signal	225.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

## Ordering Information for XBSC783.522

Type number (15NC)	Package		
	Packaging <sup>(1)</sup>	Finishing	Description
939118783522-T3N	7" T&R (1 000 pieces/reel) <sup>(3)(5)</sup>	ENIG <sup>(2)</sup>	XBSC 0201 - 22nF – 2 pads – 0.8 x 0.6 mm x 0.10mm <sup>(4)</sup>
939118783522-T3S	7" T&R (1 000 pieces/reel) <sup>(3)(5)</sup>	SAC <sup>(2)</sup>	XBSC 0201 - 22nF – 2 pads – 0.8 x 0.6 mm x 0.10mm <sup>(4)</sup>

(1) Other film frame carrier are possible on request

(2) SAC = ENIG (0.1µm Au / 5µm Ni) + SAC305 type 6 or NiAu = ENIG (0.1µm Au / 5µm Ni)

(3) missing capacitors can reach 0.5%

(4) refer to Figure 9

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
XBSC783.522	XJ0201522	XBSC 22nF/0201/BV30 – 2 pads – 0.8 x 0.6 mm x 0.10mm

Table 4 - Die information



## Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with ENIG (0.1µm Au / 5µm Ni) (Refer to Figure 6).

Other Metallization, such as SAC305 type 6 bumping (Refer to Figure 7), Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

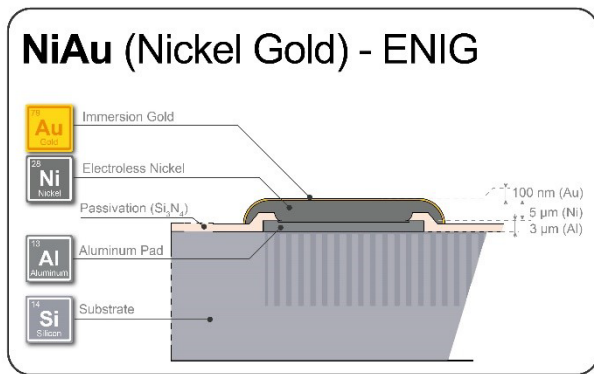


Figure 6 – Top electrode description of ENIG finishing version



Figure 7 – Top electrode description of SAC305 pre-bumped version

## Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.



## Package outline

The product is delivered as a bare silicon die.

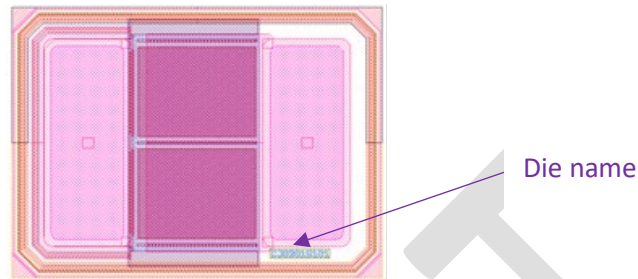


Figure 8 – Layout view

	L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
Component dimension	0.80 ±0.02	0.60 ±0.02	0.41 max or 0.11 max	0.15	0.30	0.40	0.005 <sup>(1)</sup> or 0.04 <sup>(2)</sup> 0.065 <sup>(3)</sup>
Landing pad recommendation	/	/	/	0.164 min	0.286 max	0.414 min	/

(1) Standard with ENIG

(2) Solder joint height after reflow on board in case of SAC305 pre-bumping.

(3) Solder bump height before assembly

Table 5 - Dimensions and tolerances

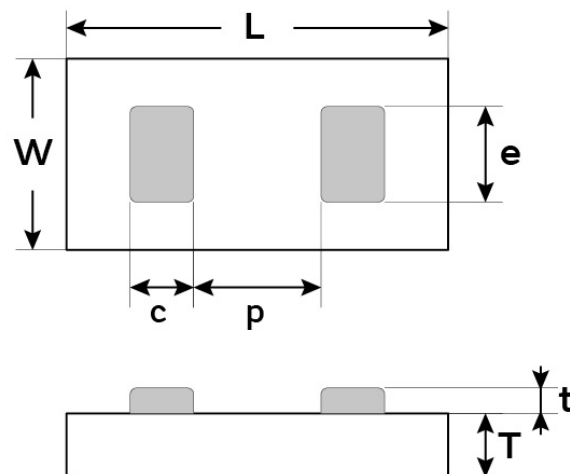


Figure 9 - Package outline drawing

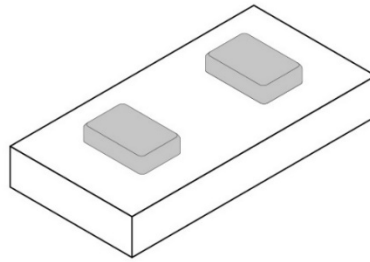


Figure 10 - Package isometric view

PRODUCT



## Assembly

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XBSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 11 Scan this QR Code to access the Murata Silicon Capacitor web page



## Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

**Tape and Reel:** Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

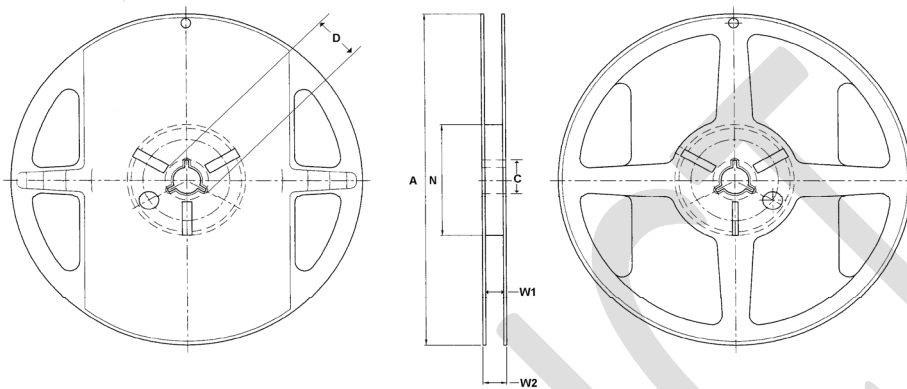


Figure 12 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 6 - Reel dimensions (mm)

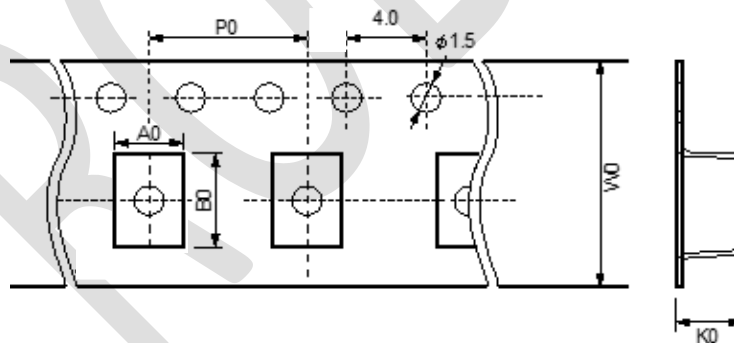


Figure 13 - Tape drawing (not to scale)

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Quantity per reel	Die thickness
A0	B0	K0				T(mm)
0.76	0.96	0.22	8	2	1 000	100µm
0.74	0.94	0.57	8	4	1 000	400µm

Table 7 - Tape dimensions (mm)

## Definitions

### Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

### Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

### Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

Revision	Date	Description	Author
Release 0.01	2021 July 01st	Creation	OGA
Release 1.02	2021 July. 15th	Objective	OGA
Release 2.00	2021 Nov. 18th	Preliminary	OGA
Release 2.01	2024 January 05th	Extended high limit frequency / adding scheme	DYE
Release 3.00	2025 January 15th	Extended high limit frequency / adding scheme	DYE / MOK / OGA
Release 3.01	2025 March 15th	Complementary land pattern information	DYE / MOK / OGA
Release 3.02	2025 Oct. 21st	Ordering information has been updated according to the latest product lineup and specification.	CGU, HFU

## Disclaimer / Life support applications

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