Extreme-Broadband Silicon Capacitor XBSC 0201M 10nF BV30

Rev. 3.04

General description

XBSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products. The XBSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system. The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 160 KHz to 160 GHz.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 10 nF (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value for GHz range), combined in a 0201M [0.6x0.3mm] case.

The XBSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.

XBSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature.

Assembly: Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminate) or flex platforms.

Bump finishing: pre-bumped SAC305 type 6 or un-bumped ENIG. Copper pads for embedding version as an optional finishing.

Key features

- Ultra-Broadband performance up to 160 GHz
- Resonance free
- Phase stability
- Insertion low < 0.5dB Typ. up to 160 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 140 µm including bump height (SAC305 40µm bumps after reflow)
- Break down voltage: 30V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 01005 footprint and with EIA 0201 outline

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency *(i.e. capacitance per unit volume)*
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	10	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature(2)		-55	20	150	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
V_{DC}	Operating voltage (3)		-	-	16(4) 13.6(5)	V_{DC}
BV	Break down voltage	@+25°C	30	-	-	V
ΔC_{VDC}	Capacitance voltage variation	From 0 V to V_{DC}, @+25°C	-	-	-0.1	%/V_{DC}
IR	Insulation resistor	@V_{DC}, +25°C, 120s	-	10	-	GΩ
Fc_{-3dB}	Cut-off frequency at 3dB	@+25°C	-	160	187	kHz
IL	Insertion loss	@ 20 GHz, +25°C	-	0.2	-	dB
		@ 40 GHz, +25°C	-	0.3	-	dB
		@ 60 GHz, +25°C	-	0.3	-	dB
		@ 80 GHz, +25°C	-	0.4	-	dB
		@ 160 GHz, +25°C	-	0.5	-	dB
RL	Return loss	Up to 160 GHz, +25°C	10	-	-	dB
ESD	HBM stress (6)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): *other tolerance available upon request.*

(2): *Regarding the storage temperature, please refer to the following application note.: Storage and shelf life conditions*

(3): *Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.*

(4): *10 years of intrinsic lifetime prediction at 100°C continuous operation.*

(5): *10 years of intrinsic lifetime prediction at 150°C continuous operation.*

(6): *please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.*

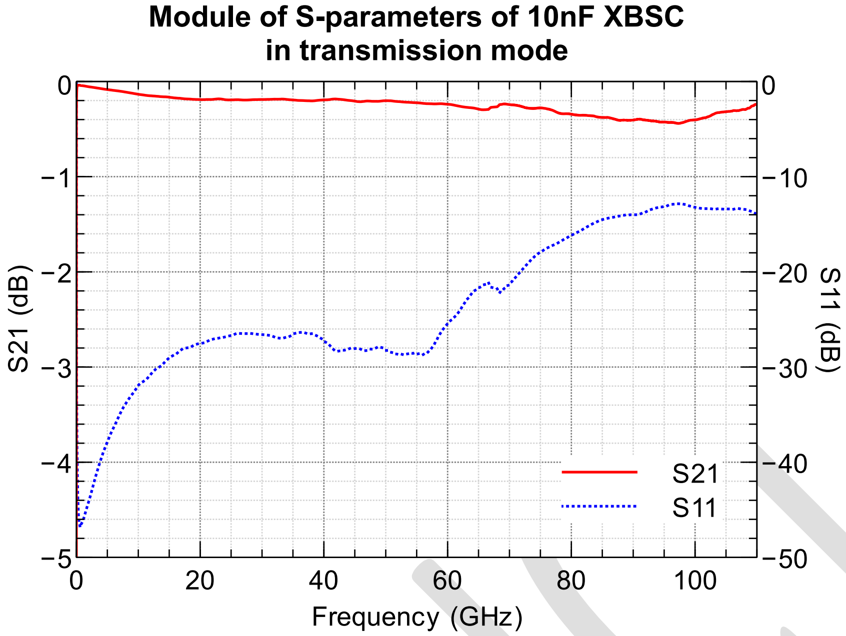
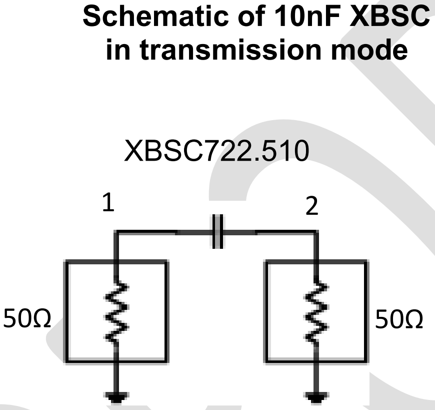


Figure 2 - 10nF XBSC simulated results (module of S-parameters)



4-mil Rogers 4350B.
Microstrip mode – line width = 0.200mm and gap = 0.200 mm.
(nominal 50 ohm characteristic impedance).

Figure 3 - 10nF XBSC measurement schematic

Example of 0201M surface mounted

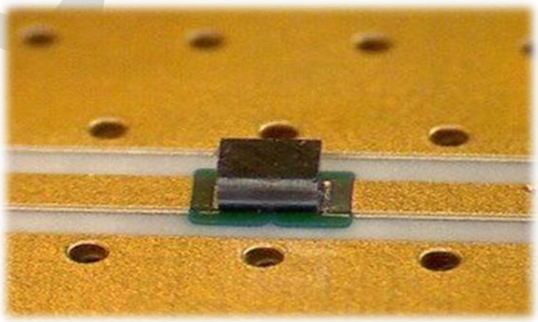


Figure 4 – micro picture of XBSC mounted on board in coplanar mode

Pinning definition

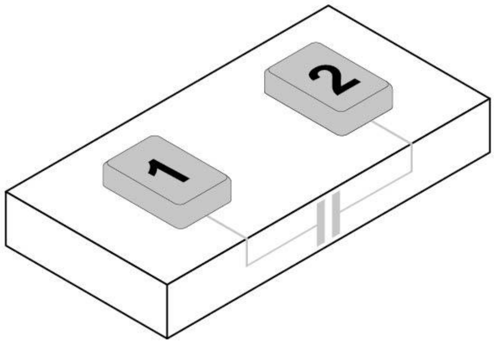


Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-150.0 / 0.0
2	Signal	150.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information for XBSC722.510

Type number	Package		
	Packaging (1)	Finishing	Description
939118722510-T3S	7” T&R (1 000 pieces/reel) (3) (5)	SAC (2)	XBSC 0201M - 10nF – 2 pads – 0.6 x 0.3 x 0.10 mm (4)
939118722510-T5S	7” T&R (5 000 pieces/reel) (3) (6)		
939118722510-T4S	7” T&R (10 000 pieces/reel) (3) (6)		
939118722510-T3N	7” T&R (1 000 pieces/reel) (3) (5)	ENIG (2)	
939118722510-T5N	7” T&R (5 000 pieces/reel) (3) (6)		
939118722510-T4N	7” T&R (10 000 pieces/reel) (3) (6)		

(1) Other Film Frame Carrier are possible on request
(2) SAC = ENIG (0.1µm Au / 5µm Ni) + SAC305 type 6 or ENIG 0.1µm Au / 5µm Ni
(3) Missing capacitors can reach 0.5%
(4) Refer to Figure 9
(5) Dedicated for Pre-Production
(6) For all demands including Mass Production

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
XBSC722.510	XTM0201510	XBSC 10nF/0201M/BV30 – 2 pads – 0.6 x 0.3 x 0.10 mm

Table 4 - Die information

Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with SAC305 type 6 bumping (Refer to Figure6).
Other Metallization, such as ENIG (0.1µm Au / 5µm Ni) (Refer to Figure7), Copper, Thick Gold or Aluminum pads are possible on request.
Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

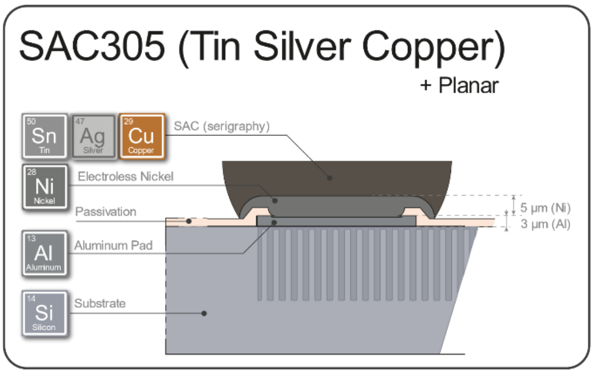


Figure 6 – Top electrode description of SAC305 pre-bumped version

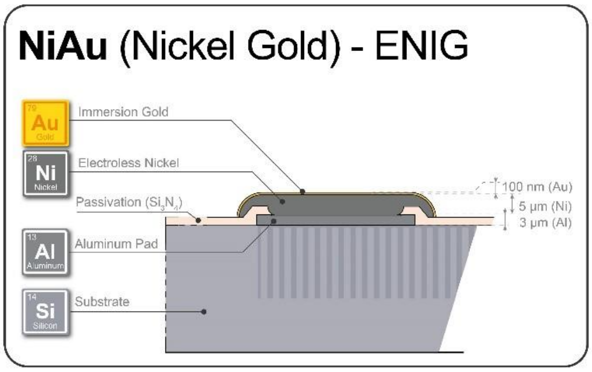


Figure 7 – Top electrode description of ENIG finishing version

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die, with passivation opening for contacts.

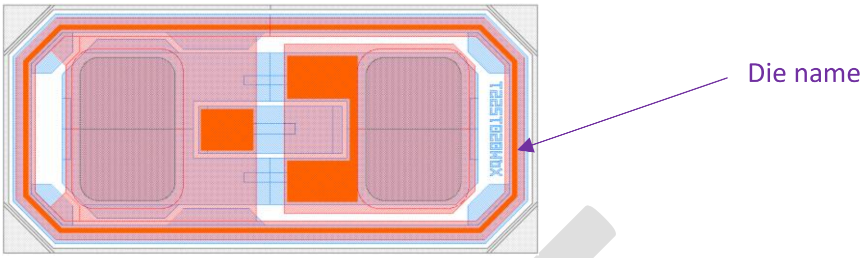


Figure 8 — Layout view

	L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
Component dimension	0.60 ±0.02	0.30 ±0.02	0.11 max	0.10	0.20	0.15	0.04(1) 0.05(2) 0.005 (3)
Landing pad recommendation	/	/	/	0.114 min	0.186 max	0.164 min	/

(1) Solder joint height after reflow on board with mirror pads
(2) Solder bump height before assembly
(3) only with ENIG on optional version

Table 5 - Dimensions and tolerances

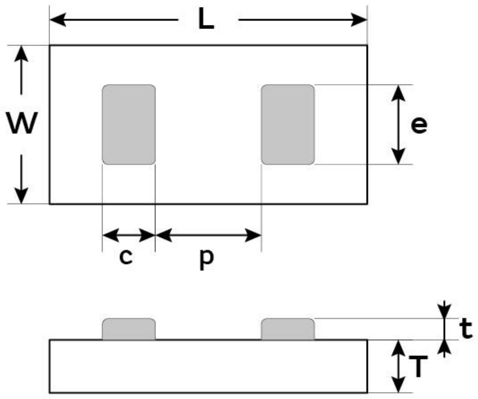


Figure 9 - Package outline drawing

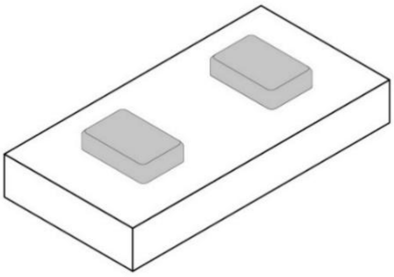


Figure 10 - Package isometric view

Assembly

XBSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 11 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

Tape and Reel: Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

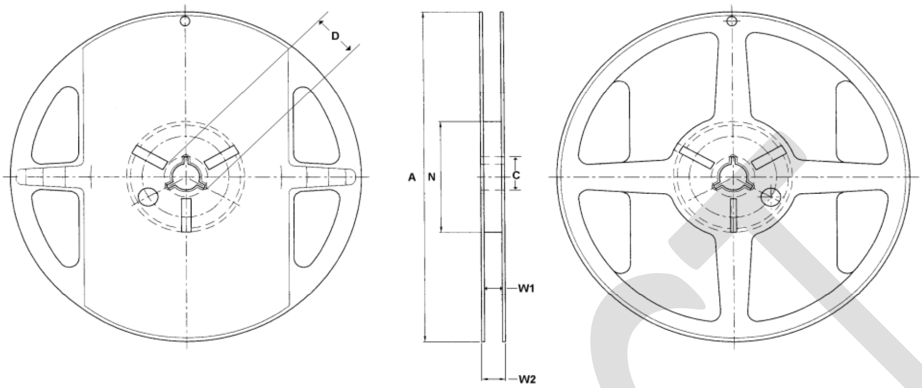


Figure 12 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	21	60	9.5	11.4

Table 6 - Reel dimensions (mm)

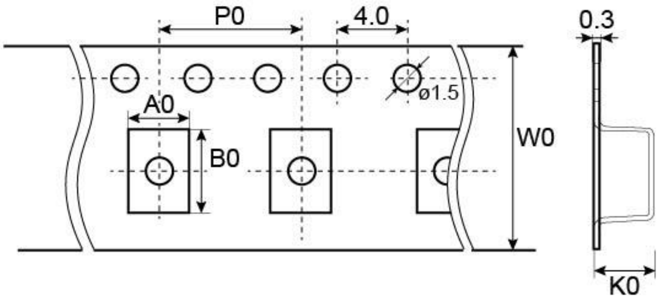


Figure 13 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
0.37 +/-0.04	0.67 +/-0.04	0.20 +/-0.04	8.00	2.00	1000 or 5000

Table 7 - Tape dimensions (mm)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 1.01	**2020 July 20th**	**Creation**	**OGA**
Release 1.02	**2020 Sept 15th**	**General update**	**OGA**
Release 1.03	**2021 May 25th**	**Add Measurement Graph**	**OGA, DDE, DYO, LLE. SCA; CGU**
Release 2.00	**2021 Nov. 23rd**	**Minor update**	**OGA, DDE, DYO, LLE. SCA; CGU**
Release 3.00	**2022 Oct. 11th**	**Product status update**	**OGA, SCA**
Release 3.01	**2023 March 10th**	**Packaging update**	**CGU**
Release 3.02	**2023 Oct 31th**	**Extended high frequency limit**	**DYE, OGA**
Release 3.03	**2025 Jan 15th**	**Complementary land pattern information**	**MOK+ DYE + OGA**
Release 3.04	**2025 Sep 24th**	**Small update**	**MOY+ DYE + OGA**

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Technical Datasheet
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