

Xtrem 220GHz Broadband Silicon Capacitor X2SC 01005M

2.2nF BV11



Rev. 2.03

General description

X2SC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.

The X2SC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 723 KHz to 220 GHz.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 2.2nF (for kHz–MHz range) and MIM capacitors for low capacitance value (for GHz range), both in a SMT 01005M (0.4 x 0.2mm).

The X2SC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability. X2SC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

Assembly: Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminate) or flex platforms.

Bump finishing: SAC305 type 6.

Copper pads optional for embedding version and ENIG for un-bumped version, as an optional finishing.

Key features

- Ultra large band performance to 220 GHz
- Resonance free
- Phase stability
- Insertion loss < 0.8dB Typ. up to 220 GHz
- Ultra-high stability of capacitance value:
 - Temperature 70ppm/K (-55 °C to +150 °C)
 - Voltage < -0.1%/Volt
 - Negligible capacitance loss through ageing
- Low profile
- SAC305 15µm bumps after reflow
- Break down voltage: 11V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 008004 footprint and with EIA 01005 outline

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. capacitance per unit volume)
- Broadband test equipment



Functional diagram

The next figure provides implementation set-up diagram.

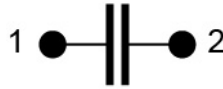


Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	2.2	-	nF
ΔC_P	Capacitance tolerance ⁽¹⁾	@+25°C	-15	-	+15	%
T _{OP}	Operating temperature		-55	20	150	°C
T _{STG}	Storage temperature ⁽²⁾		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV _{DC}	Rated voltage ⁽³⁾		-	-	3.8 ⁽⁴⁾ 3.4 ⁽⁵⁾	V _{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV _{DC} , @+25°C	-	-	-0.1	%/V _{DC}
IR	Insulation resistor	@RV _{DC} , +25°C, 120s	-	10	-	GΩ
F _{c-3dB}	Cut-off frequency at 3dB ⁽⁶⁾	@+25°C	-	723	851	kHz
IL	Insertion loss ⁽⁶⁾	@ 20 GHz, +25°C	-	0.1	-	dB
		@ 40 GHz, +25°C	-	0.1	-	dB
		@ 60 GHz, +25°C	-	0.2	-	dB
		@ 80 GHz, +25°C	-	0.2	-	dB
		@ 100 GHz, +25°C	-	0.2	-	dB
		@ 150 GHz, +25°C	-	0.3	-	dB
		@ 220 GHz, +25°C	-	0.8	-	dB
RL	Return loss ⁽⁶⁾	Up to 220 GHz, +25°C	13	-	-	dB
ESD	HBM stress ^{(6) (7)}	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request

(2): without packaging

(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'

(4): 10 years of intrinsic life time prediction at 100°C continuous operation

(5): 10 years of intrinsic life time prediction at 150°C continuous operation

(6): Simulation

(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

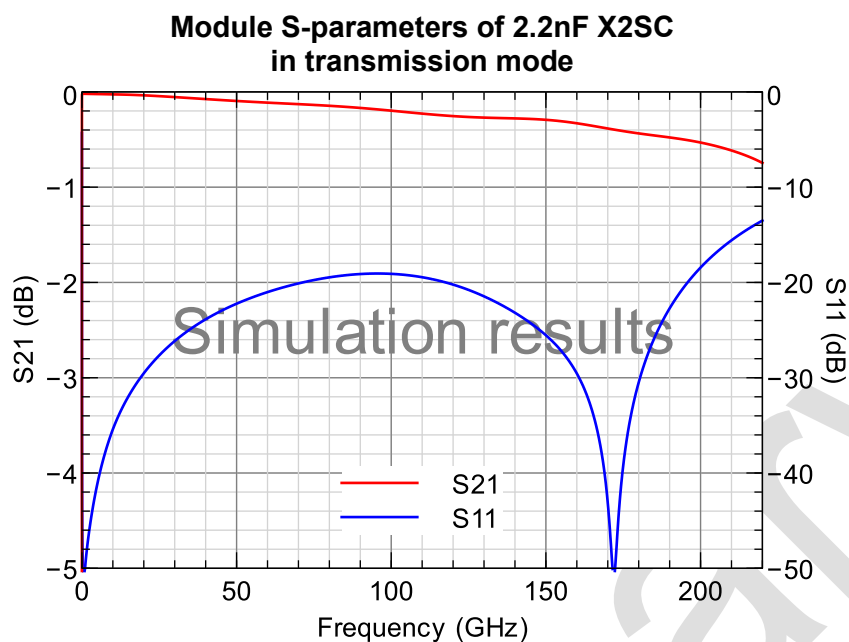
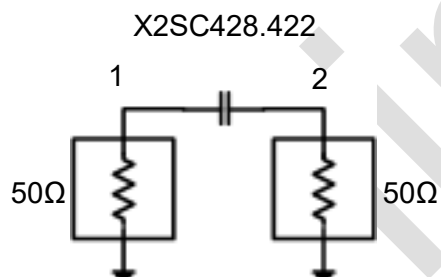


Figure 2 – 2.2nF X2SC simulation results
(module of S-parameters)

**Schematic of 2.2nF X2SC
in transmission mode**



4-mil Rogers 4350B.

Microstrip mode – line width = 0.20 mm and gap = 0.100 mm.
(nominal 50-ohm characteristic impedance).

Figure 3 – 2.2nF X2SC measurement schematic

Example of surface mounted 01005M

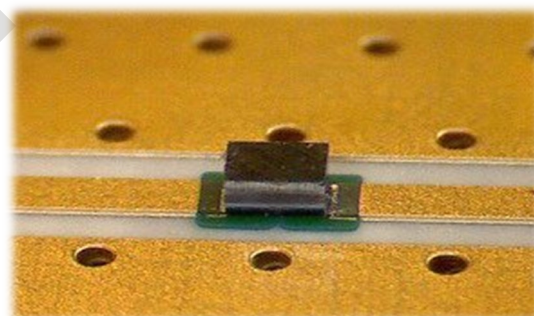


Figure 4 – micro picture of X2SC mounted on board
in coplanar mode



Pinning definition

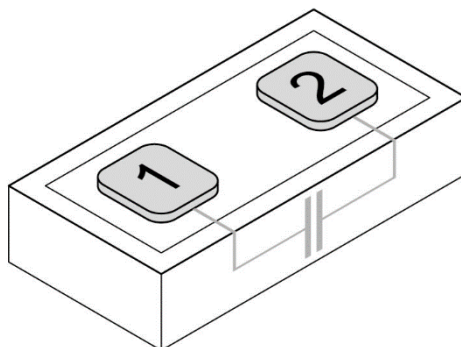


Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-104.5 / 0
2	Signal	104.5 / 0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Part number	Package		
	Packaging ⁽¹⁾	Finishing	Description
939120428422-T5S	7" T&R (5 000 pieces/reel) ⁽³⁾ ⁽⁵⁾	SAC ⁽²⁾	X2SC 01005M – 2.2nF – 2 pads – 0.40mm x 0.20mm x 0.10mm ⁽⁴⁾
939120428422-T5N	7" T&R (5 000 pieces/reel) ⁽³⁾ ⁽⁵⁾	ENIG ⁽²⁾	X2SC 01005M – 2.2nF – 2 pads – 0.40mm x 0.20mm x 0.10mm ⁽⁴⁾

Table 3 - Packaging and ordering information

- (1) Other Film Frame Carrier are possible on request
 (2) SAC = ENIG (0.1µm Au / 5µm Ni) + SAC305 type 6 or ENIG 0.1µm Au / 5µm Ni
 (3) Missing capacitors can reach 0.5%
 (4) Refer to Figure 8
 (5) For all demands including Mass Production

Product Name	Die Name	Description
X2SC428.422	XD01005422	X2SC 2.2nF/01005M/BV11 – 2 pads – 0.4 x 0.2 x 0.10 mm ⁽⁴⁾

Table 4 - Die information



Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with SAC305 type 6 bumping (Refer to Figure6). Other Metallization, such as ENIG (0.1µm Au / 5µm Ni) (Refer to Figure7), Copper, Thick Gold or Aluminium pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

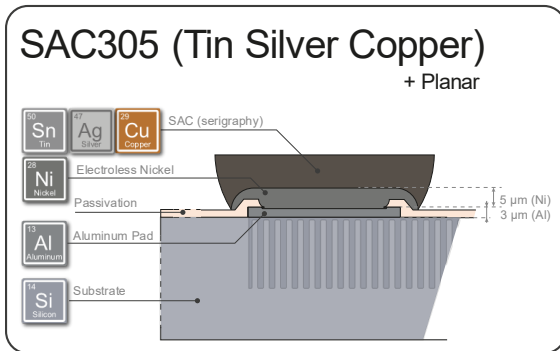


Figure 6 – Top electrode description of SAC305 pre-bumped version

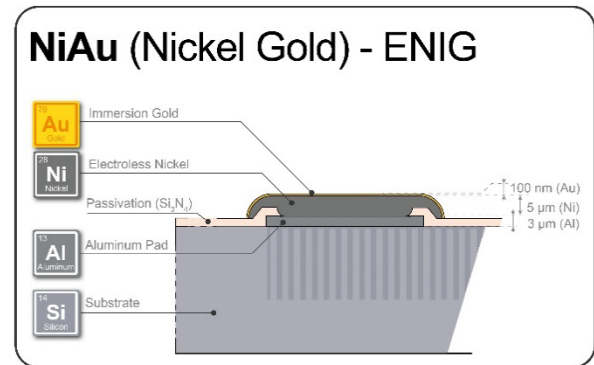


Figure 7 – Top electrode description of ENIG finishing version

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.



Package outline

The product is delivered as a bare silicon die.

L (μm)	W (μm)	T (μm)	d (μm)	e (μm)	g (μm)	b (μm)
400 ^{±20}	200 ^{±20}	100 ^{±15}	94 ^{±2}	85 ^{±2}	124 ^{±4}	22.5 ^{±6} (1) 8 ^{±2} (2)

(1) Standard with solder bump height before assembly
(2) Only in case of ENIG finishing

Table 5 - Dimensions and tolerances

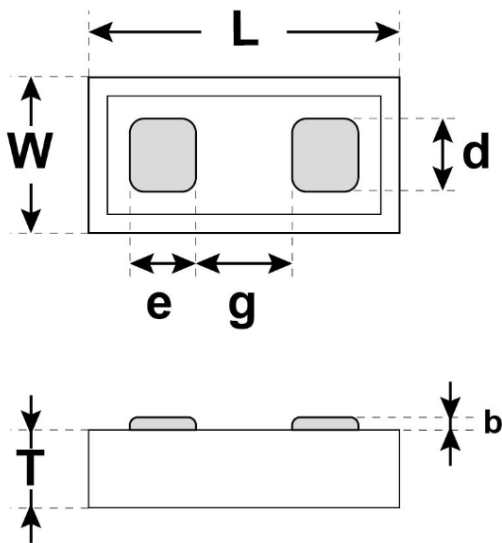


Figure 8 - Package outline drawing

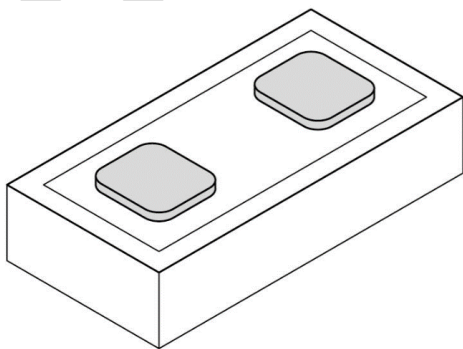


Figure 9 Isometric view



Assembly

X2SC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 10 Scan this QR Code to access the Murata Silicon Capacitor web page



Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel: Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

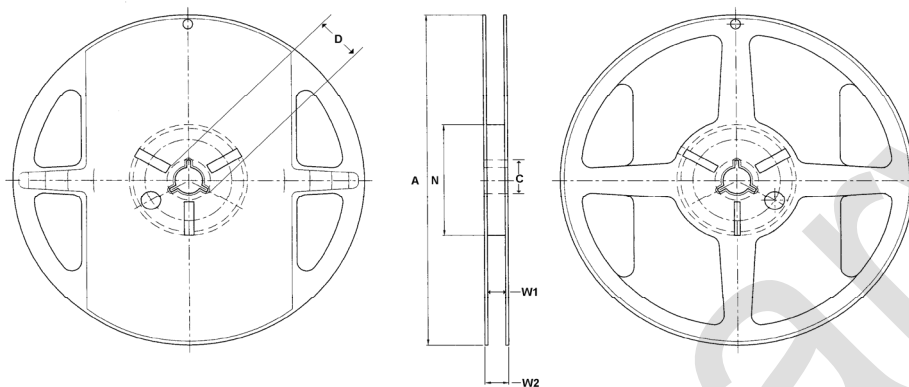


Figure 11 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	21	60	9.5	11.4

Table 6 - Reel dimensions (mm)

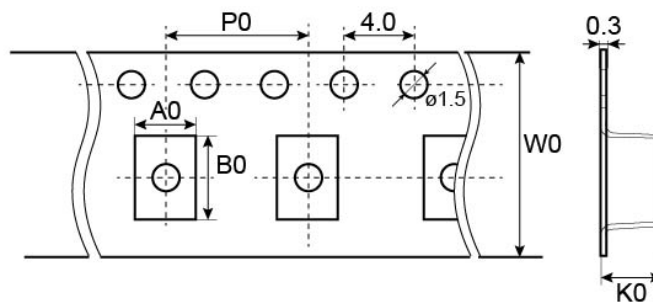


Figure 12 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity	Version
A0	B0	K0				
0.27	0.47	0.16	8	2	5 000	Pre-bumped
0.27	0.47	0.14				Un-bumped

Table 7 - Tape dimensions (mm)



Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 0.01	2021 April 8th	Initial version	OGA
Release 0.02	2021 August 31st	Update	OGA, SCA
Release 0.04	2021 Dec. 9th	Update	OGA
Release 0.05	2022 April 25th	Update of Capacitance value & expander grip ring view	OGA
Release 1.01	2022 Nov. 24th	P/N limitation to 5Kpcs/reel for both version	OGA
Release 2.00	2023 Feb. 28th	Added T&R pocket information and only T&R	OGA
Release 2.01	2023 Nov 3 rd	Update Data/ adding graph	DYE, OGA
Release 2.02	2025 Apr. 29 th	Correction of bump height	LIM, OGA
Release 2.03	2025 Oct. 21 st	Ordering information has been updated according to the latest product lineup and specification.	CGU, HFU

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