

# Ultra large band Wire bondable Silicon Capacitor UWSC 0202 1nF BV150



Rev. 3.01

## General description

**Market:** UWSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products. The UWSC is suitable for DC decoupling and bypass applications in all broadband optoelectronics and High-speed data system. The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with high rejection up to 26 GHz. These Ultra large band Wire Bondable MOS vertical Silicon Capacitors (UWSC) have been developed in a semiconductor process, in order to combine *ultra-deep trench MOS capacitors for high capacitance value of 1nF* and *MIM capacitors for low capacitance value, both in a 0202-package size*. Other capacitance values and other package size are available as a single capacitor or capacitor array; please feel free to contact us. The UWSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability. UWSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (+70ppm/K).

**Assembly:** UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding.

UWSC capacitors have the bottom electrode in Ti (0.1 μm)/Ni (0.3μm)/Au (0.2μm) and top electrode in Gold, other top finishing are available on request such as 3μm Aluminum (Al/Si/Cu: 98.96%/1%/0.04%).

## Key features

- Ultra large band performance to 26 GHz
- Resonance free
- Phase stability
- High rejection at 20 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.02%/Volts
  - Negligible capacitance loss through ageing
- Low profile: 250μm, 100 μm on request
- Break down voltage: 150V
- Low leakage current < 70pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0202 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

## Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. capacitance per unit volume)
- Broadband test equipment



**Functional diagram**

The next figure provides implementation set-up diagram.



Figure 1 Block Diagram

**Electrical performances**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	1	-	nF
$\Delta C_P$	Capacitance tolerance <sup>(1)</sup>	@+25°C	-15	-	+15	%
T <sub>OP</sub>	Operating temperature		-55	20	+150	°C
T <sub>STG</sub>	Storage temperature <sup>(2)</sup>		-70	-	+165	°C
$\Delta C_T$	Capacitance temperature variation	-55°C to +150°C		70		ppm/K
RV <sub>DC</sub>	Rated voltage <sup>(3)</sup>		-	-	68 <sup>(4)</sup> 61 <sup>(5)</sup>	V <sub>DC</sub>
BV	Breakdown voltage	@+25°C	150	-	-	V
$\Delta C_{RVDC}$	DC Capacitance voltage variation	From 0V to RV <sub>DC</sub> , @+25°C	-	-	-0.02	%/V <sub>DC</sub>
IR	Insulation resistance	@ RV <sub>DC</sub> , +25°C, 120s	-	100	-	GΩ
ESL	Equivalent Series Inductance	@+25°C, SRF shunt mode	-	4	-	pH
ESR	Equivalent Serial Resistance	@+25°C, SRF shunt mode	-	25	-	mΩ
ESD	HBM stress <sup>(6)</sup>	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request  
 (2): without packaging  
 (3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'  
 (4): 10 years of intrinsic life time prediction at 100°C continuous operation  
 (5): 10 years of intrinsic life time prediction at 150°C continuous operation  
 (6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'



PRODUCT



**1nF UWSC Impedance characteristic versus Frequency in shunt mode**

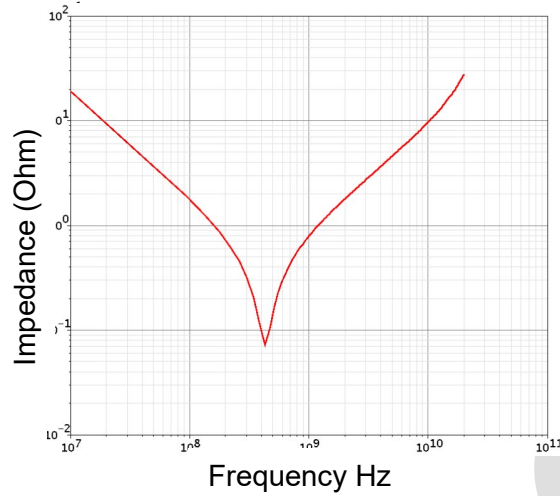


Figure 2 – 100pF UWSC measurement results (module of S-parameters)

**Schematic of 1nF UWSC in shunt mode**

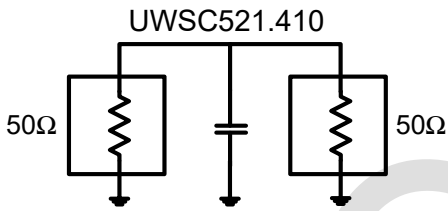


Figure 4 – 1nF UWSC measurement schematic

**Test bench**

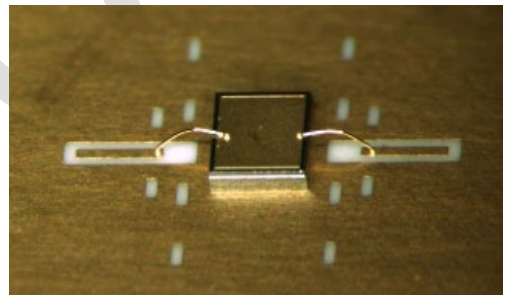


Figure 3 - test bench picture used for 1nF UWSC characterization (picture for information only)

**Pinning definition**

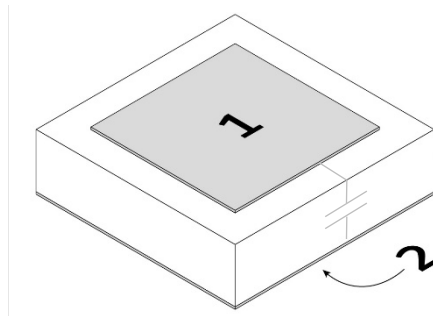


Figure 5 Pinning definition

pin #	Symbol	Coordinates X / Y
1	Signal	0.0 / 0.0
2	GND	Backside

Table 2 - Pinning description. Reference (0,0) located at the centre of the die.

**Ordering Information**

Part number (15NC)	Package		
	Packaging	Finishing	Description
935153521410-E1T	6" GR <sup>(2)</sup>	Au <sup>(1)</sup>	UWSC 1nF/0202 – 1 bondpad – 0.5x 0.5x 0.25mm
935153521410-T3T	T&R 1 000units	Au <sup>(1)</sup>	UWSC 1nF/0202 – 1 bondpad – 0.5x 0.5x 0.25mm
935153521410-W0T	WP max 400units	Au <sup>(1)</sup>	UWSC 1nF/0202 – 1 bondpad – 0.5x 0.5x 0.25mm
935154521410-E1T	6" GR <sup>(2)</sup>	Au <sup>(1)</sup>	UWSC 1nF/0202 – 1 bondpad – 0.5x 0.5x 0.10mm
935154521410-T3T	T&R 1 000units	Au <sup>(1)</sup>	UWSC 1nF/0202 – 1 bondpad – 0.5x 0.5x 0.10mm
935154521410-W0T	WP max 400units	Au <sup>(1)</sup>	UWSC 1nF/0202 – 1 bondpad – 0.5x 0.5x 0.10mm

Table 3 - Packaging and ordering information

- (1) Au = TiW (0.3µm) / Au (3µm)
- (2) Other packing under request

Product Name	Die Name	Description
UWSC521410	WO0202410	UWSC 1nF/0202/BV : 150V – 1 bondpad – 0.5 x 0.5mm x 0.25mm
UWSC521410	WO0202410	UWSC 1nF/0202/BV : 150V – 1 bondpad – 0.5 x 0.5mm x 0.10mm

Table 4 - Die information



**Pad Metallization**

This wire bondable capacitor is delivered as standard with the bottom electrode in TiNiAu (Ti (0.1 μm)/Ni (0.3μm)/Au (0.2μm)) and top electrode in TiWAu (TiWAu (0.3μm) / Au (3μm))  
Other Metallization, such as thick Gold or Aluminum top pads are possible on request.  
Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

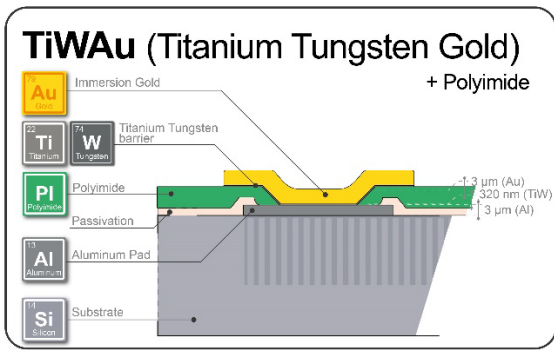


Figure 6 – Top electrode description

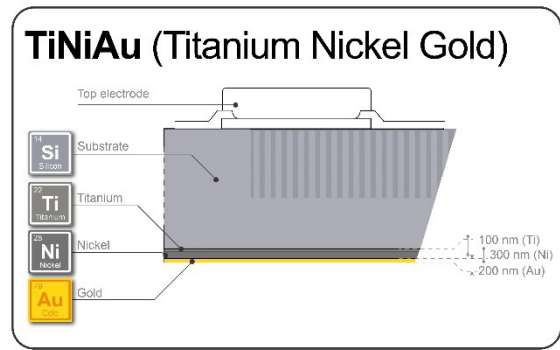


Figure 7 – Bottom electrode description

**Material regulation**

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

**Package outline**

The product is delivered as a bare silicon die.



Figure 8 - Micro photography of a 100pF Capacitor



The product is delivered as a bare silicon die, with passivation opening for contacts.

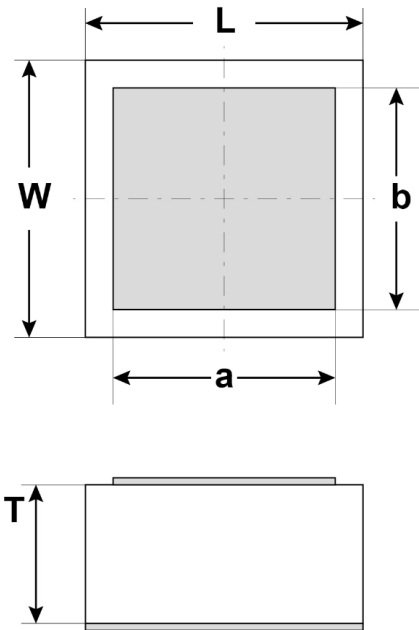


Figure 9: Package outline drawing (0.25mm thickness)

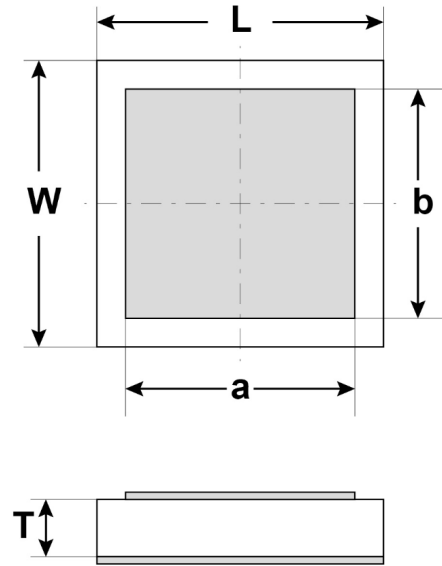


Figure 10: Package outline drawing (0.10mm thickness)

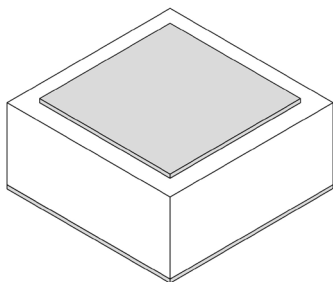


Figure 11: Package isometric view (0.25mm thickness)

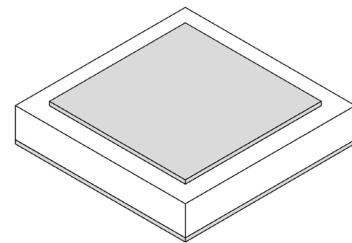


Figure 12: Package isometric view (0.10mm thickness)

L(mm)	W(mm)	T(mm)	a(mm)	b(mm)
0.50 ±0.02	0.50 ±0.02	0.25 or 0.10 ±0.01	0.38	0.38

Table 5 - Dimensions and tolerances

**Assembly**

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 13 Scan this QR Code to access the Murata Silicon Capacitor web page

**Packaging format**

Please refer to application note 'Products Storage Conditions and Shelf Life'.

**Tape and Reel:** Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

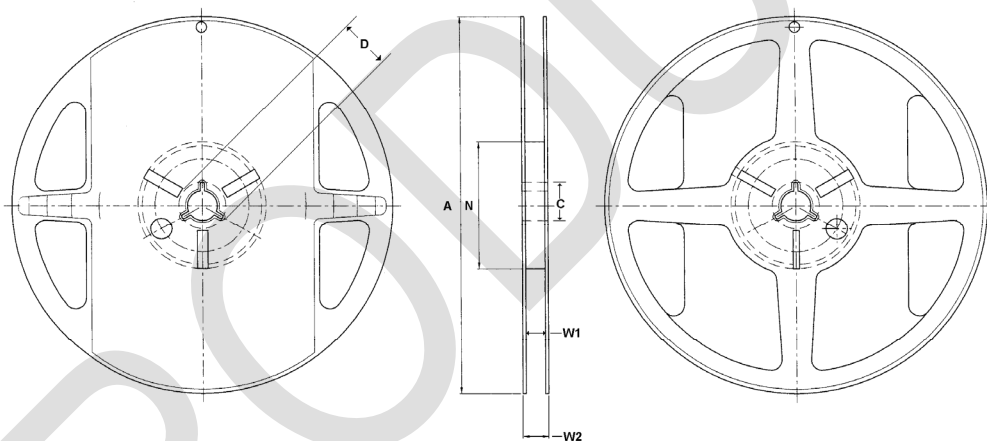


Figure 14 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9	11.5

Table 6 – Reel dimensions (mm)

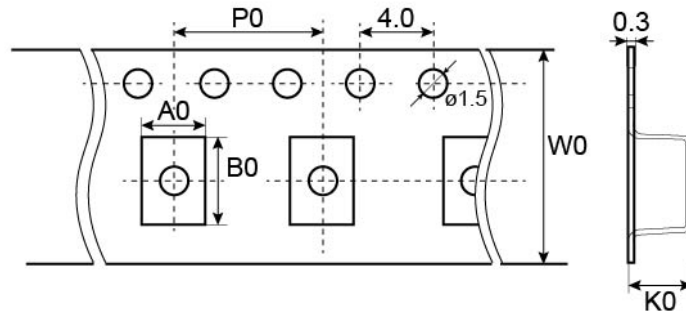


Figure 15 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0
Ao	Bo	Ko		
0.56	0.56	0.31	8 mm	4mm

Table 7 - Tape dimensions (mm)



**Film Frame Carrier:**

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

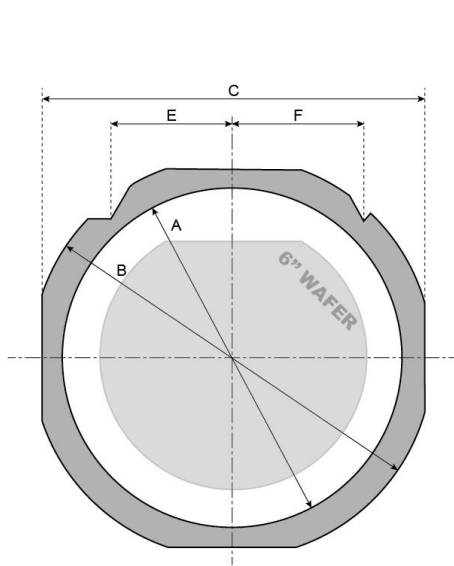


Figure 16 FF070 Frame with a 6" wafer

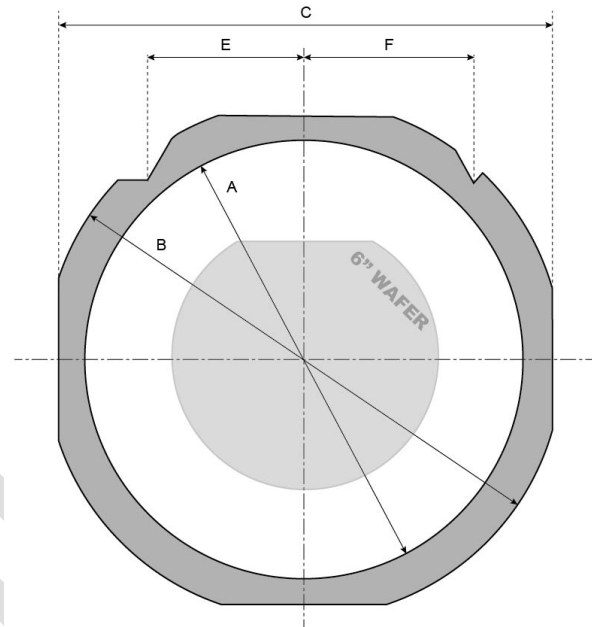


Figure 17 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 <sup>(1)</sup>	DTF-2-6-1	7.638"	8.976"	8.346"	0.048"	2.370"	2.5"
FF108 <sup>(1)</sup>	DTF-2-8-1	9.842"	11.653"	10.866"	0.048"	2.381"	2.5"

Table 8 - Frame dimensions (inches)

(1) or equivalent



**Waffle pack:**

Please refer to application note 'Waffle Pack Chip Carrier Handling & Opening Procedure'. Dies are not flipped in the waffle pack cavity (wire bond pad up).

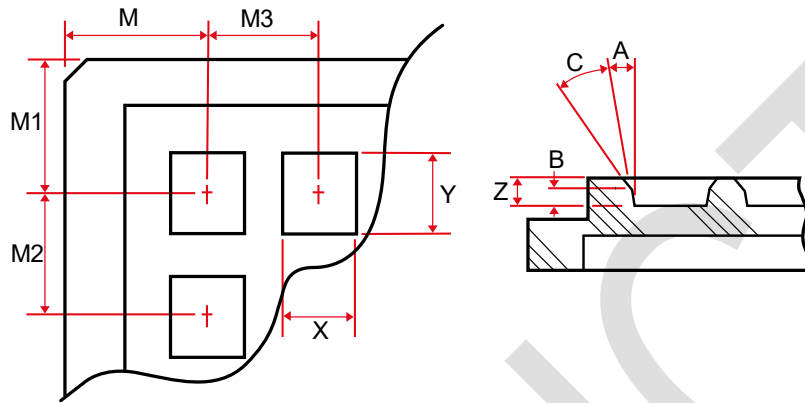


Table 9 - Waffle pack drawing

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	0.64 ±0.05	0.64 ±0.05	0.36 ±0.05

Table 10 - Waffle pack dimensions (mm) for 250µm thick product

M	M1	M2	M3	A
4.65 ±0.08	4.65 ±0.08	2.18 ±0.05	2.18 ±0.05	15° ±1/2°

Table 11 - Waffle pack dimensions (mm) for 250µm thick product

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	0.58 ±0.05	0.58 ±0.05	0.28 ±0.05

Table 12 - Waffle pack dimensions (mm) for 100µm thick product

M	M1	M2	M3	A
4.89 ±0.08	4.89 ±0.08	2.16 ±0.05	2.16 ±0.05	18° ±1/2°

Table 13 - Waffle pack dimensions (mm) for 100µm thick product



**Expander grip ring 6" diameter:**

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

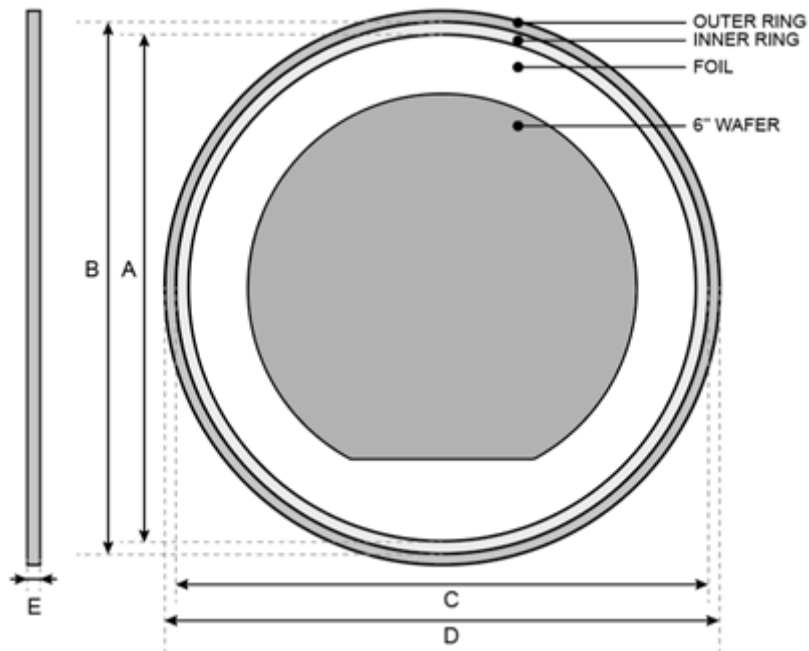


Figure 18 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 <sup>(1)</sup>	7.670"	7.973"	7.975"	8.280"	0.236"	None

Table 14 - Frame dimensions (inches)

(1) or equivalent



## Definitions

Data sheet status

**Objective specification:** This data sheet contains target or goal specifications for product development.

**Preliminary specification:** This data sheet contains preliminary data; supplementary data may be published later.

**Product specification:** This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

## Revision history

Revision	Date	Description	Author
Release 1.00	2014 July 25th	Creation	OGA
Release 1.01	2015 Nov 25th	Update	OGA
Release 1.02	2016 Jan 18th	Update	OGA
Release 1.03	2016 March 18th	Top finishing change	OGA
Release 1.04	2017 June 16th	Murata version	OGA
Release 1.05	2017 July 13th	Update	OGA
Release 2.01	2018 April 23th	Transfer FBC 0001	MSI / OGA
Release 3.00	2022 Sept. 08th	Drawings update	OGA, DYE
Release 3.01	2025 Oct 21st	Ordering information has been updated according to the latest product lineup and specification.	CGU, HFU

## Disclaimer / Life support applications

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