

Ultra large Band Wire bondable Vertical Silicon Capacitor UWSC 0303 10nF BV100



Rev.3.02

General description

UWSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products. The UWSC is suitable for DC decoupling and bypass applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with high rejection up to 26+ GHz.

These Ultra large band Wire Bondable MOS vertical Silicon Capacitors (UWSC) have been developed in a semiconductor process, in order to combine *ultra-deep trench MOS capacitors for high capacitance value of 10 nF* and *MIM capacitors for low capacitance value of 10 pF*, both in a 0303-package size. Other capacitance values and other package size are available as a single capacitor or capacitor array; please feel free to contact us.

UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding processes. Standard FR4 PCB can be used. The bottom electrode is in TiNiAu and the top electrode is in TiWAu. Other top finishings such as Aluminum are available on request.

Key features

- Ultra large band performance to 26 GHz
- Resonance free
- Phase stability
- High rejection at 20 GHz
- Compatible with MLCC footprint
- Ultra-high stability of capacitance value:
 - Temperature 41ppm/K (-55 °C to +150 °C)
 - Voltage <-0.02%/Volt
 - Negligible capacitance loss through ageing
- Low profile 0.1mm or 0.25mm
- Small size 0.80 x 0.80 mm (0303 format)
- Break down voltage: 100V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 00303 footprint
- Applicable for standard wire bonding assembly (ball and wedge)

Key applications

- Any demanding applications, such as medical, aerospace, industrial...
- Supply decoupling / filtering of active device
- High reliability applications
- Battery operated devices
- High temperature applications
- High volumetric efficiency (i.e. capacitance per unit volume)

Functional diagram

The next figure provides implementation set-up diagram.



Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	10	-	nF
ΔC_P	Capacitance tolerance ⁽¹⁾	@+25°C	-15	-	+15	%
T _{OP}	Operating temperature		-55	20	150	°C
T _{STG}	Storage temperature ⁽²⁾		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55°C to +150°C	-	41	-	ppm/K
RV _{DC}	Rated voltage ⁽³⁾		-	-	33 ⁽⁴⁾ 29 ⁽⁵⁾	V _{DC}
BV	Breakdown voltage	@+25°C	100	-	-	V _{DC}
ΔC_{RVDC}	DC Capacitance voltage variation	From 0V to RV _{DC} , @+25°C	-	-	-0.02	%/V _{DC}
IR	Insulation resistance	@ RV _{DC} , +25°C, 120s	-	100	-	GΩ
ESR	Equivalent Series Resistance	@+25°C, shunt mode	-	250	-	mΩ
ESL	Equivalent Series Inductance	@+25°C, SRF shunt mode	-	20	-	pH
ESD	HBM stress ⁽⁶⁾	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request

(2): without packaging

(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'

(4): 10 years of intrinsic life time prediction at 100°C continuous operation

(5): 10 years of intrinsic life time prediction at 150°C continuous operation

(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'



**Impedance characteristic of 10nF UWSC
 in Shunt mode**

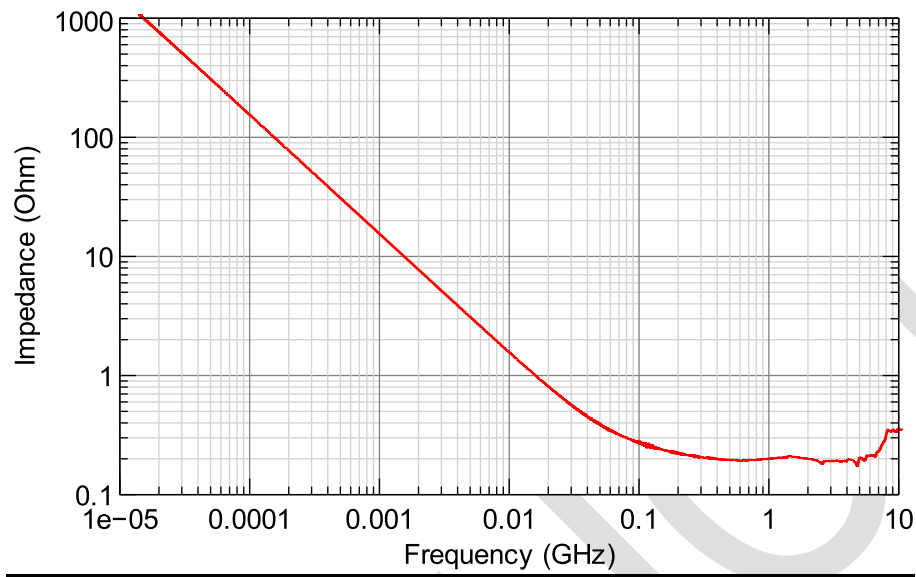


Figure 4 - 10nF UWSC measurement results
 (Impedance characteristic
 versus Frequency in shunt mode)

Schematic of 10nF UWSC in Shunt mode

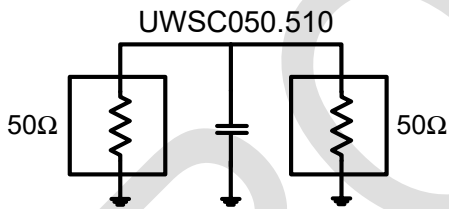


Figure 2 - 10nF UWSC measurement schematic

Example of mounted 0303

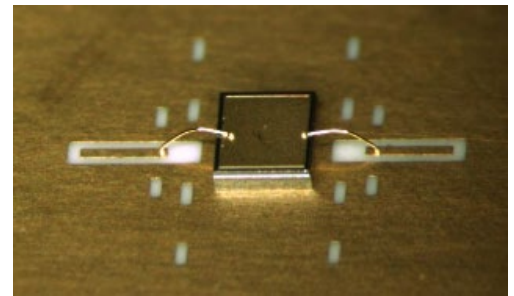


Figure 3 – micro picture of mounted 0303 UWSC



Pinning definition

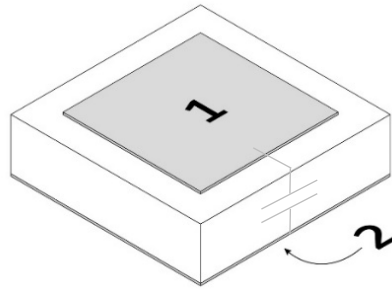


Figure 5 Pinning definition

pin #	Symbol	Metalization
1	Signal	TiWAu
2	GND	TiNiAu

Table 2 - Pining description.

Ordering Information

Part number	Package			Die Name
	Packaging	Finishing	Description	
935153050510-F1T	6" FFC	Au ⁽¹⁾	UWSC 10nF/0303/BV100 1 bondpad 0.80 x 0.80mm x 0.25mm ⁽²⁾	WK0303510
935153050510-F2T	8" FFC	Au ⁽¹⁾		
935153050510-T3T	T&R 1Kunits ⁽³⁾	Au ⁽¹⁾		
935153050510-E1T	6" GR	Au ⁽¹⁾		
935153050510-W0T	Waffle pack 400units	Au ⁽¹⁾		
935154050510-F1T	6" FFC	Au ⁽¹⁾	UWSC 10nF/0303/BV100 1 bondpad 0.80 x 0.80mm x 0.10mm ⁽²⁾	WK0303510
935154050510-F2T	8" FFC	Au ⁽¹⁾		
935154050510-E1T	6" FFC	Au ⁽¹⁾		
935154050510-T3T	T&R 1Kunits ⁽³⁾	Au ⁽¹⁾		
935154050510-W0T	Waffle pack 400units	Au ⁽¹⁾		

Table 3 - Packaging and ordering information

(1) TiWAu (TiWAu (0.3µm) / Au (3µm)).

(2) Refer to Package outline

(3) missing capacitors can reach 0.5% (only applicable to T&R)



Pad Metallization

This wire bondable capacitor is delivered as standard with the bottom electrode in TiNiAu (Ti (0.1 μm)/Ni (0.3μm)/Au (0.2μm)) and top electrode in TiWAu (TiWAu (0.3μm) / Au (3μm)).

Other Metallization, such as thick Gold or Aluminum top pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

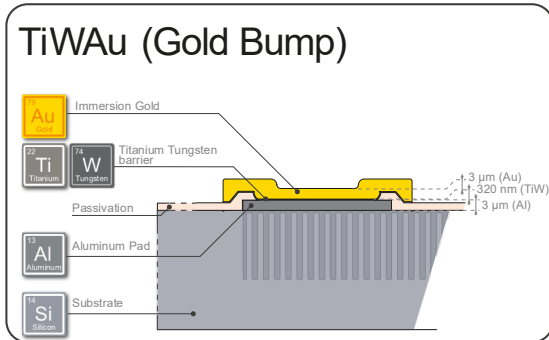


Figure 6 – Top electrode description

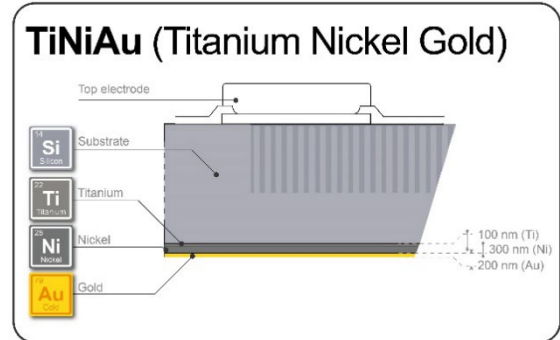


Figure 7 – Bottom electrode description

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

PROOF



Package outline

The product is delivered as a bare silicon die.

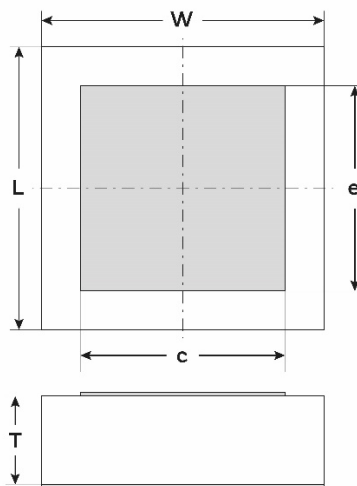


Figure 8 - Package outline drawing

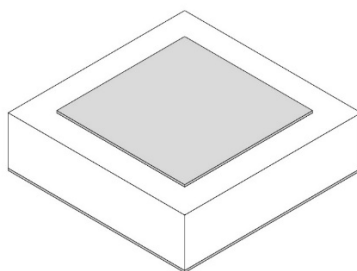


Figure 9 - Package isometric view

L (mm)	W (mm)	T (mm)	c (mm)	e (mm)
0.80 ±0.02	0.80 ±0.02	0.25 or 0.10 ±0.015	0.58	0.58

Table 4 - Dimensions and tolerances



Assembly

UWSC capacitors are directly mounted on the PCB application using die bonding and wire bonding. It is applicable for standard wire bonding assembly (ball and wedge).

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



Figure 10 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

Die orientation (No flip) within the case related to T&R orientation.

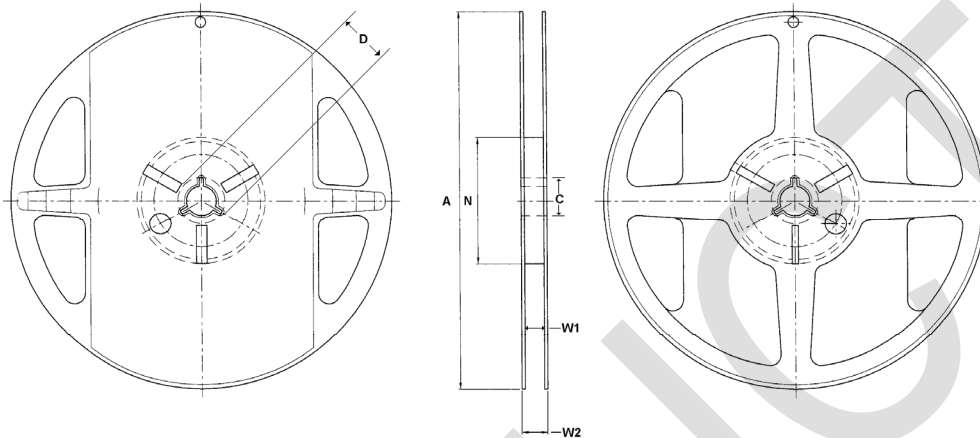


Figure 11 - Reel drawing

Tape Width	Diameter A	C	D	N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 5 – Reel dimensions (mm)

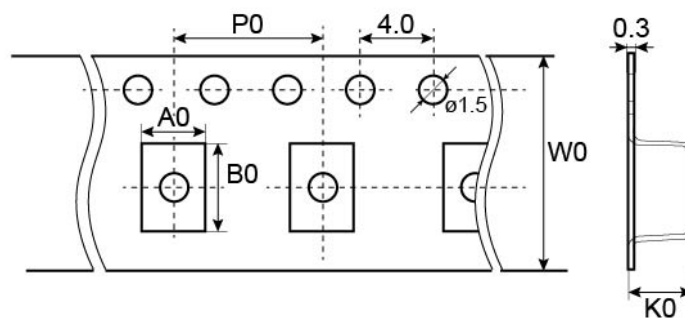


Figure 12 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
1.1	1.1	0.30	8 mm	4mm	1000

Table 6 - Tape dimensions (mm)



Film Frame Carrier:

With UV curable dicing tape (UV performed).

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

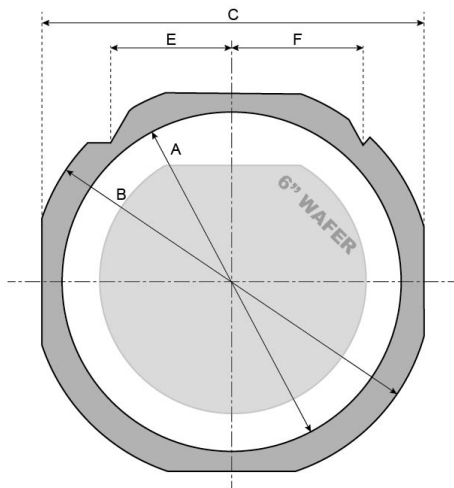


Figure 13 FF070 Frame with a 6" wafer

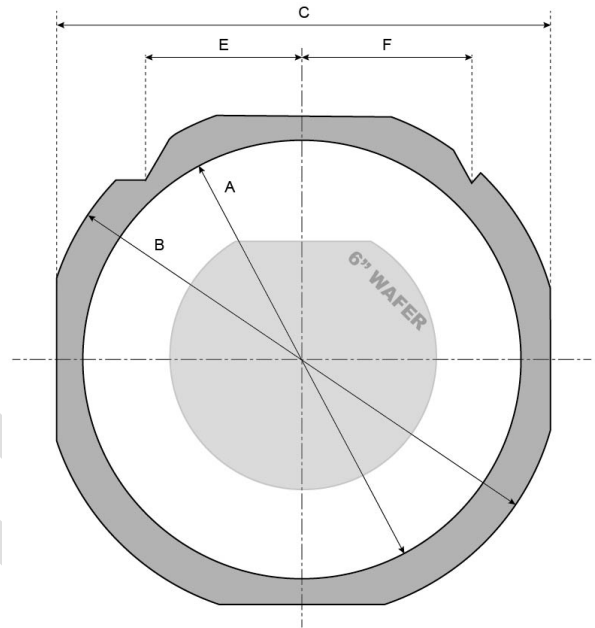


Figure 14 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 ⁽¹⁾	DTF-2-6-1	7.638"	8.976"	8.346"	0.048"	2.370"	2.5"
FF108 ⁽¹⁾	DTF-2-8-1	9.842"	11.653"	10.866"	0.048"	2.381"	2.5"

Table 7 - Frame dimensions (inches)

(1) or equivalent



Expander grip ring 6" diameter:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

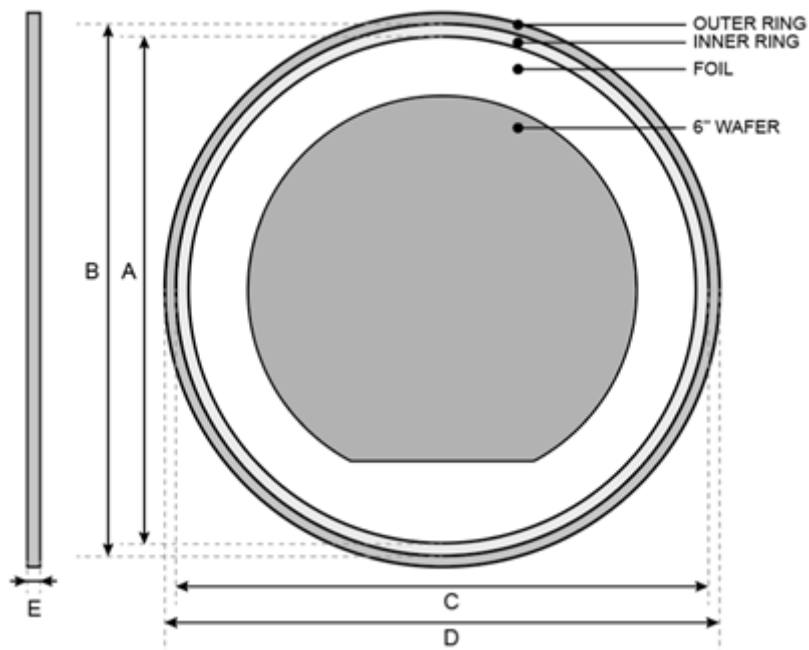


Figure 15 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 ⁽¹⁾	7.670"	7.973"	7.975"	8.280"	0.236"	None

Table 8 - Frame dimensions (inches)

(1) or equivalent

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Rev 1.0	2018 January 09th	Objective specification	OGA
Rev 1.1	2018 April 06th	Update of specification	OGA
Rev 1.2	2018 June 28th	Update	OGA
Rev 1.3	2018 September 05th	Transfer FBC 0001	OGA
Rev 2.0	2020 March 10th	Preliminary specification	SCA
Rev 2.01	2021, February 19 th	Layout and content update	CGU /LLE/SCA/OGA
Rev 2.02	2021, June 30 th	GR drawing and measurement curve	LLE/SCA/OGA
Rev 3.01	2022, June 27 th	Product specification	LLE/SCA/DDE/OGA
Rev 3.02	2025 Nov 14 th	Ordering information has been updated according to the latest product lineup and specification.	CGU / HFU

Disclaimer / Life support applications

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