Ultra-Large band Silicon Capacitor ULSC 0201 22nF BV30

Rev. 3.05

General description

ULSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The ULSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.

The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 73 KHz to 28 GHz. The performances are guaranteed up to this limit. Component might be used above this limit with degraded performances.

These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 22 nF (for kHz–MHz range) and high frequency MIM capacitors for low capacitance value for GHz range), combined in a 0201 [0.8x0.6mm] case.

The ULSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
ULSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature.

Assembly: Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminate) or flex platforms.

Bump finishing: SAC305 type 6.
Copper pads optional for embedding version and ENIG for un-bumped version, as an optional finishing.

Key features

- Ultra-Large band performance up to 28 GHz
- Resonance free
- Phase stability
- Insertion low < 0.2dB Typ. up to 28 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 400µm, 100 µm on request
- Break down voltage: 30V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 0201 footprint

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency *(i.e. capacitance per unit volume)*
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up diagram.

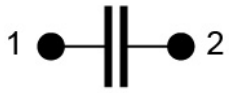


Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	22	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	16(4) 14.7(5)	V_{DC}
BV	Break down voltage	@+25°C	30	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.1	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	20	-	pH
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	220	-	mΩ
Fc-3dB	Cut-off frequency at 3dB	@+25°C	-	73	86	kHz
IL	Insertion loss	@ 28 GHz, +25°C	-	0.2	-	dB
RL	Return loss	Up to 28 GHz, +25°C	32	-	-	dB
ESD	HBM stress (6)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request.
(2): without packaging.
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation.
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation.
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.

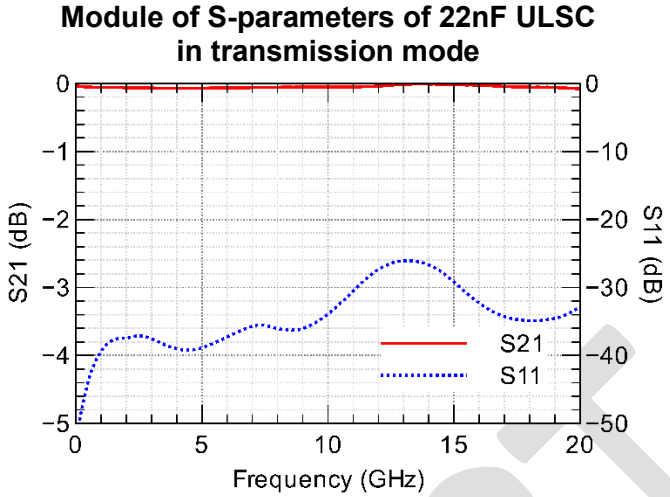
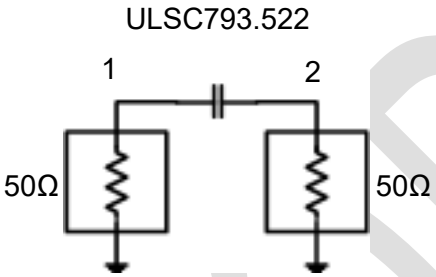


Figure 2 - 22nF ULSC Measured results (module of S-parameters)

Schematic of 22nF ULSC in transmission mode



Example of 0201 surface mounted

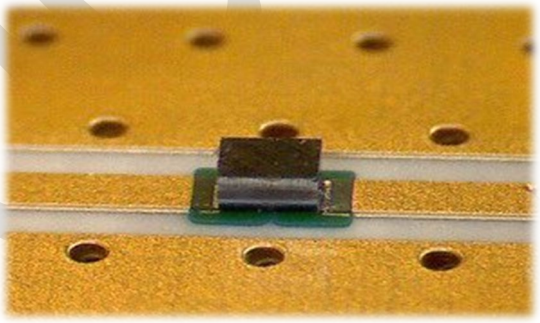


Figure 4 – micro picture of ULSC mounted on board in coplanar mode

6.6-mil Rogers 4350B.
Microstrip mode – line width = 0.400mm and gap = 0.300 mm.
(nominal 50 ohm characteristic impedance).

Figure 3 - 22nF ULSC measurement schematic

Pinning definition

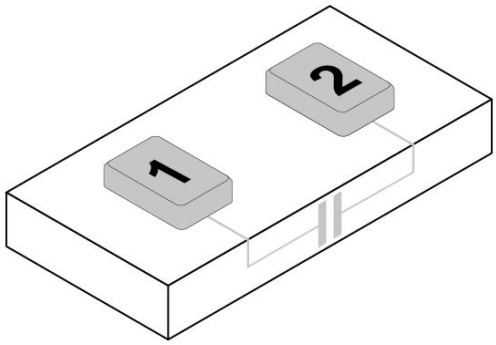


Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-225.0 / 0.0
2	Signal	225.0 / 0.0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Type number	Package		
	Packaging (1)	Finishing	Description
935156793522-T3N	7" T&R (1 000 pieces/reel) (3)	ENIG (2)	ULSC 0201 - 22nF – 2 pads – 0.8 x 0.6 mm x 0.10mm (4)
935156793522-T5N	7" T&R (5 000 pieces/reel) (3)	ENIG (2)	ULSC 0201 - 22nF – 2 pads – 0.8 x 0.6 mm x 0.10mm (4)
935155793522-T3N	7" T&R (1 000 pieces/reel) (3)	ENIG (2)	ULSC 0201 - 22nF – 2 pads – 0.8 x 0.6 mm x 0.40mm (4)
935156793522-T3S	7" T&R (1 000 pieces/reel) (3)	SAC (2)	ULSC 0201 - 22nF – 2 pads – 0.8 x 0.6 mm x 0.10mm (4)

(1) Other Film Frame Carrier are possible on request
(2) SAC = ENIG (0.1µm Au / 5µm Ni) + SAC305 type 6 or ENIG 0.1µm Au / 5µm Ni
(3) Missing capacitors can reach 0.5%
(4) Refer to Figure 9

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
ULSC793.522	XJ0201522	ULSC 22nF/0201/BV30 – 2 pads – 0.8 x 0.6 mm x 0.40mm
ULSC793.522	XJ0201522	ULSC 22nF/0201/BV30 – 2 pads – 0.8 x 0.6 mm x 0.10mm

Table 4 - Die information

Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with ENIG (0.1µm Au / 5µm Ni) (Refer to *Figure 6*).

Other Metallization, such as SAC305 type 6 bumping (Refer to *Figure7*), Copper, Thick Gold or Aluminum pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

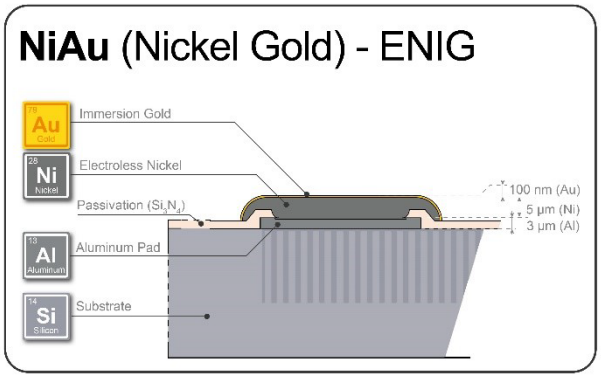


Figure 6 – Top electrode description of ENIG finishing version

Figure 7 – Top electrode description of SAC305 pre-bumped version

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

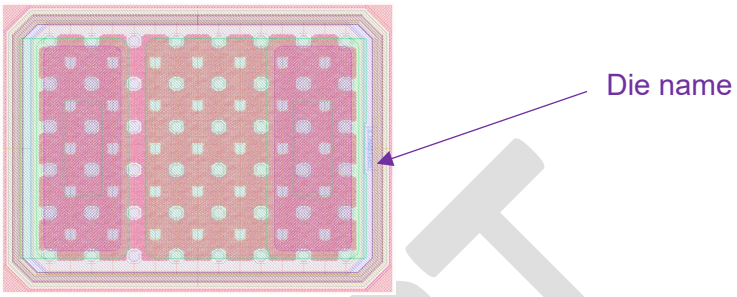


Figure 8 – Layout view

	L (mm)	W (mm)	T (mm)	c (mm)	p (mm)	e (mm)	t (mm)
Component dimension	0.80 ±0.02	0.60 ±0.02	0.41 max or 0.11 max	0.15	0.30	0.40	0.005(1) or 0.04(2) 0.065 (3)
Landing pad recommendation	/	/	/	0.164 min	0.286 max	0.414 min	/

(1) Only in case of ENIG finishing
(2) Solder joint height after reflow on board in case of SAC305 pre-bumping with mirror pads on board
(3) Solder bump height before assembly

Table 5 - Dimensions and tolerances

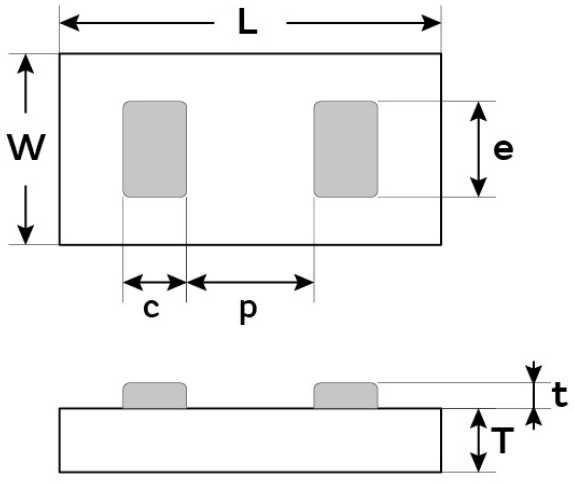


Figure 9 - Package outline drawing

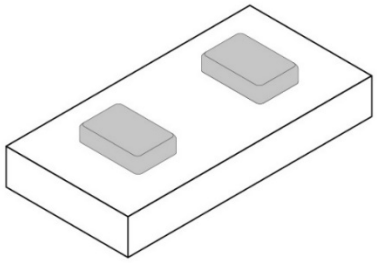


Figure 10 - Package isometric view

Assembly

ULSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note.

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 11 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

Tape and Reel: Dies are flipped in the tape cavity (bump down) withdie ID located near the driving holes of the tape.

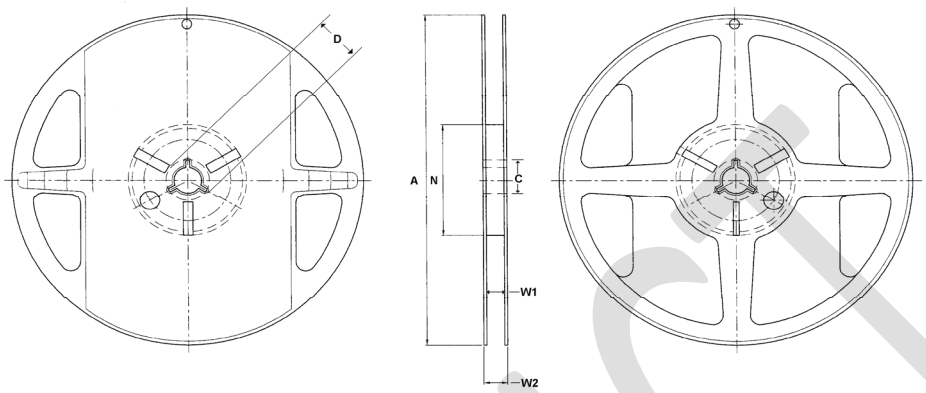


Figure 12 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 6 - Reel dimensions (mm)

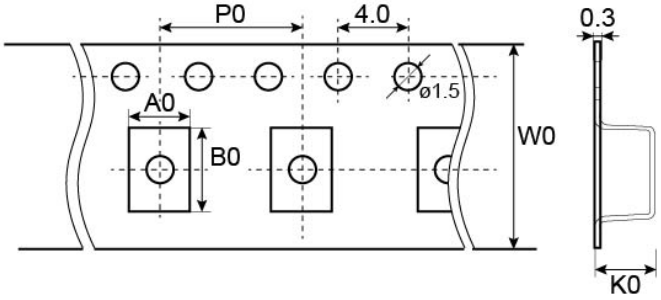


Figure 13 – Tape drawing (not to scale)

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Quantity per reel	Die thickness T(mm)
A0	B0	K0				
0.76	0.96	0.22	8	2	1 000	100µm
0.74	0.94	0.57	8	4	1 000	400µm

Table 7 - Tape dimensions (mm)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 1.00	2019 August 21st	Creation	OGA
Release 1.08	2020 August 27th	New packing update	OGA
Release 2.00	2021 April 21st	Minor update	OGA
Release 3.00	2021 May 21st	Product release	CGU, LLR, DDE, SCA, DYO, OGA
Release 3.01	2023 July 6th	Typo update	OGA
Release 3.02	2023 Nov. 13th	Extended high frequency limit	OGA, DYE
Release 3.03	2024 July 2nd	Minor Changes	SCA
Release 3.04	2025 March 15th	Complementary land pattern information	DYE / MOK / OGA
Release 3.05	2025 Oct 21th	Ordering information has been updated according to the latest product lineup and specification.	CGU, HFU

Disclaimer / Life support applications

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