Ultra Large band Silicon Capacitor ULSC 01005M 2.2nF BV11

Rev. 3.01

General description

ULSC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The ULSC is suitable for DC blocking, feedback, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.
The unique technology of integrated passive device in silicon, developed by Murata Integrated Passive Solutions, offers unique performances with low insertion loss, low reflection and phase stability from 723 KHz to 28 GHz.
These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 2.2nF (for kHz–MHz range) and MIM capacitors for low capacitance value (for GHz range), both in a SMT 01005M (0.4 x 0.2mm).
The ULSC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability. ULSC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature.

Assembly: Suitable for surface mounted application on rigid PCB, ceramic substrate, FR4 (laminate) or flex platforms.

Bump finishing: pre-bumped SAC305 type 6 or un-bumped ENIG.

Copper pads for embedding version as an optional finishing.

Key features

- Ultra large band performance to 28 GHz+
- Resonance free
- Phase stability
- Insertion loss < 0.2dB Typ. up to 28 GHz
- Ultra-high stability of capacitance value:
  - Temperature 70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile
- Break down voltage: 11V
- Low leakage current
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with EIA 008004 footprint and with EIA 01005 outline
- SAC305 15µm bumps after reflow

Key applications

- ROSA/TOSA
- SONET
- High speed digital logic
- Microwave/millimetre system
- High volumetric efficiency (i.e. *capacitance* per unit *volume)*
- Broadband test equipment

Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	2.2	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature (2)		-55	20	150	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
V_{DC}	Operating voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{VDC}	Capacitance voltage variation	From 0 V to V_{DC}, @+25°C	-	-	-0.1	%/V_{DC}
IR	Insulation resistor	@V_{DC}, +25°C, 120s	-	10	-	GΩ
ESR	Equivalent Serial Resistance(6)	@+25°C, shunt mode	-	1.5	-	Ω
ESL	Equivalent Serial Inductance(6)	@+25°C, SRF shunt mode	-	180	-	pH
Fc_{-3dB}	Cut-off frequency at 3dB(6)	@+25°C	-	723	851	kHz
IL	Insertion loss(6)	@ 28 GHz, +25°C	-	0.2	-	dB
RL	Return loss(6)	Up to 28 GHz, +25°C	30	-	-	dB
ESD	HBM stress (6) (7)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): Other tolerance available upon request
(2): Regarding the storage temperature, please refer to the following application note.: Storage and shelf life conditions
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation
(6): simulated
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

Module S-parameters of 2.2nF ULSC in transmission mode

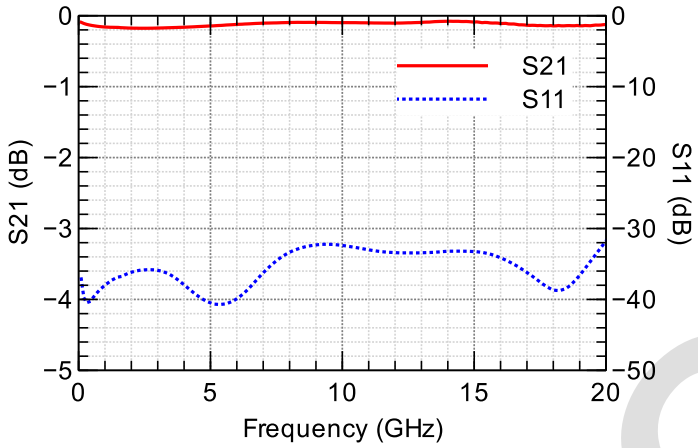
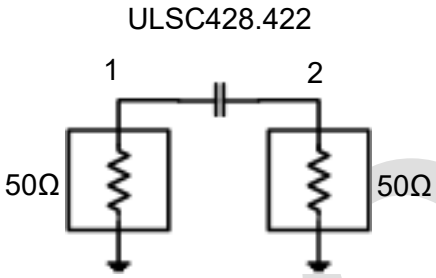


Figure 2 – 2.2nF ULSC simulation results (module of S-parameters)

Schematic of 2.2nF ULSC in transmission mode



4-mil Rogers 4350B.
Microstrip mode – line width = 0.20 mm and gap = 0.100 mm.
(nominal 50 ohm characteristic impedance).

Figure 3 – 2.2nF ULSC measurement schematic

Example of surface mounted 01005M

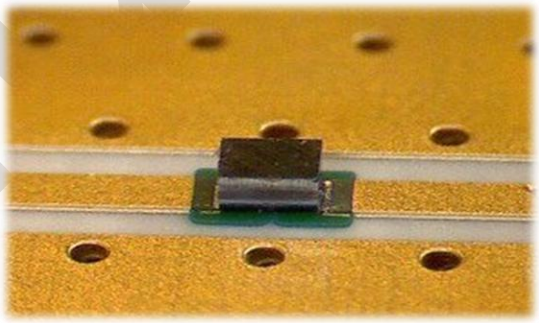


Figure 4 – micro picture of ULSC mounted on board in coplanar mode

Pinning definition

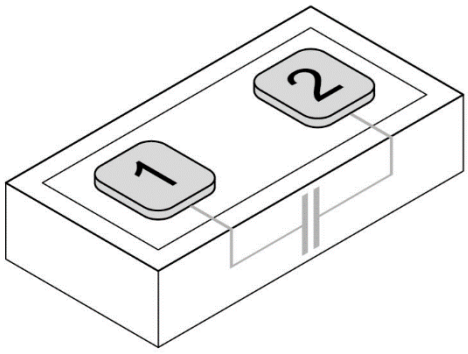


Figure 5 Pin configuration

pin #	Symbol	Coordinates X / Y
1	Signal	-104.5 / 0
2	Signal	104.5 / 0

Table 2 - Pining description. Reference (0,0) located at the centre of the die.

Ordering Information

Part number	Package		
	Packaging (1)	Finishing	Description
935156428422-T5S	7" T&R (5 000 pieces/reel) (3) (5)	SAC (2)	ULSC 01005M – 2.2nF – 2 pads – 0.40mm x 0.20mm x 0.10mm (4)
935156428422-T5N	7" T&R (5 000 pieces/reel) (3) (5)	ENIG (2)	ULSC 01005M – 2.2nF – 2 pads – 0.40mm x 0.20mm x 0.10mm (4)
935156428422-T4S	7" T&R (10 000 pieces/reel) (3) (5)	SAC (2)	ULSC 01005M – 2.2nF – 2 pads – 0.40mm x 0.20mm x 0.10mm (4)
935156428422-T4N	7" T&R (10 000 pieces/reel) (3) (5)	ENIG (2)	ULSC 01005M – 2.2nF – 2 pads – 0.40mm x 0.20mm x 0.10mm (4)

Table 3 - Packaging and ordering information

(1) Other Film Frame Carrier are possible on request
(2) SAC = ENIG (0.1µm Au / 5µm Ni) + SAC305 type 6 or ENIG 0.1µm Au / 5µm Ni
(3) Missing capacitors can reach 0.5%
(4) Refer to Figure 8
(5) For all demands including Mass Production

Product Name	Die Name	Description
ULSC428.422	XD01005422	ULSC 2.2nF/01005M/BV11 – 2 pads – 0.4 x 0.2 x 0.10 mm (4)

Table 4 - Die information

Pad Metallization

This surface mounted Silicon Capacitor is delivered as standard with SAC305 type 6 bumping (Refer to Figure6). Other Metallization, such as ENIG (0.1µm Au / 5µm Ni) (Refer to Figure7), Copper, Thick Gold or Aluminium pads are possible on request.
Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

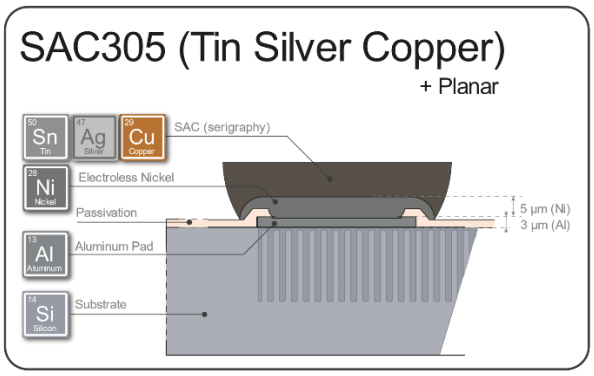


Figure 6 – Top electrode description of SAC305 pre-bumped version

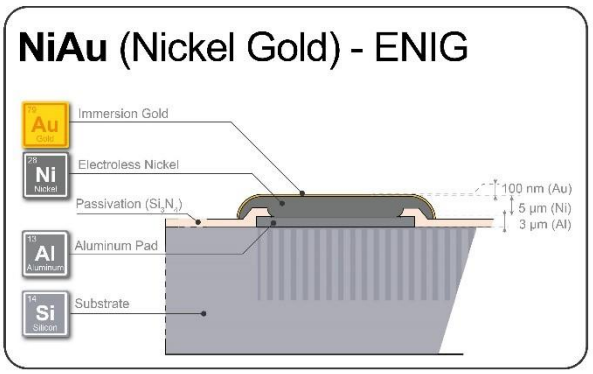


Figure 7 – Top electrode description of ENIG finishing version

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

	L (mm)	W (mm)	T (mm)	d (mm)	e (mm)	g (mm)	b (µm)
Component dimension	0.40 ±0.02	0.20 ±0.02	0.11 max	0.094	0.085	0.124	22.5 (1) $8^{\pm 2}$ (2)
Landing pad recommendation	/	/	/	0.135 min	0.074 max	0.145 min	/

Table 5 - Dimensions and tolerances

(1) *Standard with solder bump height before assembly*
(2) Only in case of ENIG finishing

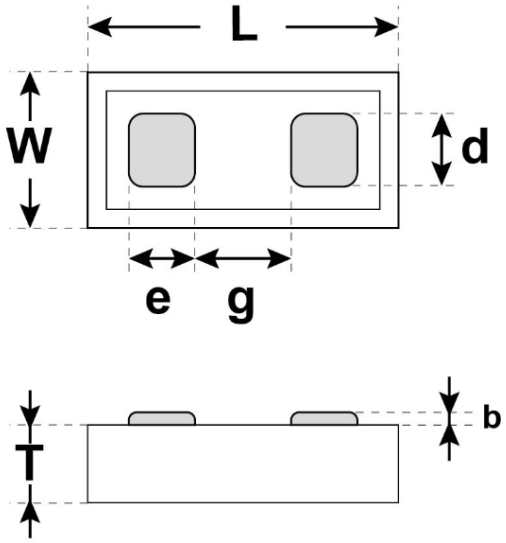


Figure 8 - Package outline drawing

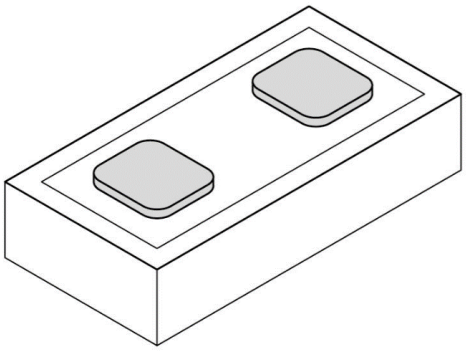


Figure 9 - Isometric view

Assembly

ULSC series is compatible with standard reflow technology.

It is recommended to design mirror pads on the PCB.

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 10 - Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

Tape and Reel: Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

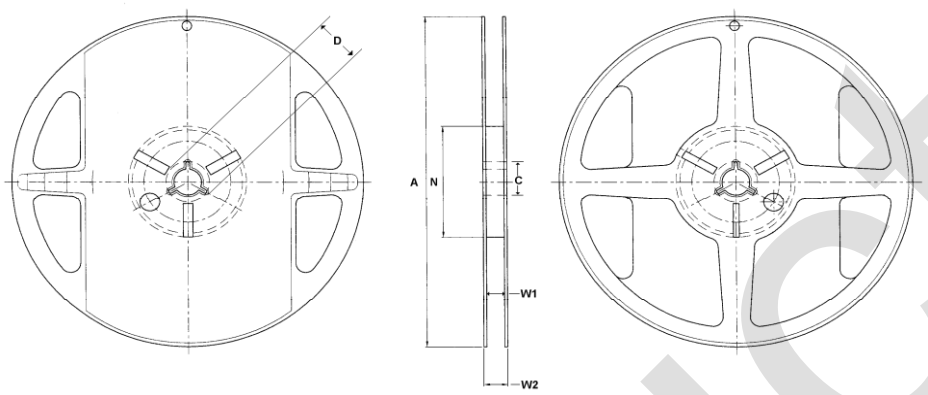


Figure 11 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	21	60	9.5	11.4

Table 6 - Reel dimensions (mm)

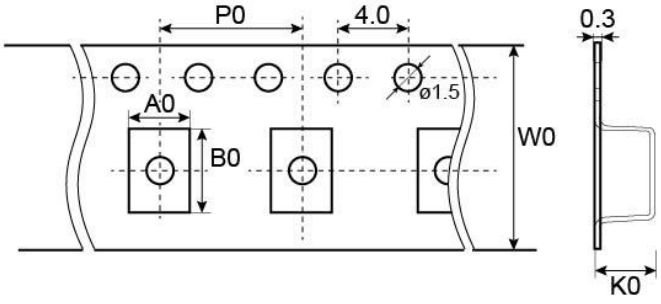


Figure 12 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
0.25	0.45	0.16	8.00	2.00	5000

Table 7 - Tape dimensions (mm)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 0.01	2021 April 8th	Initial version	OGA, SCA
Release 1.01	2021 Sept. 20th	Modif. From design review	OGA, SCA
Release 2.01	2023 Nov. 3rd	Extended high frequency limit	DYE, OGA
Release 2.02	2025 Apr. 29th	Correction on solder bump height (table 5)	LIM, OGA
Release 2.03	2025 May. 19th	Ordering information has been updated according to the latest product lineup and specification.	CGU, HFU
Release 3.01	2025 Oct. 21th	Minor update	OGA, DYE, MOY

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

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