Ultra Large band Wire Bondable and Embedded Si Cap ULEC 0404M 100nF BV11

Rev. 2.01

General description

ULEC Capacitor targets Optical communication system such as ROSA/TOSA, SONET and all optoelectronics as well as High speed data system or products.
The ULEC is suitable for DC decoupling, coupling and bypassing applications in all broadband optoelectronics and High-speed data system.
These capacitors in ultra-deep trenches in silicon have been developed in a semiconductor process, in order to integrate trench MOS capacitor providing high capacitance value of 100 nF in a SMT 0404M. The ULEC capacitor provides very high stability of the capacitance over temperature, voltage variation as well as a very high reliability.
ULEC capacitors have an extended operating temperature ranging from -55 to 150°C, with very low capacitance change over temperature (70ppm/K).
Assembly: Suitable for Wire bonded or embedded applications through existing laminated packages (LGA, BGA) or rigid PCB, FR4 (laminate) or flex platforms.
Pads finishing: Min 3µm Aluminium for wire bonding, other finishing available on request such as thin copper for embedding.
Other capacitance values and other package size are available as a single die or capacitor array, please feel free to contact us.

Key features

- Broadband performance to 20 GHz
- Resonance free
- Phase stability
- Insertion low < 1.2dB Typ. up to 20 GHz
- Ultra-high stability of capacitance value:
  - Temperature +70ppm/K (-55 °C to +150 °C)
  - Voltage <-0.1%/Volt
  - Negligible capacitance loss through ageing
- Low profile: 100 µm
- Break down voltage: 11V
- Low leakage current < 100pA
- High reliability
- High operating temperature (up to 150 °C)
- Compatible with high temperature cycling during manufacturing operations (exceeding 300 °C)
- Compatible with almost EIA 0404 footprint

Key applications

- Any demanding applications, such as medical, aerospace, industrial…
- Supply decoupling / filtering of active device
- High reliability applications
- Battery operated devices
- High temperature applications
- High volumetric efficiency *(i.e. capacitance per unit volume)*

Functional diagram

The next figure provides implementation set-up diagram.

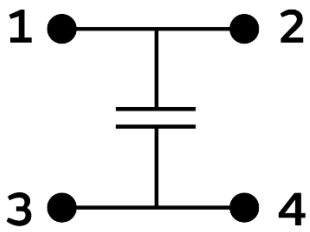


Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	100	-	nF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	150	°C
T_{STG}	Storage temperature (2)		-70	-	165	°C
ΔC_T	Capacitance temperature variation	-55 °C to 150 °C	-	70	-	ppm/K
RV_{DC}	Rated voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Break down voltage	@+25°C	11	-	-	V
ΔC_{RVDC}	Capacitance voltage variation	From 0 V to RV_{DC}, @+25°C	-	-	-0.1	$\%/V_{DC}$
IR	Insulation resistor	@RV_{DC}, +25°C, 120s	-	10	-	GΩ
ESR	Equivalent Serial Resistance	@+25°C, shunt mode	-	100	-	mΩ
ESL	Equivalent Serial Inductance	@+25°C, SRF shunt mode	-	200	-	pH
Fc_{-3dB}	Cut-off frequency at 3dB	@+25°C	-	16	19	kHz
IL	Insertion loss	@ 20 GHz, +25°C	-	0.6	-	dB
RL	Return loss	Up to 20 GHz, +25°C	12	-	-	dB
ESD	HBM stress (6)	JS-001-2017	2	-	-	kV

Table 1 - Electrical performances

(1): other tolerance available upon request
(2): without packaging
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'
(4): 10 years of intrinsic life time prediction at 100°C continuous operation
(5): 10 years of intrinsic life time prediction at 150°C continuous operation
(6): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'

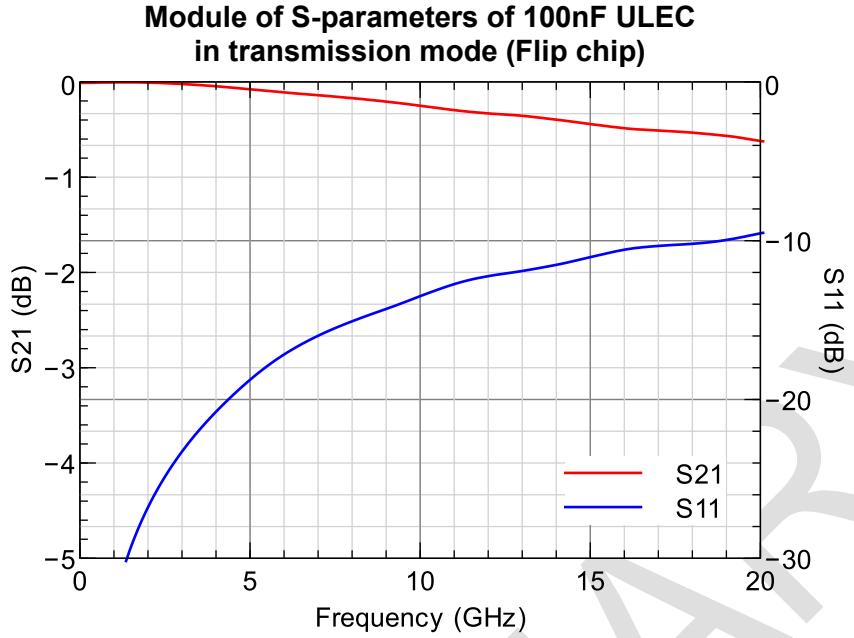


Figure 2 - 100nF ULEC measurement results (module of S-parameters)

Schematic of 100nF ULEC in transmission mode

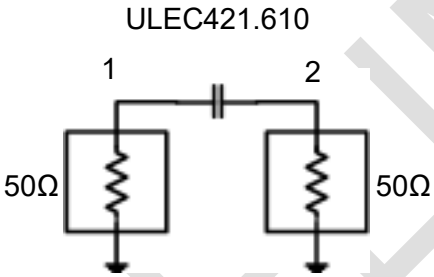


Figure 3 - 100nF ULEC measurement schematic

Example of 0404M Flip-chipped

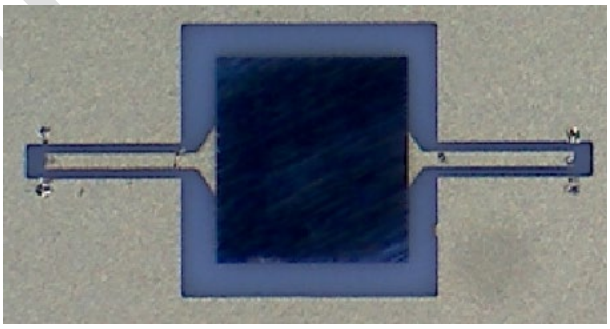


Figure 4 – micro picture of ULEC mounted on board in coplanar mode

Pinning definition

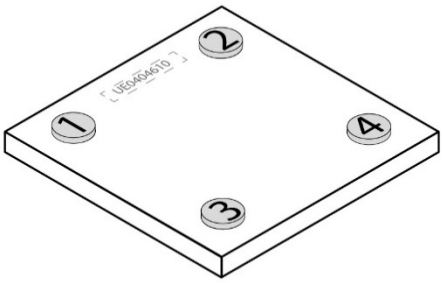


Figure 5 Pinning definition

pin #	Symbol	Coordinates X / Y
1	Signal1	-360 / 360
2	Signal1	360 / 360
3	Signal2	-360 / -360
4	Signal2	360 / -360

Table 2 - Pining description. Reference (0,0) located at the center of the die.

Parts should be glued with non-conductive paste. If conductive glue is used on the backside of the silicon capacitor, it's strongly recommended to avoid connecting the backside to electrical signal. If backside is connected to electrical signal, this signal will absolutely be the same as pads 3-4.

Ordering Information

Type number	Package		
	Packaging	Finishing	Description
935158421610-F1A	6" film frame carrier(1)	Alu(2)	ULEC 0404M - 100nF – 4 pads – 1.07mm x 1.07mm x 0.10mm
935158421610-W0A	WP 400units(3)	Alu(2)	ULEC 0404M - 100nF – 4 pads – 1.07mm x 1.07mm x 0.10mm
935158421610-T3A	T&R 1 000units(3)	Alu(2)	ULEC 0404M - 100nF – 4 pads – 1.07mm x 1.07mm x 0.10mm

(1) Other film frame carrier are possible on request
(2) Alu (AlSiCu)
(3) missing capacitors can reach 0.5%
(4) Refer to Figure7

Table 3 - Packaging and ordering information

Product Name	Die Name	Description
ULEC421.610	UE0404610	ULEC 100nF/0404M/BV11 – 4 pads – 1.07mmx1.07mmx0.10 (4)

Table 4 - Die information

Pad Metallization

This wire bonding / embedding Silicon Capacitor is delivered as standard with Aluminum (AlSiCu) pads. Other Metallization, such as Copper or thick Gold pads are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

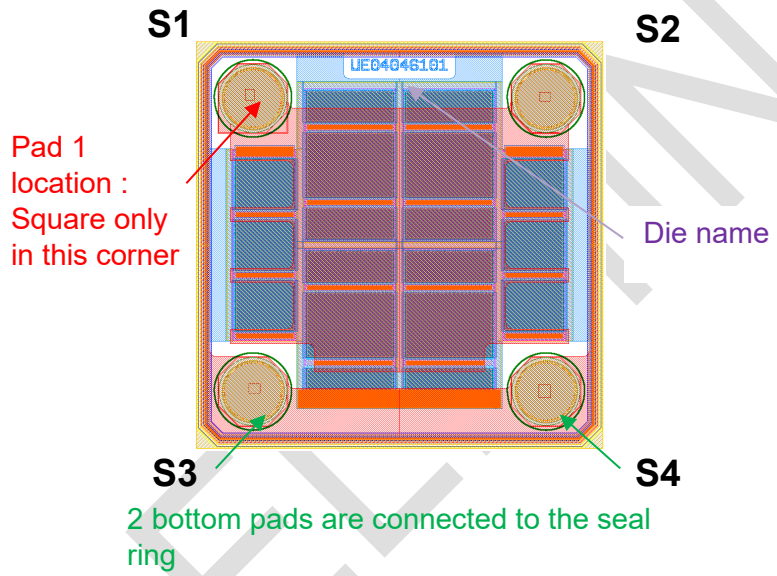


Figure 6 - Micro photography of a 100 nF Capacitor

A (mm)	B (mm)	T (mm)	c (mm)	d (mm)	e(mm)
1.07 ±0.04	1.07 ±0.04	0.10±0.01	0.152 (Al) 0.152 (ENIG) 0.20 (Cu)	0.72	0.72

Table 5 - Dimensions and tolerances

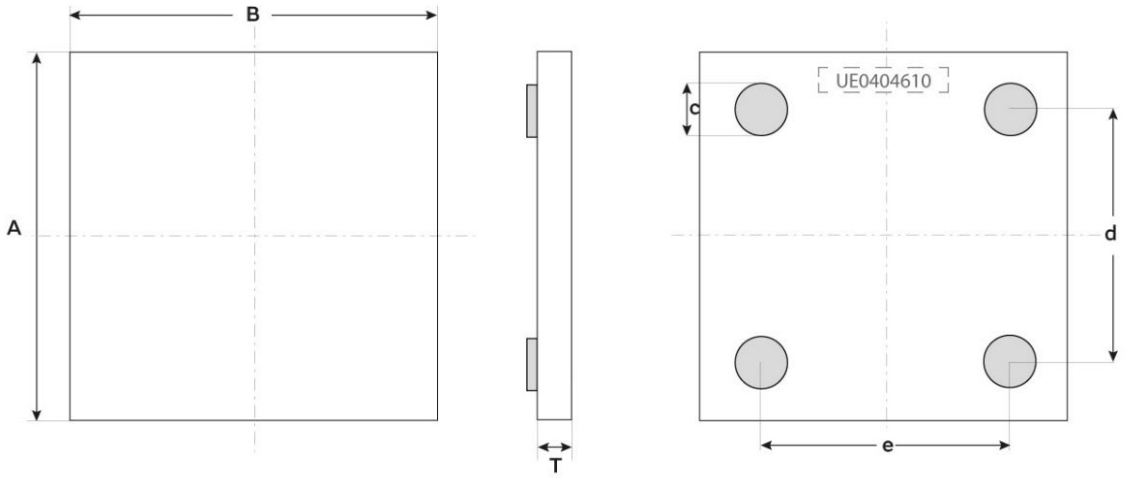


Figure 7 - Package outline drawing

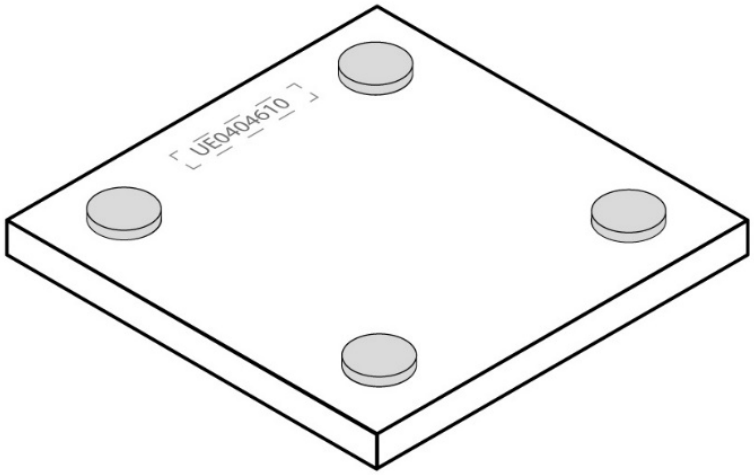
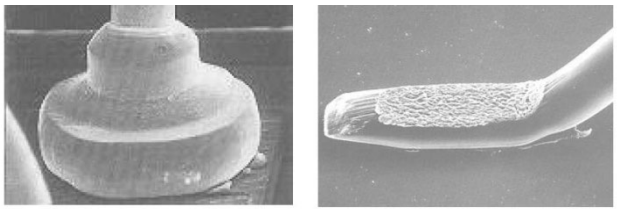


Figure 8 - Package isometric view

Assembly

ULEC series is compatible with standard wire bonding assembly (ball and wedge) technology. It can be directly mounted on the PCB using standard.



Ball bond Wedge bond

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 9 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note ‘Products Storage Conditions and Shelf Life’.

Film frame carrier:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

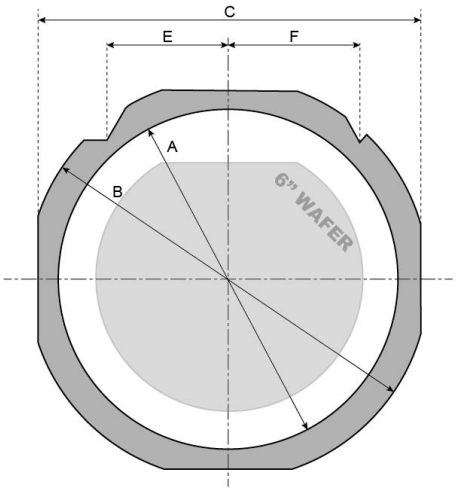


Figure 10 FF070 Frame with a 6" wafer

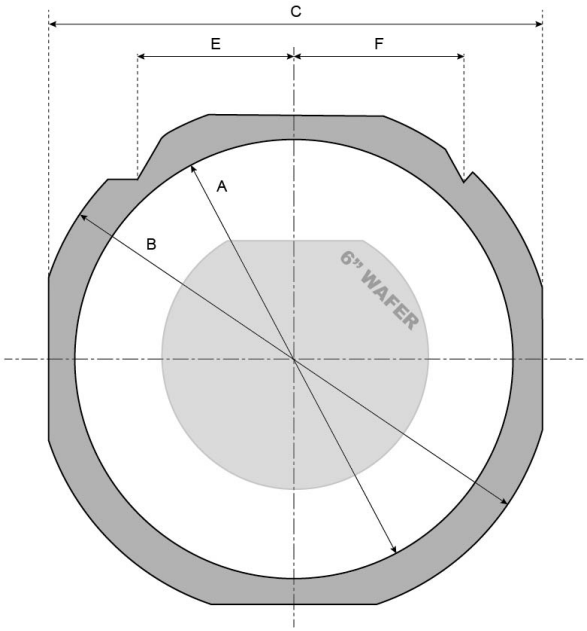


Figure 11 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 (1)	DTF-2-6-1	7.638”	8.976”	8.346”	0.048’’	2.370”	2.5’’
FF108 (1)	DTF-2-8-1	9.842”	11.653”	10.866”	0.048”	2.381”	2.5’’

Table 6 - Frame dimensions (inches)

(1) or equivalent

Expander grip ring 6” diameter:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

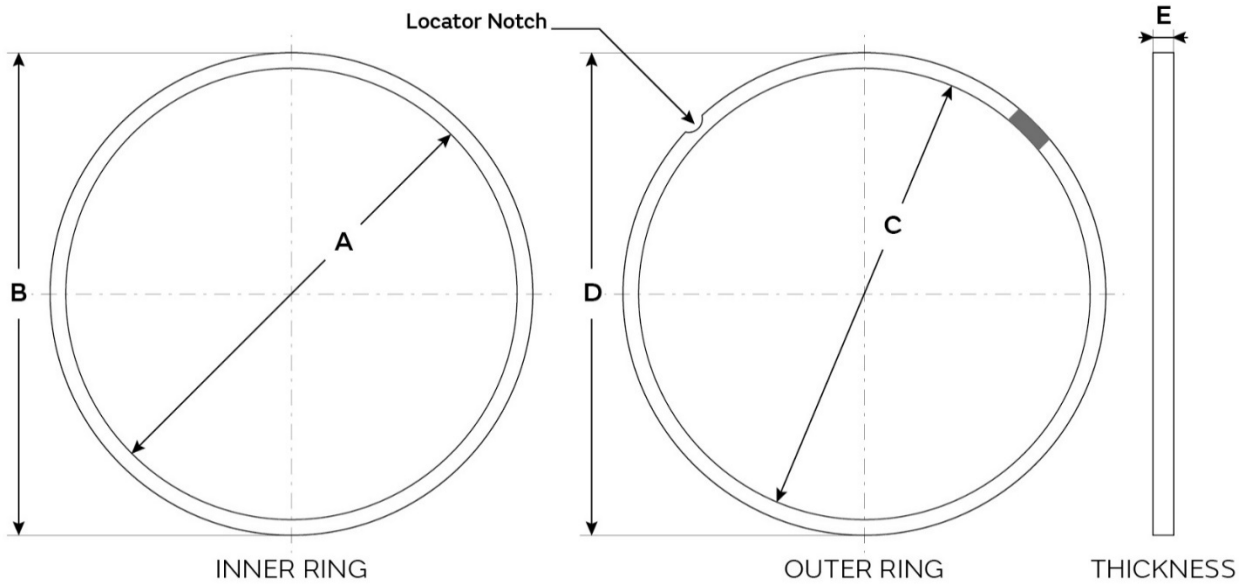


Figure 12 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 (1)	7.670”	7.973”	7.975”	8.280”	0.236”	None

Table 7 - Frame dimensions (inches)

(1) or equivalent

Tape and Reel: (Die orientation (no-flip for Aluminum and Copper pads finishing & flip for ENIG pads finishing) within the case related to T&R orientation)

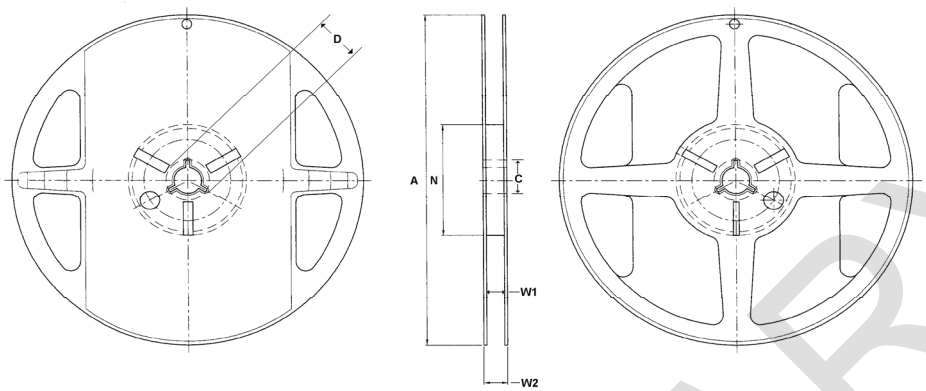


Figure 13 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	93	11.5

Table 8 - Reel dimensions (mm)

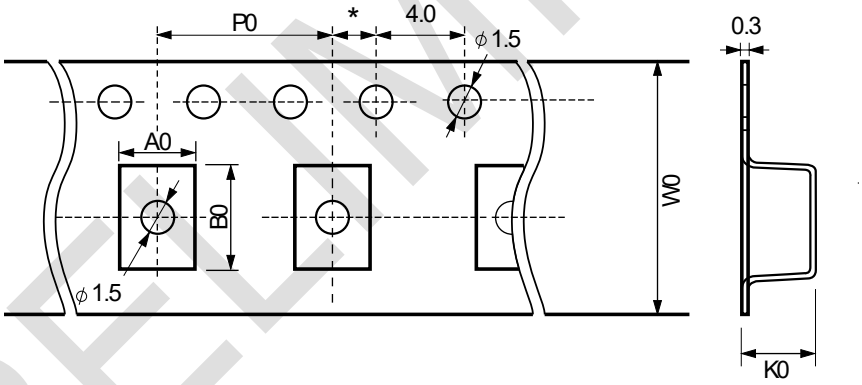


Figure 14 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Quantity per reel
A0	B0	K0			
1.20	1.20	0.47	8	4	1 000

Table 9 - Tape dimensions (mm)

Waffle pack: Die orientation (no flip) within the pocket related to waffle pack orientation

Please refer to application note 'Waffle Pack Chip Carrier Handling & Opening Procedure'

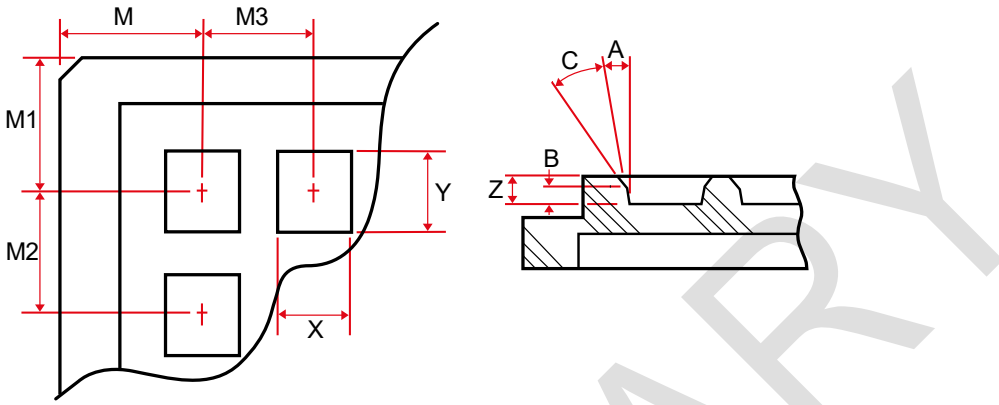


Table 10 - Waffle pack drawing

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	1.19 ±0.05	1.19 ±0.05	0.51 ±0.05

Table 11 - Waffle pack dimensions (mm)

M	M1	M2	M3	A
4.17 ±0.08	4.17 ±0.08	2.24 ±0.05	2.24 ±0.05	0° ±1/2°

Table 12 - Waffle pack dimensions (mm)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 0.01	2016 February 18th	Objective specification	OGA
Release 1.1	2016 March 18th	Graphs updated	OGA
Release 1.11	2021 April 02nd	Minor update	CGU, SCA, LLR, DDE, DYO, OGA
Release 2.00	2021 April 30nd	Preliminary status	CGU, SCA, LLR, DDE, DYO, OGA
Release 2.01	2025 Oct 20th	Key applications have been updated according to the latest market requirement. Ordering information has been updated according to the latest product lineup and specification.	CGU, HFU

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

www.murata.com
mis@murata.com

www.murata.com
mis@murata.com