Low Profile Silicon Capacitor LPSC 1206 1µF BV11

Rev. 3.02

General description

1µF LPS Capacitor targets filtering and decoupling with space constraint.
Capacitor targets RF filtering and power supplies decoupling of active devices. This version is a single 1µF capacitor in 1206 size.
The LPS Capacitor is based on PICS silicon technology.

Assembly: flip chip applications through existing laminated packages (LGA, BGA) or rigid PCB, FR4 or flex platforms suitable.
Please refer to our assembly Application note for further recommendations.

Market: All demanding markets with space constraint such as telecom, avionics engine, aerospace application and others where integration needs to be managed for performances.

Pad finishing: nickel/gold electroless (ENIG). Other finishing available on request such as Aluminium, thin copper, lead-free nickel solder coating or thin gold.

Other capacitance values and other package sizes are available as single die or capacitor array, please feel free to contact us.

Key features

- High temperature stability (up to 150°C)
  - Temperature ±0.5% (-55°C to +150°C)
  - Voltage <0.1%/Volts
  - Negligible capacitance loss through ageing
- Small size: 1206 (3.40mm x 1.80mm)
- Low profile (100µm).
- Low leakage current < 100pA
- High reliability
- Compatible with high temperature cycling during manufacturing operations (exceeding 300°C)
- Applicable for almost embedded and wire bonding application
- Compatible with almost EIA 1206 footprint

Key applications

- Any demanding applications, such as medical, aerospace, industrial…
- Supply decoupling / filtering of active device
- High reliability applications
- Devices with battery operations
- High temperature applications
- High volumetric efficiency (i.e. capacitance per unit volume)

Functional diagram

The next figure provides implementation set-up diagram.

Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@+25°C	-	1	-	µF
ΔC_P	Capacitance tolerance (1)	@+25°C	-15	-	+15	%
T_{OP}	Operating temperature		-55	20	+150	°C
T_{STG}	Storage temperature (2)		-70	-	+165	°C
ΔC_T	Capacitance temperature variation	-40°C to +200°C		70		ppm/K
RV_{DC}	Rated voltage (3)		-	-	3.8(4) 3.4(5)	V_{DC}
BV	Breakdown voltage	@+25°C	11	-	-	V_{DC}
ΔC_{RVDC}	DC Capacitance voltage variation	From 0V to RV_{DC}, @22°C	-	-	0.1	$\%/V_{DC}$
IR	Insulation resistance	@ RV_{DC}, +22°C, 120s	-	100	-	GΩ
ESR(6)	Equivalent Series Resistance	@+22°C, shunt mode	-	120	-	mΩ

Table 1 - Electrical performances

(1): other tolerance available upon request.
(2): without packaging.
(3): Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'.
(4): 10 years of intrinsic lifetime prediction at 100°C continuous operation.
(5): 10 years of intrinsic lifetime prediction at 150°C continuous operation.
(6): estimate
(7): please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'.

Pinning definition

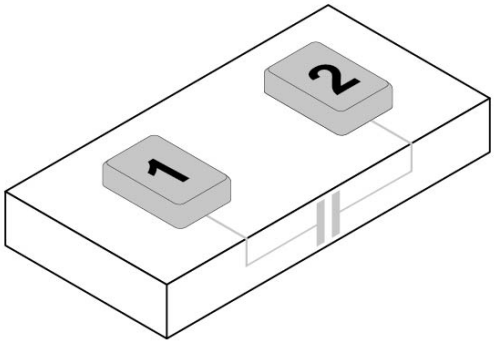

Figure 2 Pinning definition

pin #	Symbol
1	Signal1
2	Signal2

Table 2 - Pining description.

Ordering Information

Part number	Package		
	Packaging	Finishing	Description
935121427710-T3N	Tape & Reel 1000[2]	NiAu[1]	Low Profile Silicon Capacitor 1uF, -55/+150°C, 1206, 3.4 x 1.8mm, Thickness: 100um, BV: 11V[3]

Table 3 - Packaging and ordering information

[1]: Detail for pad finishing.
[2]: Missing capacitors can reach 0.5% (only applicable to T&R).
[3]: Refer to Package outline

Die Name	Description
C1206710	Low Profile Silicon Capacitor 1uF, -55/+150°C, 1206, 3.4 x 1.8mm, Thickness: 100um, BV: 11V

Table 4 - Die information

Pad Metallization

The standard pad finishing metallization is NiAu (ENIG).

Other Metallization are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes ‘Assembly Notes’ section ‘Handling precautions and storage’.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

The product is delivered as a bare silicon die.

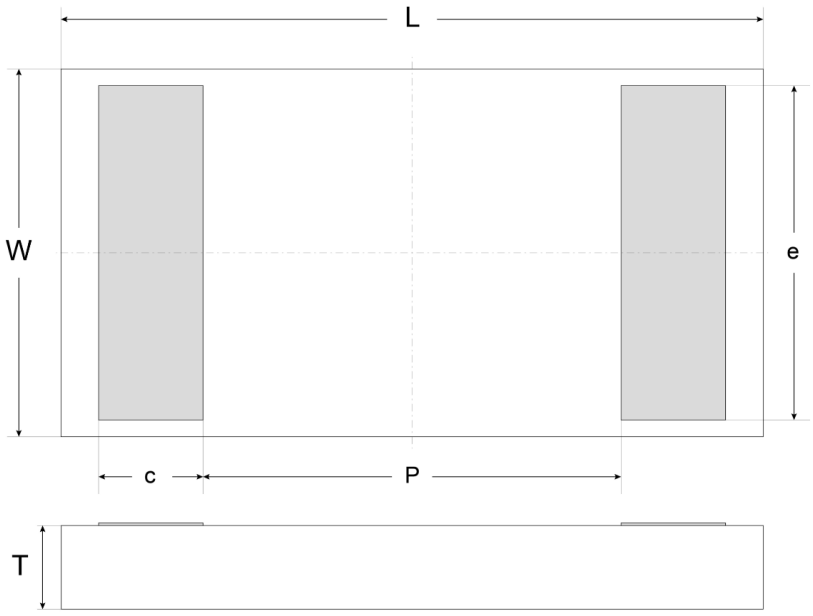

Figure 3 - Package outline drawing

L (mm)	W (mm)	T (mm)	c (mm)	P (mm)	e (mm)
$3.40^{\pm 0.04}$	$1.80^{\pm 0.04}$	$0.10^{\pm 0.015}$	0.50	2.00	1.60

Table 5 - Dimensions and tolerances

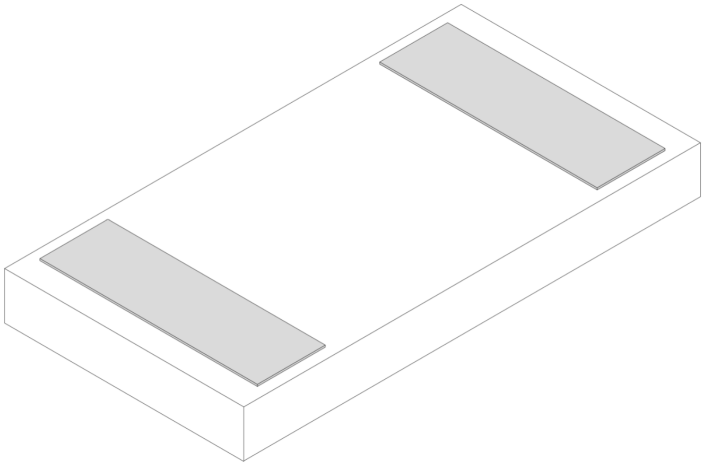

Figure 4: Isometric view

Assembly

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on https://www.murata.com/en-us/products/capacitor/siliconcapacitors and read them carefully.**

Figure 5 Scan this QR Code to access the Murata Silicon Capacitor web page

Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel:

Dies are flipped in the tape cavity (bump down) with die ID located near the driving holes of the tape.

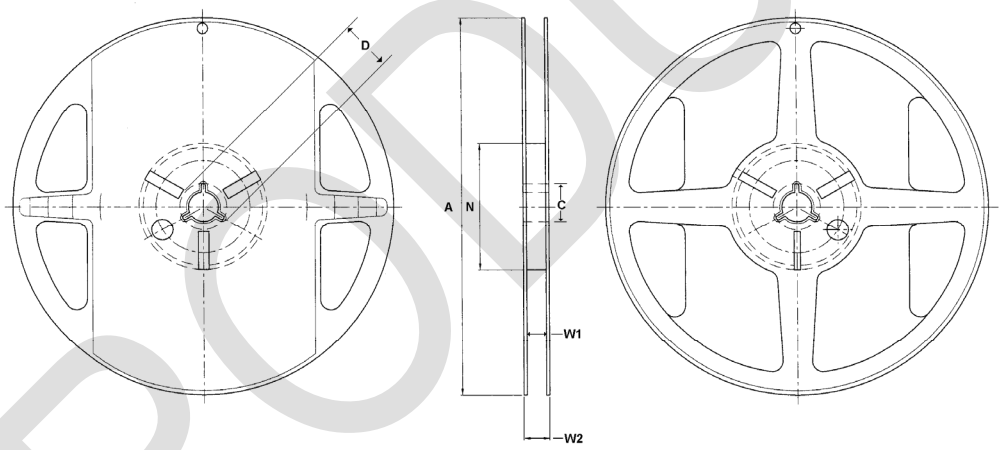

Figure 6 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9.3	11.5

Table 6 – Reel dimensions (mm)

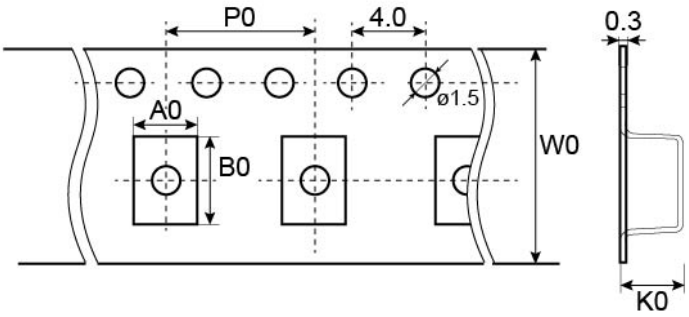

Figure 7 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Reel Capacity
Ao	Bo	Ko			
1.95	3.65	0.95	12	4	1 000

Table 7 - Tape dimensions (mm)

Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author
Release 1.00	2013 November 27th	Objective specification	LLE
Release 2.00	2021 January 29th	Preliminary specification	LLE
Release 3.00	2022 April 5th	Product specification	OGA
Release 3.01	2022 April 17th	Minor update	OGA
Release 3.02	2025 October 20th	Key applications have been updated according to the latest market requirement./ Ordering information has been updated according to the latest product lineup and specification.	CGU - HFU

Disclaimer / Life support applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Murata customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Murata for any damages resulting from such improper use or sale.

www.murata.com
mis@murata.com

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mis@murata.com