



Rev. 2.01

General description

1 μ F ETS Capacitor targets filtering and decoupling in harsh environment with high temperature and space constraint.

This Capacitor is designed to support embedded and wire bond applications.

ETS Capacitor is based on Silicon Integrated Passive technology could work to 300°C.

ET Silicon Capacitor is optimized for laminated substrate package, rigid/flex PCB, FR4, ceramic, glass, lead frame or foil platforms.

Assembly: Chip On Board (COB) Chip On Foil (COF), Chip On Glass (COG), Chip On Ceramic (COC), flip chip and embedded applications.

Market: All demanding market with High temperature constraint (up to 200°C) such as oil exploitation, aerospace application and others where integration needs to be managed for performances.

Pad finishing: Aluminum, other finishing available on request such as thin copper, nickel/gold or thin gold.

Other capacitance values and other package size are available as a single die or capacitor array, please feel free to contact us..

Key features

- Full compatible Monolithic ceramic capacitors for replacement
- Low profile (250 μ m)
- Ultra-high stability of capacitance value:
 - Temperature $\pm 1\%$ (-55°C to +200°C)
 - Voltage <0.1%/Volts
 - Negligible capacitance loss through ageing
- Small size 4x4mm +/-40 μ m (1616)
- Low leakage current <100pA
- High reliability
- Compatible with high temperature cycling during manufacturing operations (exceeding 300°C)
- Applicable for all embedded and wire bonding application

Key Applications

- Any demanding applications, such as medical, aerospace, industrial...
- Supply decoupling / filtering of active device
- High reliability applications
- High volumetric efficiency (i.e. *capacitance per unit volume*)
- Devices with battery operations
- High temperature applications



Functional diagram

The next figure provides implementation set-up diagram.

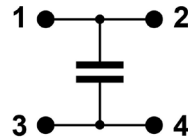


Figure 1 Block Diagram

Electrical performances

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
C	Capacitance value	@25°C	-	1000	-	nF
$\Delta C_P^{(1)}$	Capacitance tolerance	@25°C	-15	-	+15	%
T _{OP}	Operating temperature		-55		+200	°C
T _{STG} ⁽²⁾	Storage temperature		-70	-	+215	°C
ΔC_T	Capacitance temperature variation	-55°C to 200°C		62		ppm/K
RV _{DC} ⁽³⁾	Rated voltage		-	10	15 ⁽⁴⁾	V _{DC}
BV	Break Down voltage	@25°C	30	-	-	V _{DC}
ΔC_{RVDC}	Capacitance voltage variation	From 0V to 10V @25°C	-	-	0.1	%/V _{DC}
IR	Insulation resistor	@25°C, 10V, 120s	-	10	-	GΩ
ESR ⁽⁵⁾	Equivalent Serial Resistor	@+25°C, shunt mode	-	1	-	Ω
ESD	HBM stress ⁽⁶⁾	(100pF/1.5kOhms) max +/-8kV Level H3B	8	-	-	kV
ESD	HMM stress ⁽⁶⁾	ANSI/ESD SP5.6-2009 (150pF/330Ohms) max +/-8kV Setup A Level 5	8	-	-	kV

Table 1 – 1μF ETS capacitor performances

⁽¹⁾: other tolerance available upon request

⁽²⁾: without packaging

⁽³⁾: Lifetime is voltage and temperature dependent, please refer to application note 'Lifetime of 3D capacitors'

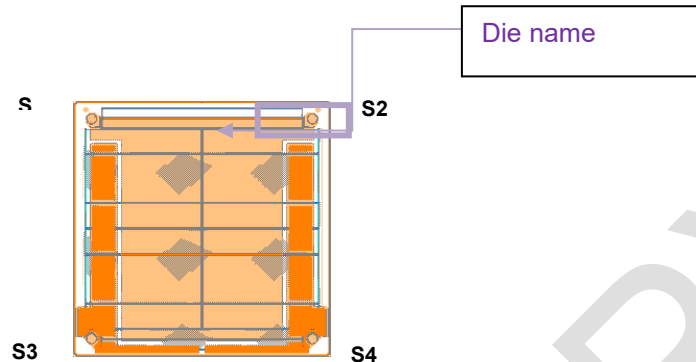
⁽⁴⁾: 10 years of intrinsic life time prediction at 100°C continuous operation

⁽⁵⁾: estimate

⁽⁶⁾: please refer to application note 'ESD Challenge in 3D Murata Integrated Passive technology'



Pinning definition



pin #	Symbol (optional)	Coordinates X / Y
1	Signal	-1720 / 1720
2	Signal	1720 / 1720
3	Signal	-1720 / -1720
4	Signal	1720 / -1720

Table 2 - Pinning description. Reference (0,0) located at the centre of the die.

Parts should be glued with non-conductive paste. If conductive glue is used on the backside of the silicon cap, it's strongly recommended to avoid to connect the backside to electrical signal. If backside is connected to electrical signal, this signal will absolutely be the same as pads 3-4.

Ordering Information for product ETSC 1616 1 μ F BV30

Type number	Package		
	Packaging	Finishing	Description
935124736710-F1A	6" film frame carrier ⁽¹⁾	Alu ⁽²⁾	1616 -1 μ F – BV30 – FFC, Alu pads
935124736710-T3A	7" T&R	Alu ⁽²⁾	1616 -1 μ F – BV30 – T&R 1000pcs, Alu pads
935124736710-W0A	Waffle Pack	Alu ⁽²⁾	1616 -1 μ F – BV30 – Waffle pack, Alu pads

Table 3 - Packaging and ordering information

(1) Other Film Frame Carrier are possible on request

(2) Alu (3 μ m) - AlSiCu

(3) Missing capacitors can reach 0.5%



Pad Metallization

This Wirebondable and Embedding Silicon Capacitor is delivered as standard with Aluminum finishing (3 μ m thickness +/- 10%), with 2 pads on each terminal.

Other Metallization, such as ENIG, Copper or Thick Gold are possible on request.

Silicon dies are not sensitive to humidity, please refer to applications notes 'Assembly Notes' section 'Handling precautions and storage'.

Material regulation

This product is RoHS compliant at the time of publication. For further information about regulation compliancy, please ask your sales representative.

Package outline

This ETSC Capacitor is delivered as a naked die, with 150 μ m opening

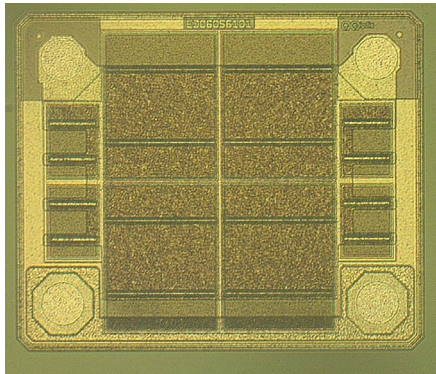


Figure 3 – Layout top view of a 1 μ F EMS capacitor.

A (mm)	B (mm)	T (mm)	c (mm)	d (mm)	e (mm)
4.00 ± 0.02	4.00 ± 0.02	0.25 ± 0.015	0.15	3.44	3.44

Table 5 - Dimensions and tolerances

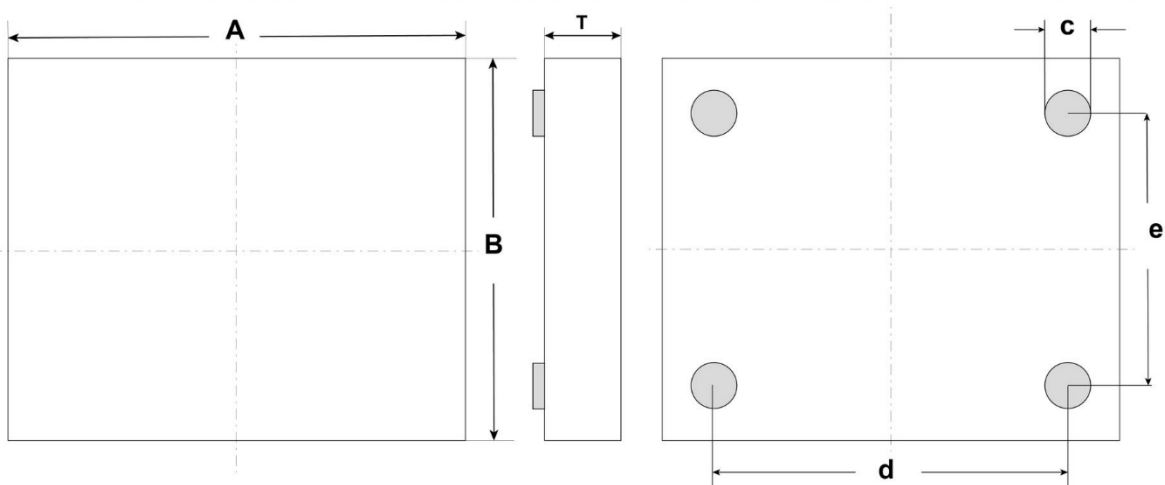


Figure 4 - Package outline drawing

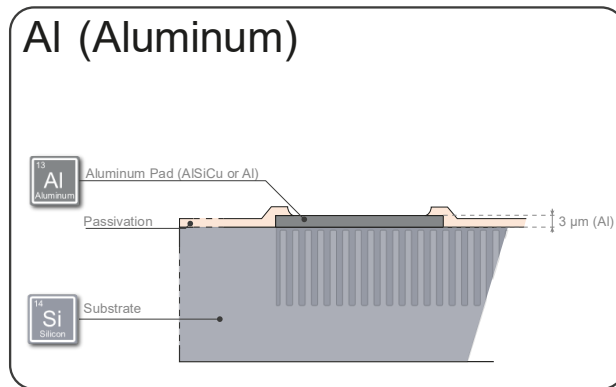


Figure 4 – Cross section on top finishing

Assembly

ETSC series is compatible with standard wire bonding and embedding technology.

For further information, please see our mounting application note

The attachment techniques recommended by Murata on the customer's substrates are fully detailed in specific documents available on our website. To assure the correct use and proper functioning of Murata capacitors **please download the assembly instructions on <https://www.murata.com/en-us/products/capacitor/siliconcapacitors> and read them carefully.**



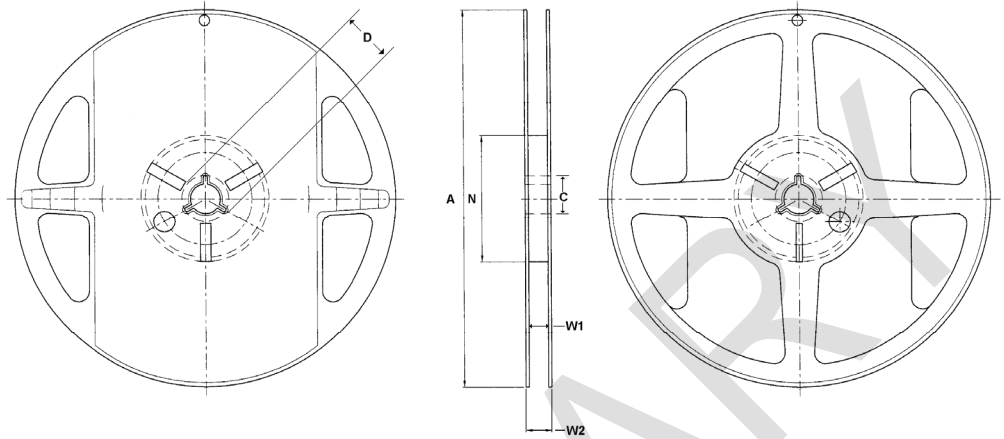
Figure 2 Scan this QR Code to access the Murata Silicon Capacitor web page



Packaging format

Please refer to application note 'Products Storage Conditions and Shelf Life'.

Tape and Reel: Dies are not flipped in the tape cavity (wire bond pad up) with die ID located near the



driving holes of the tape.

Figure 3 - Reel drawing

Tape Width	Diameter A	C	D	Hub N	W1	W2
8	178 (7 inches)	13.5	20.2	60	9	11.5

Table 4 – Reel dimensions (mm)

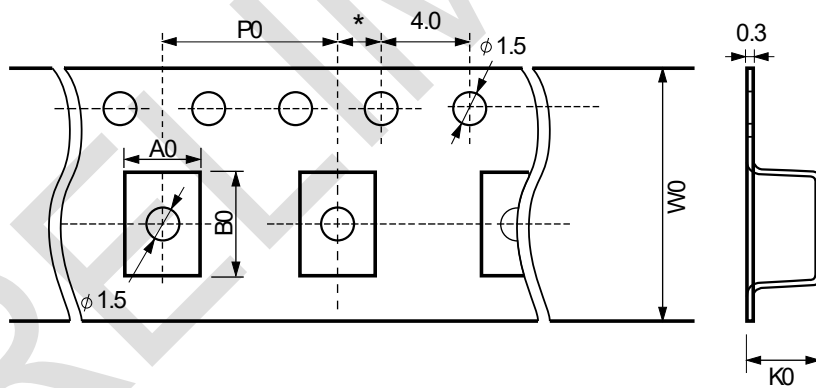


Figure 4 - Tape drawing

Cavity dimensions			Carrier tape width W0	Carrier tape pitch P0	Quantity per reel
A0	B0	K0			
!	!	!	!	!	1000

Table 5 - Tape dimensions (mm)



Film frame carrier:

With UV curable dicing tape (UV performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

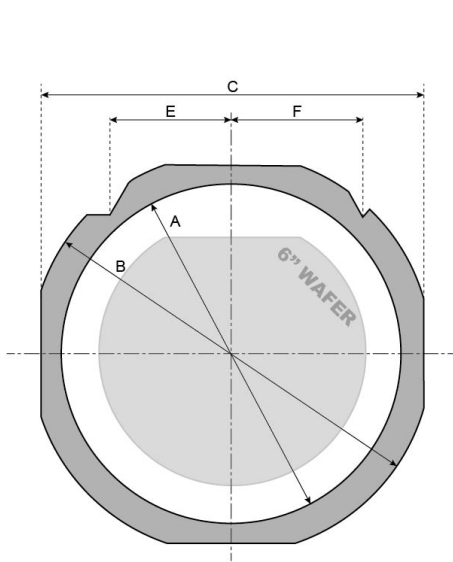


Figure 5 FF070 Frame with a 6" wafer

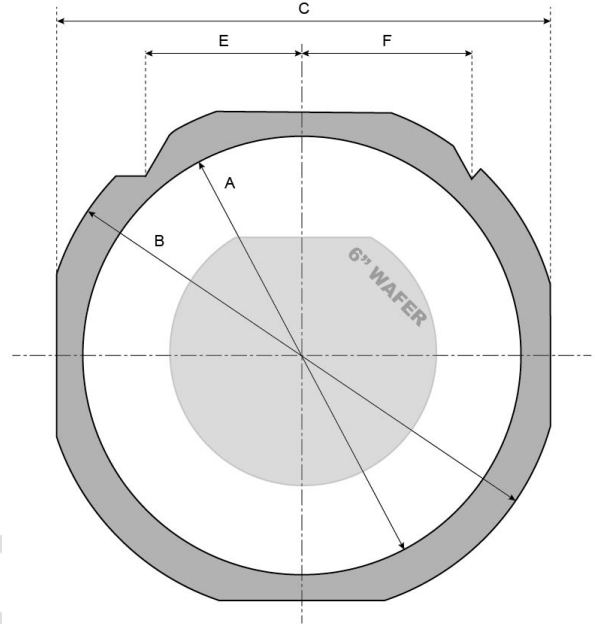


Figure 6 FF108 Frame with a 6" wafer

Frame Reference	Frame Style	Inside diameter A	Outside diameter B	Width C	Thickness	Pin location E	Pin location F
FF070 ⁽¹⁾	DTF-2-6-1	7.638"	8.976"	8.346"	0.048"	2.370"	2.5"
FF108 ⁽¹⁾	DTF-2-8-1	9.842"	11.653"	10.866"	0.048"	2.381"	2.5"

Table 6 - Frame dimensions (inches)

(1) or equivalent



Expander grip ring 6" diameter:

With UV curable dicing tape (UV not performed)

Good dies are identified using the SINF electronic mapping format. No ink is added on wafer to label other dies.

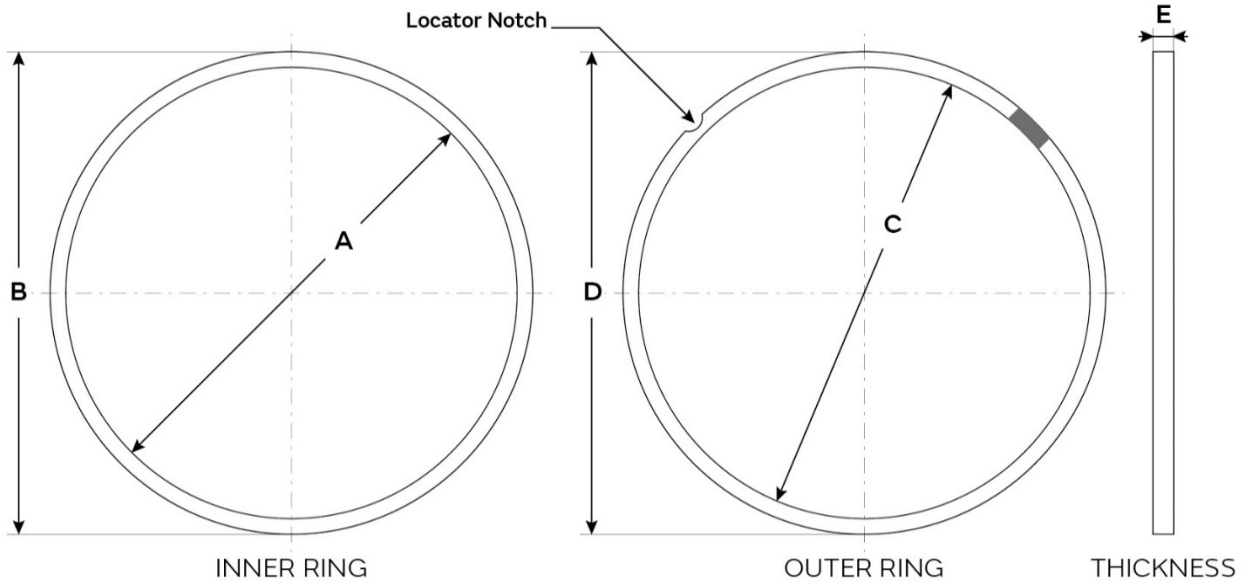


Figure 7 – Grip Ring drawing

Grip Ring Style	A	B	C	D	E	Locator Notch
GRP-2620-6 (1)	7.670"	7.973"	7.975"	8.280"	0.236"	None

Table 7 - Frame dimensions (inches)

(1) or equivalent

Waffle pack:

Please refer to application note 'Waffle Pack Chip Carrier Handling & Opening Procedure'. Dies are not flipped in the waffle pack cavity (wire bond pad up).

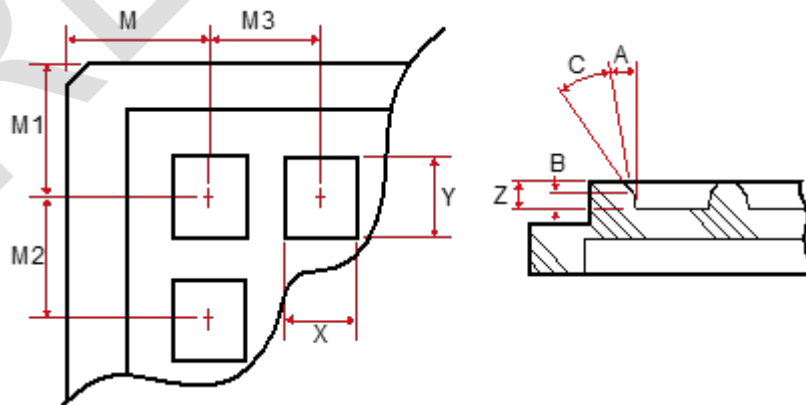


Table 8 - Waffle pack drawing

External dimensions	Max. capacity	Pocket length X	Pocket width Y	Pocket depth Z
2 inches	20 x 20	±0.05	±0.05	±0.05



Table 9 - Waffle pack dimensions (mm)

M	M1	M2	M3	A
±0.08	±0.08	±0.05	±0.05	° ±1/2°

Table 10 - Waffle pack dimensions (mm)

PRELIMINARY



Definitions

Data sheet status

Objective specification: This data sheet contains target or goal specifications for product development.

Preliminary specification: This data sheet contains preliminary data; supplementary data may be published later.

Product specification: This data sheet contains final product specifications.

Limiting values

Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Electrical performances sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

Revision history

Revision	Date	Description	Author.
1.10	13/03/2018	Objective specifications	L Lengignon
1.20	22/03/2018	Spec revision	L Lengignon
1.30	13/04/2018	Spec revision	L Lengignon
1.40	12/07/2021	Re-formatting to Murata template	G.B
2.00	06/04/2023	General update	OGA
2.01	20/10/2025	Key applications have been updated according to the latest market requirement. Ordering information has been updated according to the latest product lineup and specification.	CGU - HFU

Disclaimer / Life support applications

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mis@murata.com